ZnO nanowires and their application in field-effect transistors

by

Conor Patrick Burke-Govey

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Abstract

ZnO nanowires have shown great promise as a semiconducting material for a variety of different electronic applications at the nanoscale, and can be easily synthesised at low temperatures using the hydrothermal growth method. However, efforts to reliably produce field-effect transistors (FETs) using ZnO nanowires have been hampered by excessive charge carriers, requiring high temperature annealing ($\geq$400°C) at the expense of the low-temperature synthesis before field dependence is achieved. This thesis presents hydrothermally synthesised ZnO nanowires which can effectively be used as FETs in dry and liquid environments without requiring any annealing or post-growth processing.

The role of polyethylenimine (PEI) in the hydrothermal growth of vertical ZnO nanowires is thoroughly investigated. PEI is a polymer used to increase the aspect ratio of ZnO nanowires, but the molecular weight of the polymer and interactions with other growth precursors are often overlooked. Using 4 mM of PEI($\mathrm{M_W}$ = 1300 g/mol) results in hierarchical nanowires, consisting of large primary nanowires which abruptly terminate in thinner secondary nanowires. The secondary nanowires, with lengths of up to 10 μm and diameters below 50 nm, are synthesised during a PEI-mediated secondary growth phase, where Zn-PEI complexes continue to provide Zn^{2+} ions after the bulk of the precursors have been exhausted.

The PEI-mediated synthesis of hierarchical nanowires is used to fabricate FETs by laterally growing intersecting networks of nanowires from spaced pairs of ZnO/Ti films, which have been patterned on SiO_2/Si device substrates. All of these FETs show marked field dependence between V_G = -10 V to 10 V, despite being used without annealing. Typical on-off ratios are between 10^3 - 10^5, with threshold voltages between -7.5 V to 5 V. This is a significant result, as the majority of ZnO nanowire FETs reported in the literature require high temperature annealing. Persistent photoconductivity measurements indicate that surface states on the nanowires contribute to the intrinsic field dependence of the devices.

Hierarchical nanowires are also synthesised by modular primary and secondary hydrothermal growths. FETs fabricated using these hierarchical nanowires show less field dependence than PEI-mediated hierarchical nanowires, with limited function-

ality when used in air. The best FET measured in air operates with an on-off ratio of 10^4 and a threshold voltage of $\approx$ 0 V. Devices which are field-independent in air can be reliably gated by measuring the FETs in a wet environment, using de-ionised water as a dielectric. A back-gated wet FET operates with an on-off ratio of 10^5 and a threshold voltage of $\approx$8 V. Top-gated wet FETs operate with on-off ratios within 10^3 - 10^4, and threshold voltages within 0.4 - 0.9 V. These devices also have significantly low subthreshold swings, on the order of 80 mV/decade.

FETs are fabricated by contacting individual ZnO nanowires using electron-beam lithography, although only one vertical ZnO nanowire shows field dependence, with an on-off ratio of 10^4 and a threshold voltage of -7 V. A PEI-mediated hierarchical nanowire is also contacted and shows field dependence, with an on-off ratio of 10^2 and a threshold voltage of -6 V. The poor on-off ratio is caused by high leakage currents of the device. The contacted nanowires undergo dissolution over time, disappearing from the substrates after 8 months, and also exhibit a conducting-to-insulating transition over 48 hours. This transition can be temporarily reversed by exposure to an electron beam. Neither of these effects are reported in the literature, and their causes are speculated on.

Finally, the thesis concludes with proposals for future work to further the advances made here.

Dedicated in memory of my mum, Jacquie Burke
30/01/1954 - 03/02/2014

For some we loved, the loveliest and the best
that from his vintage rolling Time hath pressed
have drunk their cup a round or two before
and one by one crept silently to rest

— Omar Khayyam,
The Rubaiyat of Omar Khayyam (circa 1120 CE)

Acknowledgments

A PhD is not a walk in the park, and I was helped by many people at many stages through this project. I am long overdue to acknowledge them.

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Chapter 1

Introduction

1.1 Motivation

The transistor was first conceptualised in the first quarter of the twentieth century, and was eventually realised on the 23^{rd} of December, 1947, at Bell Laboratories in the United States of America [1]. The importance of this invention was realised at the time, with John Bardeen, Walter Brattain, and William Shockley being awarded the 1956 Nobel Prize in Physics for their contributions to the project. Despite these accolades, the impact of the transistor must have been far greater than any of its inventors or contemporaries could have conceived of. What followed over the ensuing decades was an enormous paradigm shift called the Digital Revolution, which has arguably had the largest technological impact on humanity since the Industrial Revolution of the nineteenth century. Digital electronics have now become ubiquitous, available to almost all people of every society, culture, and socio-economic background.

Further development of the transistor lead to devices using different operating principles and semiconducting materials. Silicon emerged as the most common semiconductor used for transistor applications, and it now underpins the majority of modern electronics, and will continue to do so for some time. However, electronics are gradually trending towards applications which silicon is no longer suitable for, such as transparent electronics [2], blue/ultraviolet photonics [3], and high temperature applications [4]. Lucrative markets are already becoming established as these niche electronics mature from prototypes to consumer electronics. As an example, transparent LCD/OLED displays are predicted to be worth billions of dollars by the end of the decade [5] (shown in Figure 1.1.) These demands have renewed an interest in wide band-gap semiconductors over the last several decades, some of which are now mature technologies with commercial applications (such as gallium nitride.)

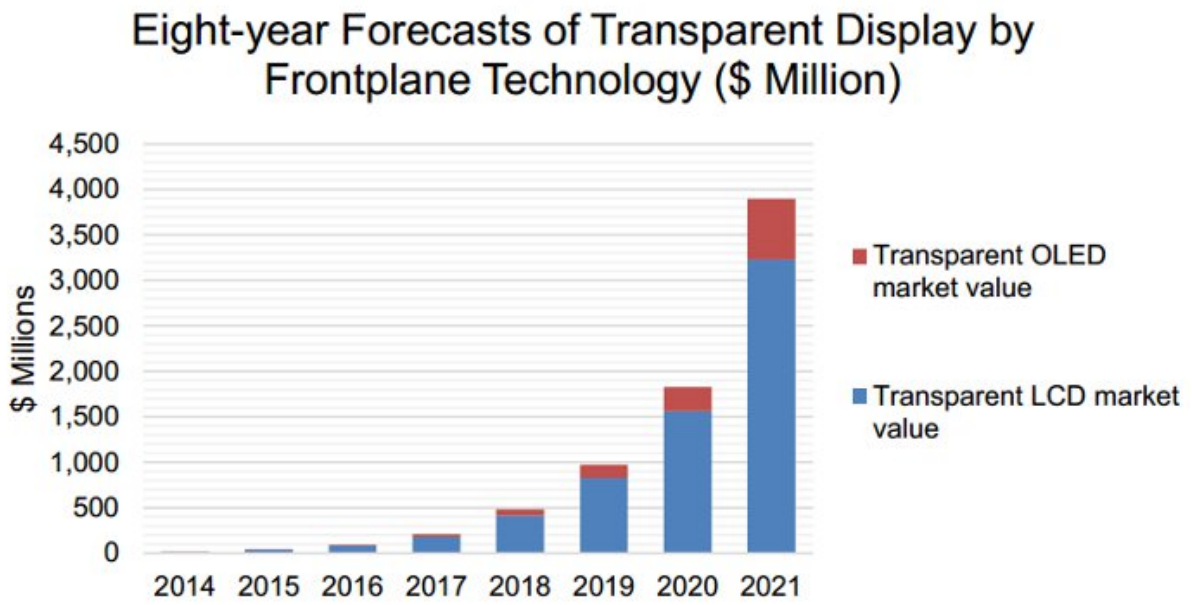

Figure 1.1: Eight-year forecasts of the transparent display markets. Figure reproduced from [5].

Silicon transistors are also facing pressure from the continual demands of scaling and miniaturising, as per Moore's law. The International Technology Roadmap for Semiconductors predicts that the current field-effect transistor (FET) architecture, the FinFET, will be reduced to its minimum size some time during 2020 [6]. New device architectures will then be required to fit more transistors on a single chip. The forefront of these new architectures are based around nanowires, with lateral all-around-gate nanowires and vertical all-around-gate nanowires predicted to find applications in commercial electronics from 2019 to 2030. This roadmap is graphically summarised in Figure 1.2(a), while Figure 1.2(b) shows specific ways of stacking nanowires to achieve more complex and high-density transistors.

These factors strongly motivate research into materials with wide bandgaps, high thermal stability, good optoelectronic properties, and ease of nanostructure synthesis. ZnO in particular has risen to the forefront of wide-bandgap semiconductor research over the past two decades due to its myriad of attractive properties. In addition to its intrinsic physical properties, ZnO nanostructures can be readily synthesized through a variety of means [9]. Perhaps the most promising synthesis route is the hydrothermal method, which is a low-cost, low-temperature wet chemical method for nanowire synthesis, with great potential for scaling compared to other contemporary nanowire synthesis methods [10]. Despite the potential of the synthesis route, hydrothermal ZnO nanowires are rarely used in field-effect transistor applications, primarily because of unintentionally high charge-carrier concentrations [11].

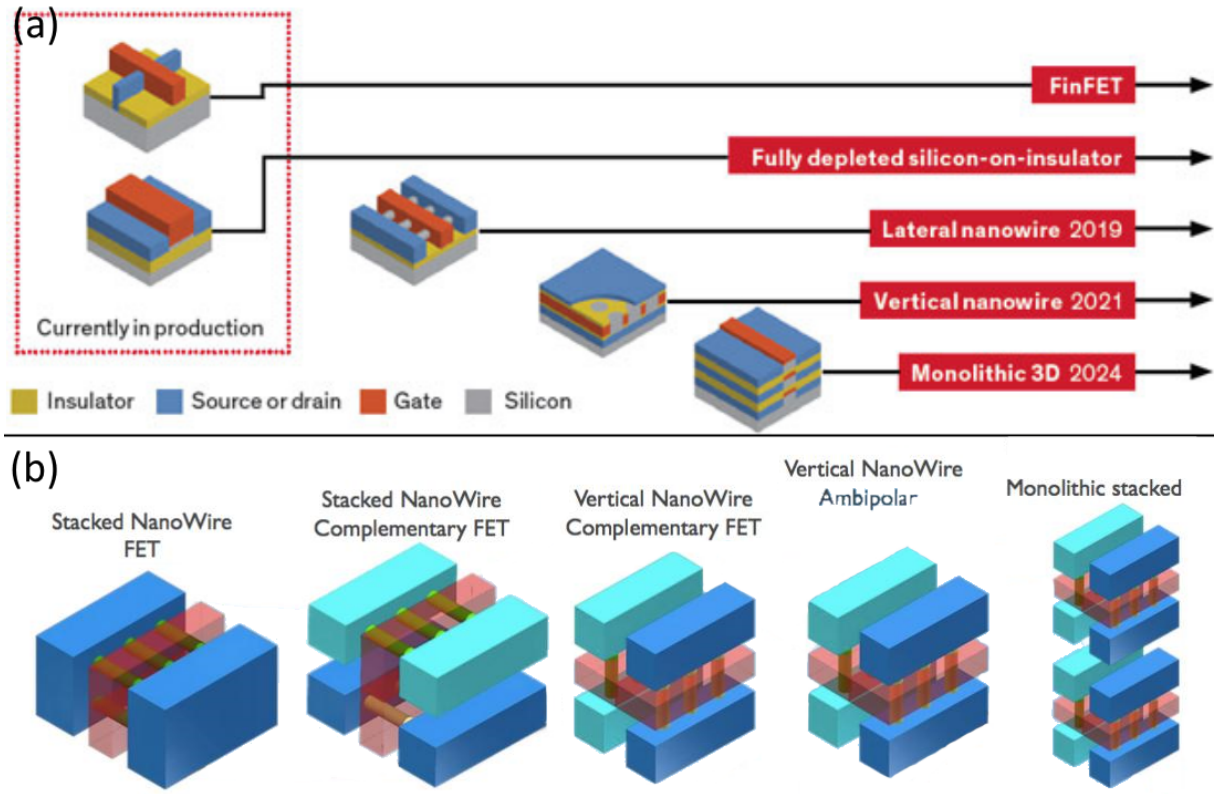

Figure 1.2: (a) A graphical representation of transistor development outlined by the International Technology Roadmap for Semiconductors [6]. Reproduced from [7]. (b) A series of different transistors of increasing complexity based on lateral and vertical nanowires. Adapted from [8].

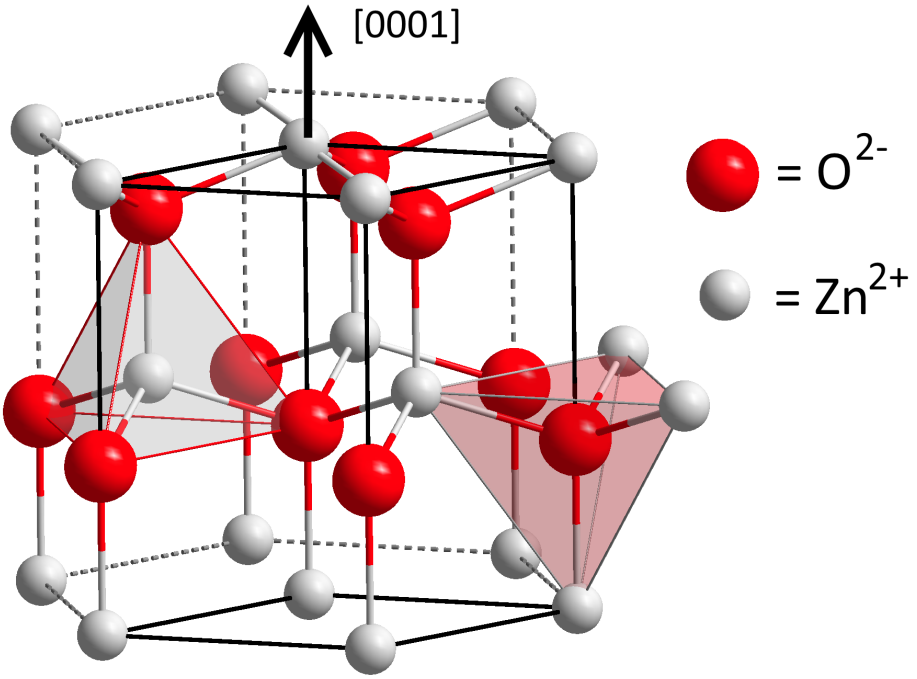

Figure 1.3: A diagram showing the hexagonal wurtzite crystal structure of ZnO. Figure adapted from [14].

This thesis aims to explore the hydrothermal synthesis of ZnO nanowires and their applications in field-effect transistors, and solve some of the problems which prohibit their greater implementation. Attention is paid to single-nanowire FETs and FETs consisting of lateral arrays of nanowires, with a particular emphasis on scalability of fabrication. These results hopefully shed some light on the feasibility of hydrothermal ZnO nanowires in FET applications, and also offer a platform for further integration into sophisticated devices, such as biosensors.

1.2 Fundamental properties of ZnO

ZnO is a Group II-VI semiconductor which occurs in the hexagonal wurtzite crystal structure (shown in Figure 1.3), although both rock-salt and zincblende structures are possible if grown under high pressure [12]. It has a very wide direct bandgap of approximately 3.37 eV [13], which corresponds to a photon wavelength of ≈368 nm, making it transparent to the visible spectrum and an excellent material for UV detection. The wide band gap also reduces thermal noise for high temperature applications. This is complemented by the high cohesive energy (7.52 eV) of the Zn-O bonds, which make the crystal structure extremely stable over high temperatures [12].

As with most II-VI semiconductors, ZnO forms mainly through ionic bonds. The O-plane and Zn-planes in the ZnO crystal structure are effectively ionised as O^{2-} and

Zn^{2+}, giving rise to a permanent dipole moment [15]. This also gives ZnO a very strong piezoelectricity, which is useful for many different micro-electromechanical devices and applications, such as ambient energy scavenging and wearable electronics [16]. Piezoelectric effects can also be combined with FET applications, which gives rise to the piezotronic effect. This has opened up a new class of ZnO NW devices over the past decade, with future applications in a variety of sensors and other similar devices [17].

The large bandgap of ZnO is coupled with an extremely high free exciton binding energy of 60 meV [12], which is roughly 2.4 times higher than the energy ($k_BT \approx 25$ eV) of room temperature thermal phonons. Free excitons are therefore theoretically stable at room temperature, which has important implications for devices such as solar cells and lasers [12]. These characteristics make ZnO a very attractive material for UV and optoelectronic applications.

ZnO also readily forms into a wide variety of nanostructures, such as nanowires, nanobelts, nanoflakes, nanourchins, and a plethora of other morphologies [18]. These are typically synthesized through high temperature vapour phase transport (VPT) methods, or low-temperature hydrothermal / solution phase techniques. The former techniques are the most widely used, despite being expensive and prohibitive to scale. On the contrary, hydrothermal methods are cheap and very easy to scale, but the nanowires which are produced can often have unintentionally high charge carrier concentrations [11].

1.2.1 Electronic properties

Electron donors in intrinsic ZnO

The electronic properties of bulk and nanostructured ZnO have been investigated in detail over several decades, although variability across different reported samples has made authoritative measurements difficult [19]. As such, the electronic properties of ZnO are still not well understood. ZnO is a natively n-type semiconductor at room temperature, caused by shallow electron donors which are seemingly unavoidable in the material. The exact origin of the electron donors is unclear and still a matter of study [20]. Temperature-dependent Hall-effect measurements suggest that these donors have ionisation energies between 30 to 70 meV [21].

Oxygen vacancies (V_O) and zinc interstitials (Zn_I) were initially proposed as shallow electron donors in ZnO, and are still often cited as being responsible for the n-type behaviour of as-grown ZnO. However, this assumption was seriously challenged

around the turn of the millennium, with theoretical calculations by Kohan et al. [22] showing that both V_O and Zn_I have high formation energies in n-type ZnO, and are also likely to be relatively deep donors. These calculations suggested that both defects would be relatively uncommon due to their formation energies, and if they were present in crystal ZnO, their ionisation energies would be too high to donate free electrons [19]. Conversely, other research has suggested that Zn_I ionises at lower energies than previously thought [23, 24], and could possibly donate shallow electrons in ZnO. However, the rather large formation energy of Zn_I restricts the number of defects present in ZnO, limiting its ability to affect the conductivity of the material.

The role of V_O and Zn_I as electron donors in ZnO was further challenged by theoretical research published by Van de Walle [25], which showed that incorporated hydrogen is a shallow donor in ZnO with a low enough formation energy to be abundant. As such, it was suggested that H is unintentionally incorporated in ZnO, where it becomes a dominant background donor and is responsible for the n-type behaviour. The role of H in ZnO has been tested in high-quality bulk ZnO, and has been experimentally confirmed to act as a shallow donor [26].

Nevertheless, there is still disagreement about the exact dopants which donate electrons in ZnO, and whether certain dopants are shallow or deep electron donors. Other research suggests that native defects may act as shallow donors by forming complexes [19], as many native defects are only considered as point defects in theoretical calculations. Furthermore, other structural defects such as stacking faults and line defects may affect the electrical properties of ZnO, and these have not been thoroughly investigated yet. As such, there is still a lot to learn about electron donors in ZnO. A discussion of the different possible dopants and their effects on ZnO nanowire FETs is included in Chapter 3.

Residual charge carrier concentrations in ZnO

Regardless of the exact nature of the donors, it is abundantly clear that ZnO is an n-type material. Due to the variability of electrical properties between reports in ZnO, it is difficult to find values of the charge carrier concentration which are representative. High-quality bulk intrinsic ZnO typically has a charge carrier concentration on the order of 1×10^{16} cm^{-3} in the best case [21], although more often is higher by an order of magnitude or more [27]. Figure 1.4 shows the measured charge carrier concentration of high-quality intrinsic bulk ZnO as a function of $10^3/T$ (K^{-1}), alongside its theoretical fit. There have been reports of lower charge carrier concentrations in thin films of ZnO, on the order of 1×10^{15} cm^{-3} in (0001) oriented ZnO [28] and 1×10^{14}

cm^{-3} in (10$\bar{1}$0) oriented ZnO [29].

The charge carrier concentration for nanostructured ZnO also shows a significant amount of variation, although tends to be significantly higher than high-quality bulk crystals. As-grown nanowires typically have charge carrier concentrations on the order of 10^{18} - 10^{19} cm^{-3} [30, 31]. High charge carrier concentrations pose a severe problem for FET applications, as they necessitate very large gate voltages to deplete the nanowire channel and achieve switching. In particular, ZnO is degenerately doped at $n \approx 4 \times 10^{18}$ cm^{-3}, which renders most as-grown nanowires incompatible for FET use [11]. This value is explicitly calculated in Chapter 3, and the techniques used to reduce the charge carrier concentration for FET use are also described in detail with reference to electron donors present in the nanowires.

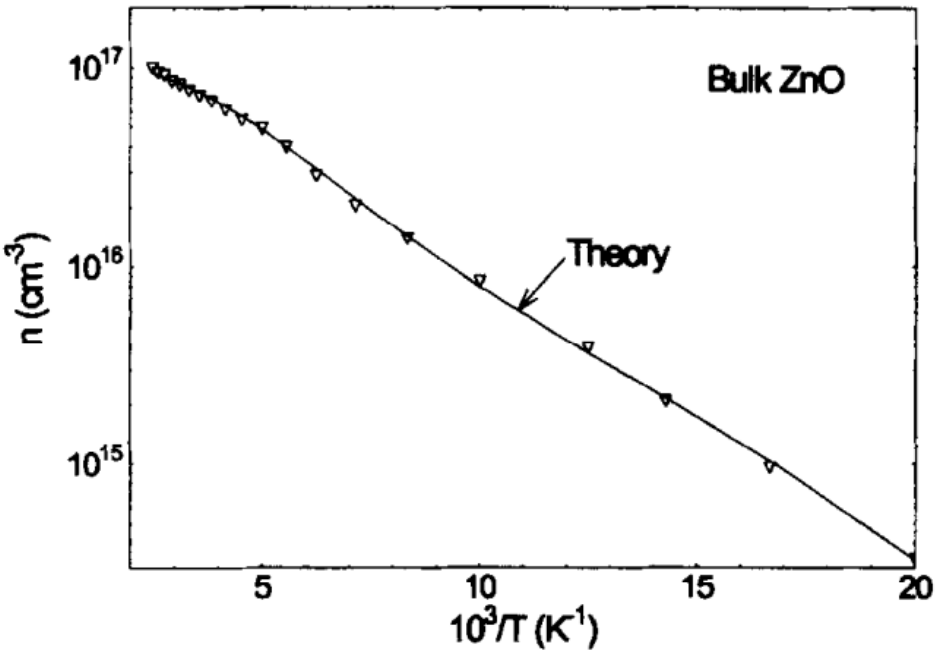

Figure 1.4: The relationship between the charge carrier concentration and temperature for high-quality bulk ZnO. Reproduced from [21]

Electron mobility in ZnO

The mobility of electrons in intrinsic ZnO has been reported several times for both bulk crystals and nanostructures, although reported values can differ considerably. The electron mobility in bulk crystals is most often determined by Hall-effect measurements, and is typically in the range of 200 cm^2 V^{-1} s^{-1} [12] for low fields at room temperature. Initial Monte Carlo simulations reported by Albrecht et al. [32] predicted that the room-temperature mobility of electrons in intrinsic ZnO should be

approximately 300 cm^2 V^{-1} s^{-1} at room temperature, which has been corroborated by further theoretical calculations yielding values around 285 - 300 cm^2 V^{-1} s^{-1} [33, 34]. However, reported mobilities of bulk ZnO are almost always lower than this, with most mobilities around 150 cm^2 V^{-1} s^{-1} or lower [12].

One of the highest electron mobility reported in bulk ZnO is 205 cm^2 V^{-1} s^{-1} at room temperature [21], which agreed very well with non-Monte Carlo predictions. This data is shown in Figure 1.5. The theoretical model used to predict the electron mobility is based on solving the Boltzmann transport equation using Rode's method, and taking into consideration major sources of scattering, such as polar-optical-phonon scattering and Coulomb scattering. The peak value was approximately 2000 cm^2 V^{-1} s^{-1} at 50K.

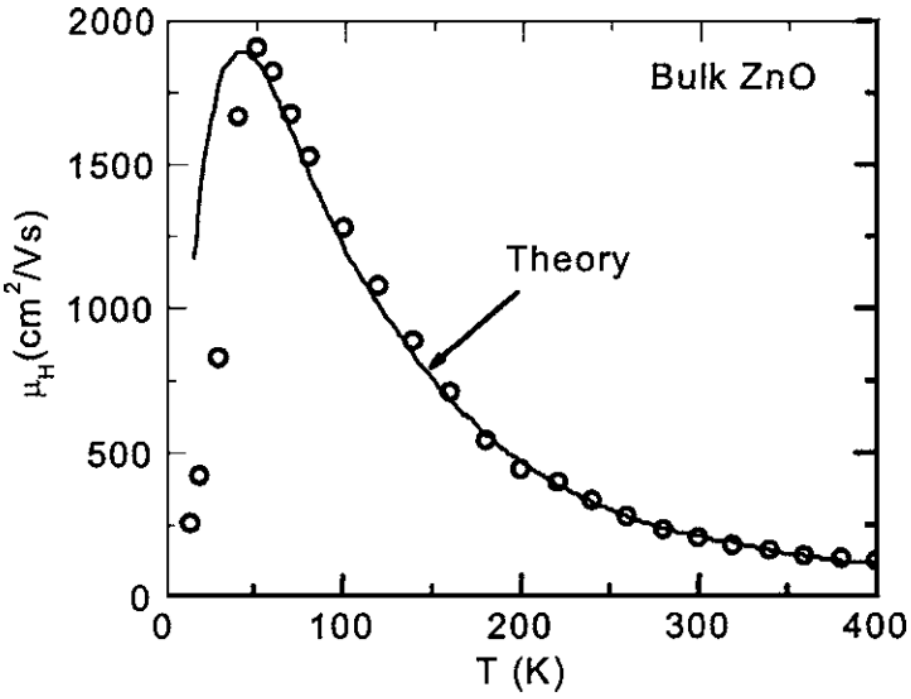

Figure 1.5: The relationship between the electron mobility and temperature for high-quality bulk ZnO. Reproduced from [21]

In comparison to bulk values, reported mobilities for ZnO nanostructures are typically below 100 cm^2 V^{-1} s^{-1}, although particularly high-quality samples can sometimes show mobilities in the range of 1000+ cm^2 V^{-1} s^{-1} at room temperature [35, 36, 37, 15]. However, these are typically regarded as anomalous, and some authors have questioned these results [38]. The majority of hydrothermally-synthesised devices have mobilities under 50 cm^2 V^{-1} s^{-1}; these results are reviewed and summarised in Chapter 3.

ZnO generally has a lower mobility than GaN due to its higher effective electron mass and larger optical phonon scattering parameter [13]. However, ZnO has been predicted to have a higher saturation velocity than GaN under high-field conditions. Albrecht et al. [32] theorised that the saturation velocity for bulk ZnO would be 3.2×10^7 cm s^{-1} at 270 kV cm^{-1}. The predicted high-field drift velocities of ZnO and GaN as functions of temperature are shown in Figure 1.6. These results suggest that ZnO could outclass GaN in high-field conditions, which is extremely useful for high speed devices. Further theoretical publications have reinforced these claims, with predicted saturation velocities on the order of 1.5 - 2.2 $\times 10^7$ cm s^{-1} [33, 34]. Although there is comparatively little experimental research on high-field transport in ZnO, there are reports of saturation velocities on the order of 7.6×10^6 cm s^{-1} [39].

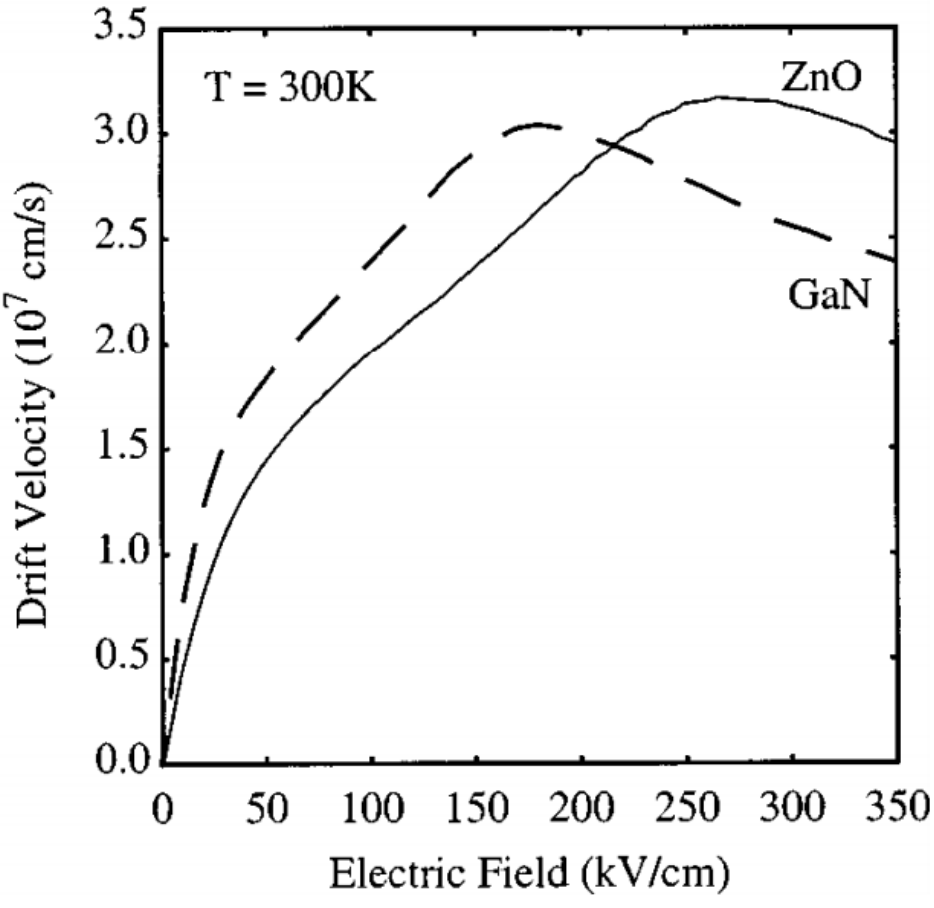

Figure 1.6: Monte Carlo simulations of the drift velocities of ZnO and GaN in high-field conditions. ZnO has a higher saturation velocity than GaN. Reproduced from [32]

1.3 Thesis outline

This thesis consists of 9 chapters, with 4 results chapters devoted to three distinct research topics - namely, the hydrothermal growth of vertical nanowires, the hydrothermal growth of lateral arrays of nanowires used as FETs *in situ*, and the use of individual ZnO nanowires as FETs.

Chapter 2 describes the hydrothermal growth of ZnO nanowires. The current literature is discussed and referenced to explain the growth mechanisms and kinetics of ZnO nanowires. Homogeneous precipitation of ZnO is considered, and the heterogeneous nucleation from seeded substrates is discussed. These seeded substrates are used in the ensuing vertical and lateral growth chapters.

Chapter 3 reviews the current state of hydrothermally-synthesized ZnO nanowires in FET applications. The chapter begins with the fundamental theory behind FETs, and the relevant metrics and device parameters used to determine their quality. A review of the literature featuring hydrothermally-synthesized FETs then follows, with both single-nanowire and multi-nanowire devices discussed. The need for high-temperature annealing to achieve field dependence in both hydrothermal FETs and VPT FETs is also discussed. Theoretical papers predicting the expulsion of electron donors under high temperatures are considered in the context of field dependence and annealing.

Chapter 4 discusses the experimental methods used throughout this thesis. Topics include the fabrication of substrates for vertical and lateral nanowire growth and the electrical measurements of FETs.

Chapter 5 deals with the hydrothermal growth of vertical ZnO nanowires from thin films of ZnO. The impact of the molecular weight and concentration of polyethylenimine (PEI) (a typical additive in the hydrothermal growth) is explored and discussed. Vertical hierarchical nanowires are synthesised, which are caused by a PEI-mediated secondary growth phase driven by the release of Zn^{2+} ions through the Mannich reaction.

Chapter 6 presents FETs fabricated using lateral arrays of hierarchical nanowires which show field dependency without the need for any post-growth anneal or processing. The PEI-mediated hierarchical synthesis of ZnO nanowires is applied to lateral substrates, which works successfully. The growth mechanism of these hierarchical nanowires is related back to the hierarchical growth mechanism of vertical

nanowires presented in Chapter 5. FETs are fabricated by growing intersecting networks of the hierarchical nanowires, and all of the devices show field dependence. Persistent photoconductivity measurements indicate that the threshold voltage is strongly affected by the presence of the surface states, although they do not exclusively cause the observed field dependence of the nanowires.

Chapter 7 presents the modular two-pot synthesis of lateral arrays of hierarchical nanowires, and their use in FETs. The PEI-mediated growth technique of Chapter 6 is separated into two separate modular hydrothermal growths, and lateral hierarchical nanowires are successfully synthesised. The growth parameters of the two modular hydrothermal growths are investigated to optimise the yield of the hierarchical nanowires. Intersecting networks of the hierarchical nanowires are used as FETs. Dry measurements of the FETs are presented, which show limited intrinsic field dependence when used in air. Devices which are not field dependent as-is are wet-measured in de-ionised H_2O, and field dependence is achieved using back and top gates.

Chapter 8 presents the contacting of individual ZnO nanowires using electron beam lithography. Annealed and unannealed vertical nanowires are contacted in 3 total batches. All of the contacted nanowires show back-to-back Schottky contacts, which are modelled and fitted. The change in the Schottky contacts with exposure to UV light is investigated. The contacted nanowires show limited use as FETs, although two separate devices are fabricated. The nanowires show a drastic transition from conducting to insulating over 48 hours after liftoff. This transition can be temporarily reversed by exposing the nanowires to an electron beam. The nanowires disappear over a period of 8 months, most likely due to an interaction with the atmosphere. Accumulation of acidic carbon is considered.

Finally, **Chapter 9** is the conclusion of the thesis, summarising the work and laying ground for future research.

Chapter 2

Hydrothermal growth

2.1 Introduction

ZnO readily forms into a wide range of nanostructures due to the strong polarity of its crystal structure [18]. There are several different ways to synthesize these nanostructures, although most techniques can be broadly categorised into either vapour phase transport (VPT) techniques, or hydrothermal techniques [40]. This chapter focuses on the hydrothermal technique, as the hydrothermal growth is exclusively used throughout this thesis to synthesize ZnO nanowires. The chemistry of the hydrothermal growth is described in detail, along with some of the points of contention which still remain today. The growth of ZnO nanostructures is also described, and how homogeneous and heterogeneous nucleation affects the final product. Finally, nanowire growth from seeded substrates is discussed, which underpins the synthesis of the devices presented in this thesis.

2.2 Vapour phase transport

Vapour phase transport (VPT) synthesis techniques involve vaporised precursors which condense into ZnO nanowires. All of these techniques take place at high temperatures, and utilise expensive equipment. The most common VPT synthesis route is chemical vapour deposition (CVD). There are many variations of CVD procedures, including thermal evaporation [41], metal-organic [42], and carbon thermal reduction [43] amongst others. Despite the wide variation of procedures, most CVD techniques work on similar principles. The choice of substrate for CVD growth methods determines whether growth is possible at all, and if so what orientation the nanowires will take with respect to the substrate. Well-aligned vertical growth is achieved by exploiting lattice mismatches between the substrate and the ZnO nanowires, and has been demonstrated for a number of epitaxial substrates including both a-plane and

c-plane sapphire [44], Si [45], GaN and SiC [46], amongst others [38].

The necessity to exploit lattice mismatches between ZnO and the growth substrate, coupled with the high temperatures throughout the growth, greatly reduces the number of substrates that are compatible with VPT, and discourages direct growth onto device substrates or technologically relevant substrates. This thesis focuses on the hydrothermal method, which offers far greater flexibility due to its low cost and comparatively low temperature.

2.3 Hydrothermal methods

2.3.1 Introduction

The hydrothermal technique is one of the common methods of synthesizing ZnO nanostructures [10], including ZnO nanowires. The hydrothermal method is based on the hydrolysis of metal salts. Hydrothermal synthesis of ZnO nanowires takes place in water, with the precursors dissolved in the solution [40]. At least two precursors are typically used, with one precursor providing the zinc salt to be hydrolysed, and the other precursor providing the hydroxyl ions.

The hydrothermal synthesis of ZnO micro/nanostructures was first reported by Andre-Vergas et al. in 1990 [47], although the significance of this new synthesis method was somewhat overlooked. The authors synthesized ZnO microcrystals from aqueous solutions by combining zinc chlorides and zinc nitrates with hexamethylenetetramine (HMT). They investigated how the different variables of the synthesis process affected the reaction products, such as the temperature, the pH, the precursor concentrations, and the particular type of zinc salt used. This publication was eventually followed by Vayssieres in 2003, who hydrothermally synthesized ZnO nanowires on seeded substrates by mixing zinc nitrate hexahydrate with HMT in aqueous solution [48]. This publication was very well received, and the technique has since become the *de facto* standard for hydrothermal synthesis. Some of the ZnO microstructures and nanowires synthesized by Vayssieres and Andre-Verges et al. are displayed in Figure 2.1(a) and (b), respectively.

Although ZnO nanowires can be precipitated directly from the hydrothermal solution, they are typically grown on seeded substrates which are immersed within the solution. The growth solution is heated in a sealed vessel to relatively low temperatures (usually between 90 to 130 °C) at atmospheric pressure. This only requires a small amount of inexpensive and rudimentary equipment, such as a water bath or convection oven, making it very easy to scale up the hydrothermal synthesis of ZnO

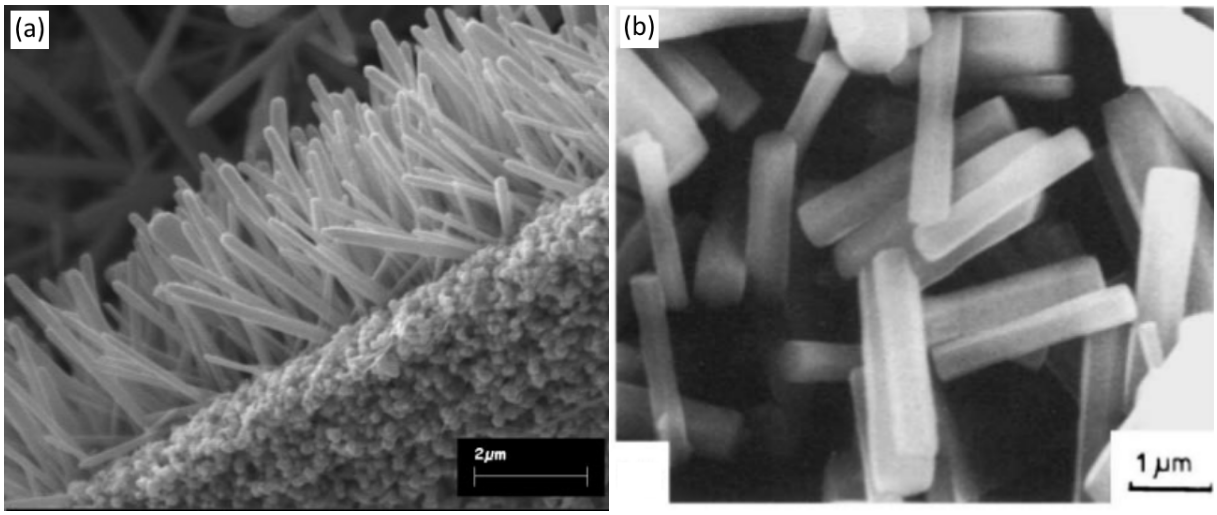

Figure 2.1: ZnO nanowires hydrothermally grown via $Zn(NO_3)_2$ by (a) Vayssieres and (b) Verges. Adapted from references [48] and [47] respectively.

nanowires. In comparison, the expensive vacuum equipment and very high temperatures necessary for VPT synthesis make scaling expensive and difficult. The very low temperatures involved in the hydrothermal synthesis also makes the technique compatible with many vulnerable substrates, such as transparent and flexible materials, which are incompatible with high-temperature VPT methods.

2.3.2 Hydrothermal synthesis equipment and method

The simple hydrothermal set-up used throughout this thesis is displayed schematically in Figure 2.2. Individual 250 mL Schott bottles are filled with hydrothermal growth solution and were submerged in a Grant JBN12 water bath to raise their temperature to 95°C. The bottles can be left to pre-heat if necessary, before substrates are introduced into the growth solution. This allows the initial hydrothermal reactions to take place in the absence of a solid seed layer, restricting the ZnO growth to homogeneous nucleation. This can have a strong effect on the morphology of the final ZnO nanowires.

Seeded substrates are affixed to glass microscope slides using Kapton tape, and the slides are placed inside of the Schott bottles. Each slide can have multiple seeded substrates attached to it. Care must be taken to place the glass slides in the bottle so that the seeded substrates point ”down”, to ensure that homogeneously nucleated ZnO which precipitates out of solution doesn’t fall on the surface of the substrates (indicated in Figure 2.2(b)). After the hydrothermal growth is complete, the slides are removed from the Schott bottles and placed in de-ionised H_2O. The substrates are then removed from the glass slides, individually rinsed in clean de-ionised H_2O, and

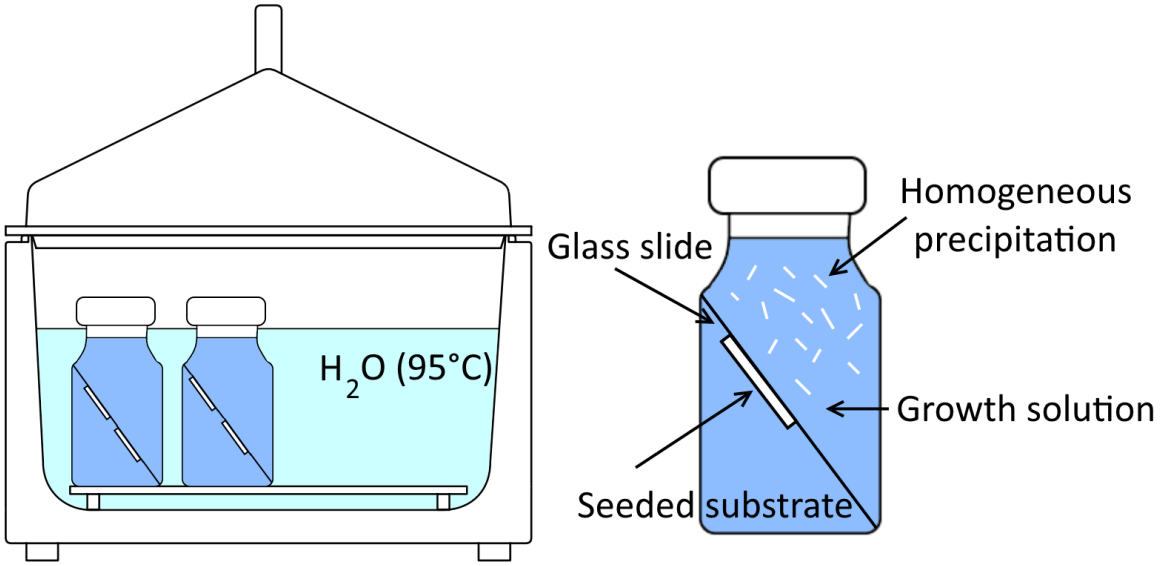

Figure 2.2: A simple schematic showing the equipment used to hydrothermally grow nanowires throughout this thesis.

dried with nitrogen at room temperature. The exact parameters and recipes of the hydrothermal growths used throughout this thesis are given in their relevant chapters.

2.4 Chemistry of the hydrothermal growth

As stated previously, the most common precursors used in the hydrothermal growth are zinc nitrate hexahydrate [$Zn(NO_3)_2$] and hexamethylenetetramine (HMT) [$(CH_2)_6N_4$]. These precursors are dissolved using de-ionised H_2O as the solution. The $Zn(NO_3)_2$ provides Zn^{2+} ions, while the HMT provides the hydroxyl ions necessary for crystallisation of ZnO. The crystallisation of ZnO out of solution can be understood by the following reactions [10]:

$$(CH_2)_6N_4 + 6H_2O \longrightarrow 6HCHO + 4NH_3 \tag{2.1}$$

$$Zn(NO_3)_2 \longrightarrow Zn^{2+} + 2NO_3^- \tag{2.2}$$

$$NH_3 + H_2O \longleftrightarrow NH_4^+ + HO^- \tag{2.3}$$

$$Zn^{2+} + 2HO^- \longrightarrow ZnO + H_2O \tag{2.4}$$

$$Zn^{2+} + 2HO^- \longleftrightarrow Zn(OH)_2 \tag{2.5}$$

$$Zn(OH)_2 \longleftrightarrow ZnO + H_2O \tag{2.6}$$

HMT is highly soluble in water due to the inherent strain energy caused by its molecular structure [49], and readily hydrolyses into ammonia ($4NH_3$) and formaldehyde (HCHO) (as per Equation 2.1). Zinc nitrate hexahydrate is also very soluble and

rapidly decomposes, providing Zn^{2+} ions (Equation 2.2). The ammonia molecules produced by the decomposition of HMT lower the pH and react with the water to produce hydroxyl ions, as per Equation 2.3 [10]. These hydroxyl ions can combine with the free Zn^{2+} ions, directly crystallising out into ZnO (shown in Equation 2.4). ZnO can also crystallise indirectly through intermediate phases. The hydroxyl ions produced by the decomposition of HMT can complex with the Zn^{2+} ions to form $Zn(OH)_2$, shown in Equation 2.5 [10]. ZnO is finally derived by dehydrating the $Zn(OH)_2$, as per Equation 2.6. Dehydration of $Zn(OH)_2$ does not occur rapidly at room temperature, and requires a relatively small increase from room temperature. All of these reactions occur at a very small rate at room temperature, so the temperature of the growth solution has to be raised (or the concentration of the precursors increased) to thermodynamically increase the rate of reaction [10]. If the temperature of the growth solution is too low, ZnO nanowires will fail to crystallise out of solution. Increasing the temperature of the growth solution typically causes longer nanowires with higher aspect ratios and smaller diameters. This is due to an increased rate of reaction between the chemical precursors, and increased mobilities and diffusion lengths for the Zn and O ions in solution [10].

The chemical equations shown above only describe a somewhat simplified version of what really occurs. Many intermediary complexes can be formed through the combination of hydroxyl ions and zinc ions, forming complexes such as $[Zn(OH)]^+$ and $[Zn(OH)_4]^{2-}$ [50, 51]. These intermediaries undergo further reactions during the growth, and do eventually dehydrate in a similar way to $Zn(OH)_2$, although it isn't known how these intermediaries affect the hydrothermal growth. Some of these complexes can form very large molecules, such as $[Zn_{57}O_{27}(OH)_{56}]^{4+}$ [52]. In addition to possibly affecting the chemical reactions leading to ZnO nanowire growth, these large complexes may dehydrate over longer periods of time than smaller complexes, which may affect the rate of nanowire growth, or even act as a second, delayed period of nanowire growth.

2.4.1 Role of HMT

The role of the HMT is more complex than shown here, and its exact role in the growth chemistry is still under debate [53, 54, 55, 56, 57, 58]. Not only does the decomposition of HMT provide the hydroxyl ions necessary for the crystallisation of ZnO, the ammonia which is produced stabilises the Zn^{2+} ions as per Equation 2.7:

$$Zn^{2+} + 4NH_3 \longleftrightarrow [Zn(NH_3)_4]^{2+} \tag{2.7}$$

Free Zn^{2+} ions in the growth solution are consumed over the course of the reaction, crystallising directly or indirectly into ZnO. Similarly, the zinc-ammonia complex

shown in Equation 2.7 gradually decomposes over time in response, causing a stable concentration of Zn^{2+} in the growth solution and a relatively low level of supersaturation. This low level of supersaturation preferentially encourages heterogeneous crystal growth on the seeded substrates and discourages homogeneous crystal growth in the bulk of the solution, which yields longer ZnO nanowires on the seeded substrates [56, 59, 60, 61].

In addition to regulating the concentration of Zn^{2+} ions in the solution, the decomposition of HMT causes a controlled and sustained release of hydroxyl ions. The rate of HMT decomposition and hydroxyl production is determined by the pH of the solution, with an increased rate of production at low pH values, and a decreased rate of production at high pH values. This effectively buffers the pH of the solution and regulates the decomposition of HMT, ensuring the gradual and sustained release of hydroxyl ions [10, 49]. This effective bottleneck on the supply of hydroxyl ions has a very important effect on the nanowire growth, as a continual source of hydroxyl ions is necessary for nanowires with high aspect ratios. If the HMT decomposed very rapidly, the excessive OH^- ions would quickly precipitate the Zn^{2+} ions out of solution, exhausting all of the precursors over a very short period of time and making ZnO nanowire growth impossible [10, 49].

Several groups and publications have looked into the possibility that HMT binds to the non-polar side faces of wurtzite ZnO, encouraging anisotropic growth along the c-axis of the nanowire. The first of these publications argued from a phenomenological approach, observing that nanowire growth was restricted almost exclusively to the c-axis without a corresponding increase in the radius of the nanowire [56]. It was argued that HMT, as a non-polar chelating agent, was binding to the non-polar faces of the ZnO nanowires, encouraging further precursors to exclusively attach to the uncapped polar c-axis face. This possibility was specifically investigated in a separate publication using attenuated total reflection Fourier transform infra-red (ATR-FTIR) spectroscopy to gauge the molecules adsorped to the faces of hydrothermally synthesized ZnO nanoparticles[57]. They concluded that there was no presence of HMT on the surface of the nanoparticles, and that HMT merely acted as a source of hydroxyl ions. This was supported by growing nanowires in an aqueous mixture using $Zn(NO_3)_2$ as the zinc ion source, and a non-HMT pH buffer and KOH to maintain HMT-esque pH conditions.

This was followed by a further publication which explicitly investigated the role of HMT in the hydrothermal growth [58]. The authors hydrothermally grew ZnO nanowires using a wide range of $Zn(NO_3)_2$:HMT ratios and recorded how the diam-

eter and length of the nanowires varied. They concluded that the HMT has a direct influence on the axial growth of the nanowires, significantly reducing their diameter while also increasing their length. These observations were supported by Raman spectroscopy, which was used to gauge the presence of molecules on the surface by looking at stretching O-H and N-H modes. These measurements suggested that complicated physio-chemical interactions between the HMT and ZnO sidewalls occur during the hydrothermal growth. The role of HMT was further complicated by its interaction with the seeded growth substrate itself, which significantly affected the nucleation and overall density of ZnO nanowires from the seeds. These findings were also corroborated by another recently published paper, which reported the shape of ZnO nanowire cross-sections changing from a hexagon to a rounded cylinder with increasing HMT [62]. This effect may be caused by the preferential attachment of HMT to the side faces of the nanowire, as similar results have been observed with other capping agents (discussed in the next section.)

There are several other variables and factors which have been reported to affect the hydrothermal growth which aren't adequately understood or accounted for in the current model. For example, although the zinc salt is usually considered as solely providing the Zn^{2+} ions necessary for ZnO growth, there is evidence which suggests the counter-ions have a significant effect on the morphology of the grown nanowires. At least six different zinc salts have been investigated, with the resulting ZnO nanocrystals being star-shaped, flower-like, rod-like, or needle-like depending on the specific salt used [63]. Similarly, oxygen dissolved in the aqueous solution isn't considered in the common models for hydrothermal growth, and there is evidence that it may have a strong effect on the hydrothermal growth [10].

The various known and unknown factors that affect the hydrothermal growth can have a negative and frustrating impact on the reproducibility of the nanowires. Sometimes drastic measures are taken, with at least one recorded instance of ZnO nanowires being grown only strictly during the weekends and evenings, to reduce any possible impact of a populated building on the experiments' reproducibility [64]. In summary, the exact mechanism of HMT-mediated ZnO nanowire growth is clearly still a point of contention, and numerous experimental results run contrary to the relatively simple chemical equations which in theory govern the hydrothermal growth.

2.4.2 Polyethylenimine as a growth additive

Growth additives can be included with the regular $Zn(NO_3)_2$ and HMT precursors in the growth solution to affect the morphology of the ZnO nanowires. These typically work by selectively binding to specific faces of the ZnO crystal during the hydrothermal growth, prohibiting further growth in that direction. The binding of the additive to the nanowire face is usually mediated through electrostatic forces, which are either attracted to the polar (c-axis) or non-polar (side faces) of the ZnO nanowire [10]. Additives which bind to the polar face of the nanowire (such as citrate ions [65, 66, 67]) encourage growth in the radial direction, giving rise to low aspect-ratio nanowires or nanocrystals. In comparison, additives which bind to the side faces of the nanowire encourage growth in the c-axis direction, increasing the aspect ratio of the nanowires. The latter is preferable for many applications, and aspect-ratio enhancing additives have been widely studied and used throughout the literature [68, 69, 70, 71, 72, 73, 74]. The capping of polar and non-polar faces of ZnO nanowires is schematically depicted in Figure 2.3, and their influence on the morphology of the nanowire.

One of the most widely used additives to increase the aspect ratio of ZnO nanowires is polyethylenimine (PEI), and is used extensively in this thesis. PEI is a repeating non-polar polymer consisting of primary, secondary, and/or tertiary amine groups in a linear or branched arrangement. A schematic of a repeating PEI molecule is shown in Figure 2.4. It was initially argued that PEI increases the aspect ratio of the nanowires by binding to the side faces of the ZnO nanowire during growth, due to the affinity of the amine groups to the non-polar crystal faces in a basic environment [68]. However, it has been shown that the role of PEI in the hydrothermal growth is significantly more complicated than this, and has an effect on the fundamental chemical reactions which drive the hydrothermal growth [75].

PEI strongly chelates with Zn^{2+} ions in the growth solution [75] by forming NH_2-Zn complexes with the terminating amines of the PEI molecules. This introduces an alternative reaction pathway for the Zn^{2+} ions, which competes with and suppresses the homogeneous precipitation of ZnO out of solution. This also lowers the concentration of Zn^{2+} ions at any given time, which has an effect on the heterogeneous nucleation of ZnO. This interaction between PEI and the Zn^{2+} ions is expressed by Equation 2.8:

$$Zn^{2+} + \text{PEI-NH}_2 \longrightarrow \text{PEI-NH}_2\text{-}Zn^{2+} \tag{2.8}$$

Critically, the Zn^{2+} ions complexed with PEI can be released back into the growth solution after some time, providing more reagents for inhomogeneous nucleation and nanowire growth. This release of Zn^{2+} ions from the PEI-Zn complexes is caused by the Mannich reaction. The Mannich reaction is defined generally as the amino alkylation of an acidic proton situated beside a carbonyl functional group, mediated

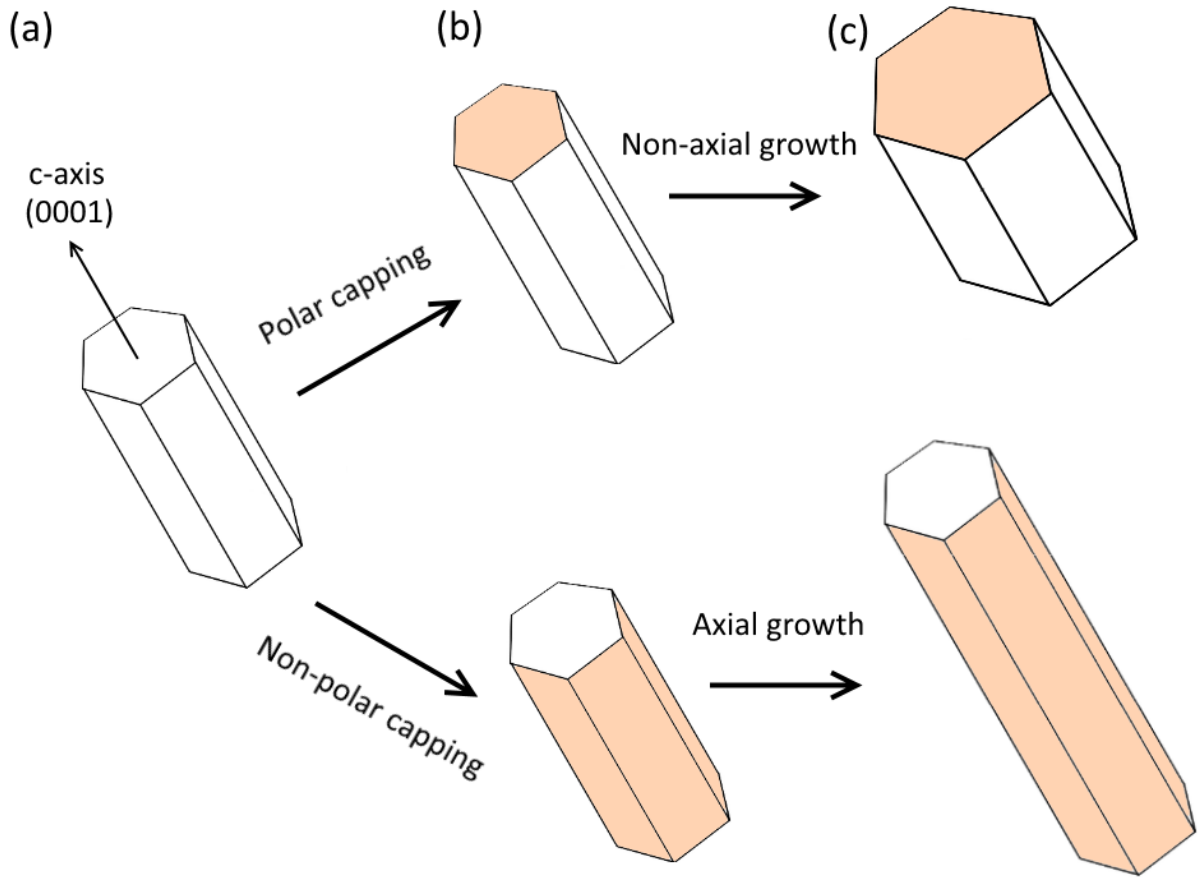

Figure 2.3: (a) A ZnO nanowire, with the polar c-axis highlighted. (b) Polar and non-polar capping agents bind to specific faces of the ZnO nanowire, depending on the electrostatic interaction between the crystal and the capping agent. (c) Polar capping agents encourage non-axial growth, while non-polar capping agents encourage axial growth.

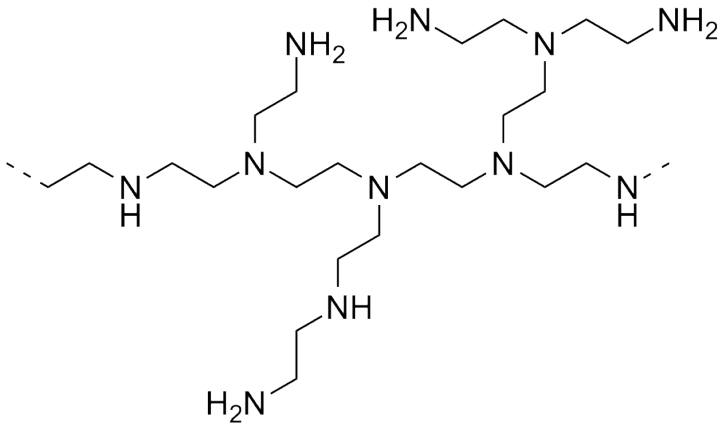

Figure 2.4: A schematic of a branched PEI molecule, showing the linear chain and branching amine groups. Figure adapted from [76]

through formaldehyde and a primary or secondary amine or ammonia. The chemistry involved in the generalised Mannich reaction lies beyond the scope of this thesis, and is considered here only in the framework of the hydrothermal growth of ZnO nanowires.

In this context, the Mannich reaction occurs between formaldehyde (HCHO) and the primary or secondary amines which terminate from branched PEI. The reaction between HCHO and the primary NH_2 amines is shown in Figure 2.5. The HCHO first interacts with the secondary amines, shown in Figure 2.5(a), forming the complex shown in (b). This complex then dehydrates into an imine group ($N{=}CH_2$), forming what is known as a Schiff base. Replacing the NH_2 amines with imine groups significantly reduces the chelating ability of PEI, releasing chelated Zn^{2+} ions back into the growth solution. This interaction is shown in Equation 2.9:

$$\text{PEI-NH}_2\text{-Zn}^{2+} + \text{HCHO} \longrightarrow \text{Zn}^{2+} + \text{PEI-N=CH}_2 \tag{2.9}$$

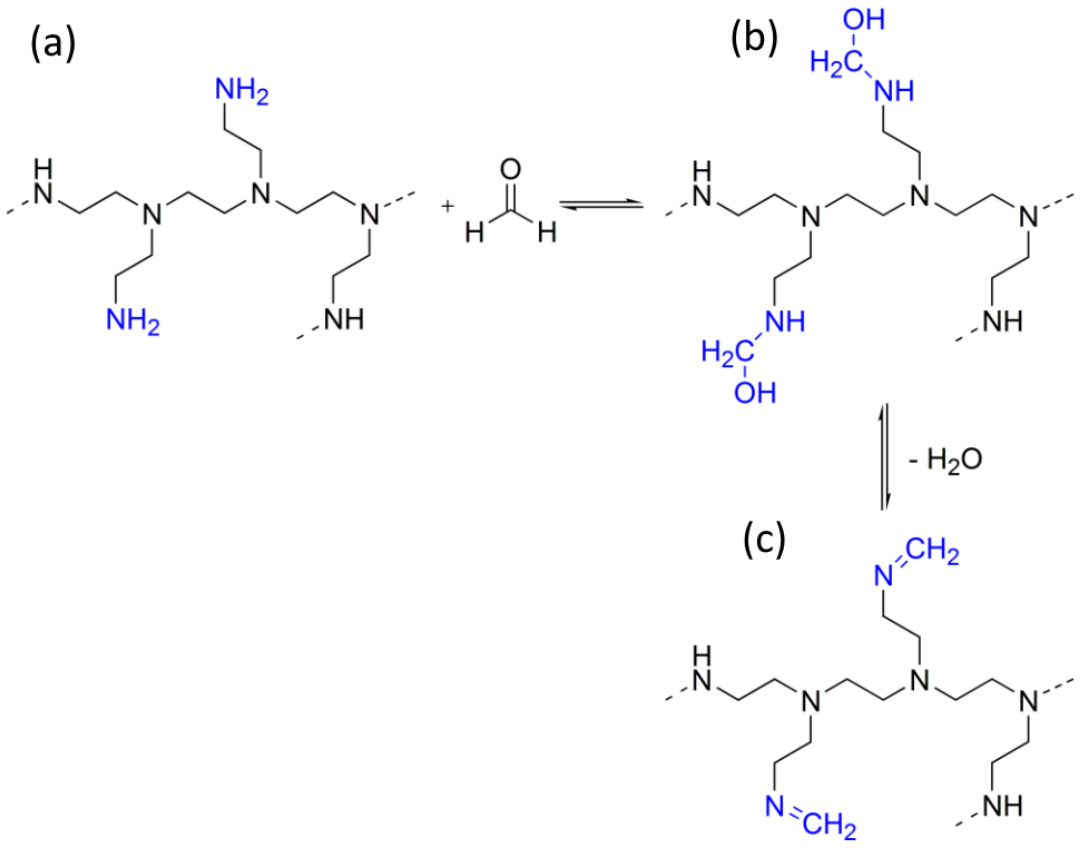

Figure 2.5: The Mannich reaction between NH_2 and HCHO. (a) Branched NH_2 interacts with HCHO, which forms an intermediary complex shown in (b). This dehydrates into the Schiff base, shown in (c). Figure reproduced from [77]

The formation of imine groups via the Mannich reaction also causes a change in colour to the growth solution. Imine groups absorb photons between 300 - 450 nm

through $\pi \rightarrow \pi*$ and n $\rightarrow \pi*$ transitions [75], which causes a yellow to orange colour in the growth solution which increases with time (an example is shown in Figure 2.7). This colour change is not observed in the hydrothermal growth solution when PEI has been omitted, which lends further evidence to the Mannich reaction taking place.

Including PEI into the hydrothermal growth solution also has further impacts on the hydrothermal growth chemistry, in addition to chelating and eventually releasing Zn^{2+} ions. PEI molecules can protonate with the NH_3 provided by the decomposition of HMT, forming NH_4^+ and a PEI-NH_3^+ complex. This in turn affects the intermediary states described by Equation 2.7. The protonation of NH_3 also provides OH^- groups into the hydrothermal growth solution, contributing to the formation of Zn complexes which in turn dehydrate into crystal ZnO. The extra production of OH^- ions through the protonation of NH_3 groups also offsets the decreased pH caused by the consumption of -NH_2 via the Mannich reaction.

The heterogeneous nucleation of ZnO through the PEI-influenced hydrothermal growth is depicted in Figure 2.6. This shows (1) the chelation between Zn^{2+} ions and PEI; (2) the protonation of the primary amine -NH_2 groups from PEI; (3) the decomposition of HMT into HCHO and NH_3; (4) the Mannich reaction between the primary amines of PEI and HCHO; (5 - 6) the heterogeneous nucleation of ZnO through the dehydration of Zn-OH complexes.

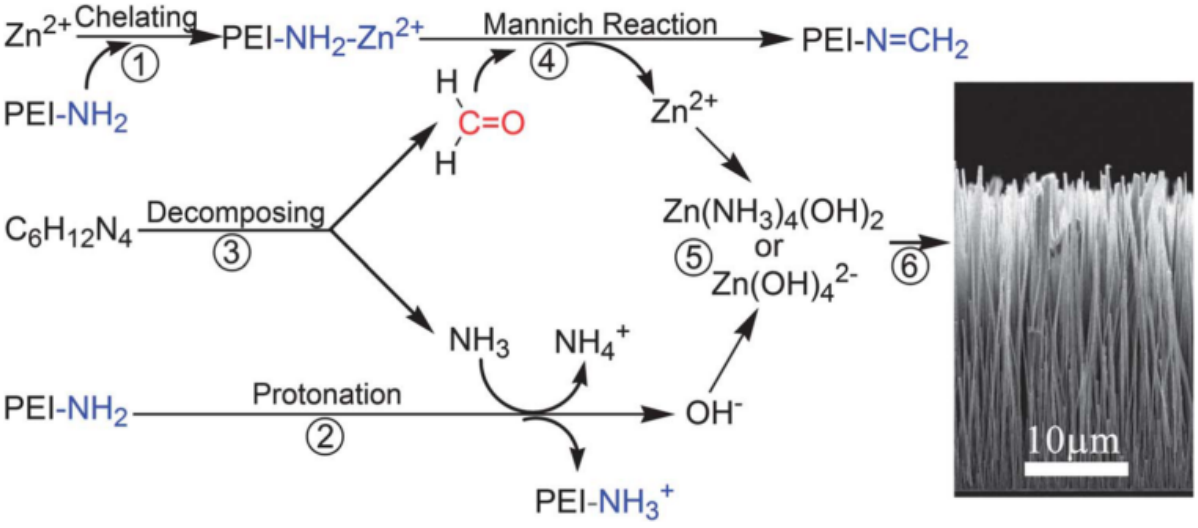

Figure 2.6: A diagram depicting the crystallisation of ZnO nanowires when PEI is included in the hydrothermal growth. Reproduced from [75]

In summary, the net effect of including PEI in the growth solution is an increase in nanowire aspect ratio and length, although the mechanism is much more complex than only encouraging growth in the c-axis direction through capping the side faces

of the nanowire. The most significant effect of PEI is the strong chelation of Zn^{2+} ions out of the growth solution, which suppresses homogeneous precipitation in much the same way as the zinc-ammonia complexes shown in Equation 2.7. These Zn^{2+} ions are introduced back into the solution over time via the Mannich reaction, supplying more precursors for nanowire growth [75].

Further evidence for this reaction is shown by the gradual yellow-orange colour change to the growth solution, caused by the conversion of primary amine to imine groups in the PEI molecules. This differs significantly from hydrothermal growths where PEI is not included, in which the HCHO produced by the decomposition of HMT does not play a role in the growth chemistry. Critically, the ability to complex and reintroduce Zn^{2+} ions into the growth solution can have a significant effect on the final nanowires, which is demonstrated in Chapters 5 and 6 of this thesis.

2.5 Hydrothermal growth of ZnO nanowires

As discussed in the introduction (Chapter 1), ZnO almost exclusively forms in the hexagonal wurtzite structure . This crystal structure has a polar c-axis which terminates in either O atoms (the (0001) face) or Zn atoms (the $(000\bar{1})$ face). The other faces of the hexagonal wurtzite crystal are non-polar, such as the side faces. Generally speaking, polar facets have a high surface energy associated with them, while the non-polar facets have a low surface energy [10]. The hydrothermal growth of a ZnO crystal is driven by minimising the energy of the thermodynamic system [10], which means that precursors will preferentially migrate to the polar face and the crystal will grow in the c-axis direction. This self-assembly and natural anisotropy of crystal growth is one of the attractive features of using ZnO as a nanostructure.

2.5.1 Homogeneous growth

Homogeneous nucleation of ZnO occurs when all of the reactants involved in the nucleation are in a solution phase [78]. Zn^{2+} ions directly react with the hydroxyl ions provided by the decomposition of HMT, and either directly crystallise into ZnO or form complexes [10]. The initial complex serves as a scaffold for further Zn^{2+} ions and hydroxyl groups to attach to, eventually incorporating the ions and forming a crystal lattice through dehydration. This occurs without any external catalyst or initial point of nucleation. The crystal continues to grow in size over time as more ions are supplied from the growth solution, preferentially interacting with the less thermodynamically stable facets of the crystal. The reliable flux of constituent ions from the solution to the crystal occurs due to the supersaturation of precursors in the

growth solution [79], and abates when the system is thermodynamically stable or when the precursors are exhausted from the solution.

Homogeneous growth of ZnO nano/microwires is typically undesirable and unintentional. The reaction products can be isolated out from the growth solution and presumably used for device applications through drop-casting methods, etc., although the products are often very large in size, and have very poor aspect ratios. The hydrothermal method is often used to synthesise nanowires in predefined locations on pre-seeded substrates, and homogeneously nucleated ZnO poses a problem for device fabrication. Firstly, ZnO nanocrystals which precipitate out of solution can fall onto the substrate surface, potentially shorting electrodes or otherwise fouling the substrate. Secondly, the precursors that are consumed through homogeneous nucleation are no longer available for heterogeneous nanowire growth. This reduces the overall length of the ZnO nanowires (by reducing the total volume of ZnO), and in the past this has necessitated refreshing the growth solution [69, 73, 80].

There are several ways to prohibit and minimise the impact of homogeneous nucleation of ZnO during the hydrothermal growth. To minimise the risk of homogeneously grown ZnO from depositing on the substrate, the substrates are typically floated face-down on the surface of the growth solution over the course of the growth, or are attached to glass slides angled downwards. To reduce the homogeneous nucleation of ZnO in the first place, the chemistry of the hydrothermal growth can be tailored to reduce the level of supersaturation in the growth solution. This can be achieved by adding NH_3 (although the decomposition of HMT naturally introduces NH_3 into the solution), or including PEI in the growth solution. These effects can be very drastic and obvious. Figure 2.7 shows a series of Schott bottles containing hydrothermal growth solution which have been allowed to pre-heat for an hour. From left to right, the bottles contain 6 mM, 8 mM, 2 mM, and 3 mM of PEI(M_W = 800 g/mol). These different concentrations have significantly affected the homogeneous precipitation within the growth solution.

The turbidity of the growth solution clearly differs between the bottles, the bottles containing 2 mM and 3 mM of PEI being almost opaque on account of the precipitation within the growth solution. In comparison, the bottles containing 8 mM and 6 mM are completely transparent, and free of any precipitation. The various shades of yellow and orange of the growth solution are caused by the complexing of PEI with HCHO via the Mannich reaction [75].

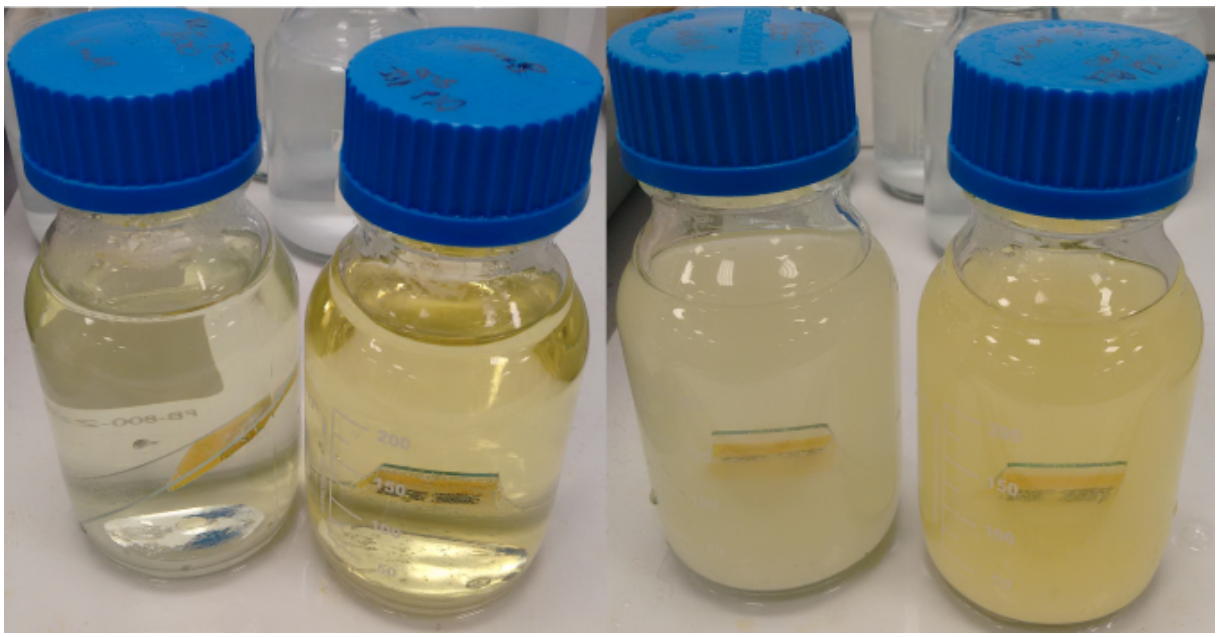

Figure 2.7: A series of bottles which have been left to preheat for one hour. From left to right, the bottles contain 6 mM, 8 mM, 2 mM, and 3 mM of PEI(M_W = 800 g/mol)

2.5.2 Heterogeneous growth

In contrast to homogeneous nucleation, heterogeneous growth occurs when the initial point of nucleation is a crystal in the solid phase, while the reactants to the growth are in the liquid phase [40]. This is usually the type of nucleation and growth exploited in the hydrothermal synthesis of ZnO, as it allows for ZnO nanowire growth directly from pre-defined crystal seeds or catalysts [59]. The crystal seeds or catalysts may be suspended in the solution, although the more common technique (and the technique used exclusively throughout this thesis) is to heterogeneously grow the nanowires from seeded substrates [59]. As the reaction takes place, ions are incorporated into the existing crystal lattice, and the crystal grows larger. The constituent ions are supplied over time in much the same way as homogeneous growth. Whether homogeneous or heterogeneous growth is favoured depends on several factors, such as the supersaturation of precursors in the solution [56, 59, 60, 61].

Different ZnO crystal seeds have been used throughout the literature, such as ZnO nanocrystallite films [81, 82] or deposited thin ZnO films [83, 84, 85, 86]. Seedless growth can also be achieved using intermediary layers like Ti/Au [87], although seeded ZnO films are the more common substrates used. Seeded growth is one of the main benefits of the hydrothermal method, as it allows the synthesis of nanowires on a wide variety of different substrates. Because the growth conditions themselves are fairly benign (e.g. below 100 °C and in a slightly basic environment), if the substrate is compatible with seed layer deposition, then it is most likely compatible with the hydrothermal growth. To this end, nanowires have been hydrothermally grown on a wide variety of interesting and relatively vulnerable substrates, such as paper [88], flexible plastics [89], carbon fibres [90], and other fabrics [91].

2.5.3 Growth from seeded substrates

Vertical growth

ZnO nanowires tend to grow normally (i.e. at a 90° angle) from thin films of ZnO used as seed layers, although the orientation of the nanowires can show some variation depending on several factors of the ZnO film [83, 84, 85, 86]. Figure 2.8 shows ZnO nanowires grown from a thin layer of Au and an RF sputtered ZnO thin film on silicon substrates. In both cases the nanowires have grown normally from the substrate and their respective seed layer, although the orientation of the nanowires is significantly better from the ZnO thin film. This results in a vertical ”forest” of ZnO nanowires, which can be isolated from the growth substrate and used for device fabrication individually. Vertical nanowire forests have also been successfully used in devices with

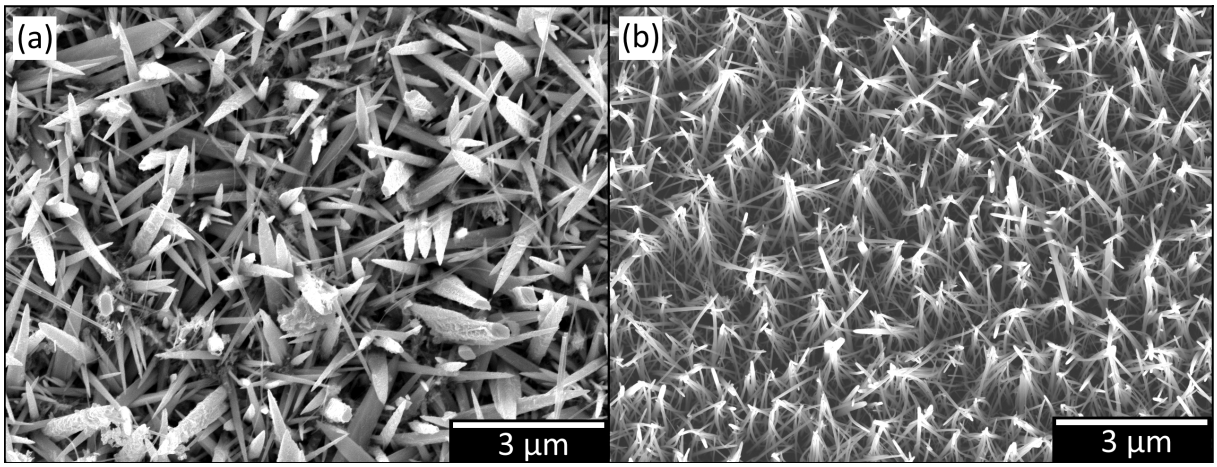

Figure 2.8: Top-down images of ZnO nanowires hydrothermally grown from thermally deposited Au (a) and RF sputtered ZnO (b) thin films.

several applications, such as power generation, lasing, and dye-sensitized solar cells [10].

Lateral growth

Hydrothermal growth from seeded substrates can also be used to grow lateral arrays of ZnO nanowires, and is one of the main advantages over VPT methods. Although it is possible to grow nanowires laterally using VPT/CVD growth [92], the results are often less than ideal, and the process is incompatible with a large number of substrates due to the high temperatures involved in the nanowire synthesis. The hydrothermal growth of lateral arrays of nanowires has been generalised to other substrates using sputtered seed layers of ZnO [93, 94, 95, 96, 97, 98]. As the nanowires grow normal to the face of the ZnO seed layer, it is necessary to fabricate a seed layer which is perpendicular to the substrate. This is most easily achieved by patterning and depositing a ZnO thin film with a capping layer. The capping layer prevents nanowire growth and nucleation from the top face of the seed, while the sidewall of the ZnO layer remains exposed to the growth solution, encouraging lateral growth. This is depicted schematically in Figure 2.9 .

Hydrothermal growth of lateral ZnO nanowires can also be achieved by combining electron beam lithography with single-crystal ZnO substrates orientated in the $(2\bar{1}10)$ direction [99]. Extremely well-ordered arrays of ZnO nanowires are able to be grown in this way, and could be transferred to flexible substrates with no loss of order to the original array. The downside to this approach is the requirement for a single-crystal ZnO substrate, textured in a single direction.

In practice, hydrothermally-grown lateral nanowires often grow in a 180° arc

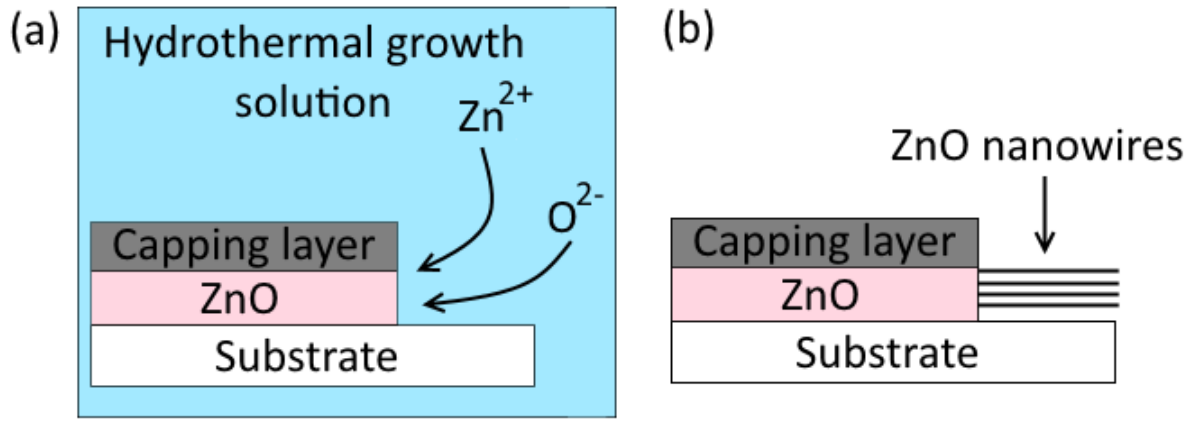

Figure 2.9: (a) A seeded substrate with a capped thin film of ZnO is submerged in hydrothermal growth solution. Zn^{2+} and O^{2-} ions nucleate on the sidewall of the thin film, which is exposed to the growth solution. (b) After growth, nanowires grow laterally from the sidewall.

from the seed layer. As the ZnO nucleates and grows at the seed layer sidewall, the crystal agglomerates into a large nucleus, partially delaminating the seed layer from the substrate. ZnO nanowires then grow from this nucleus and the underside of the seed layer, which causes the wide-angle brush orientation of the nanowires. Figure 2.10 shows a lateral array of ZnO nanowires. Figure 2.10(a) shows the lateral array from a bird's eye view. The SiO_2 substrate and capping layer have been labelled. ZnO nanowires are laterally growing from the exposed sidewalls of the ZnO seed, although they are clearly growing in a wide arc rather than purely flush to the substrate. Figure 2.10(b) shows a cross-section of the lateral array marked by the dashed box in (a). It is clear that the capping layer is preventing vertical nanowire growth, and that the ZnO seed layer has partially delaminated from the substrate. This partial delamination has caused the nanowires to grow in a 180° arc from the sidewall. This arc is shown in cross-section in the upper-right inset.

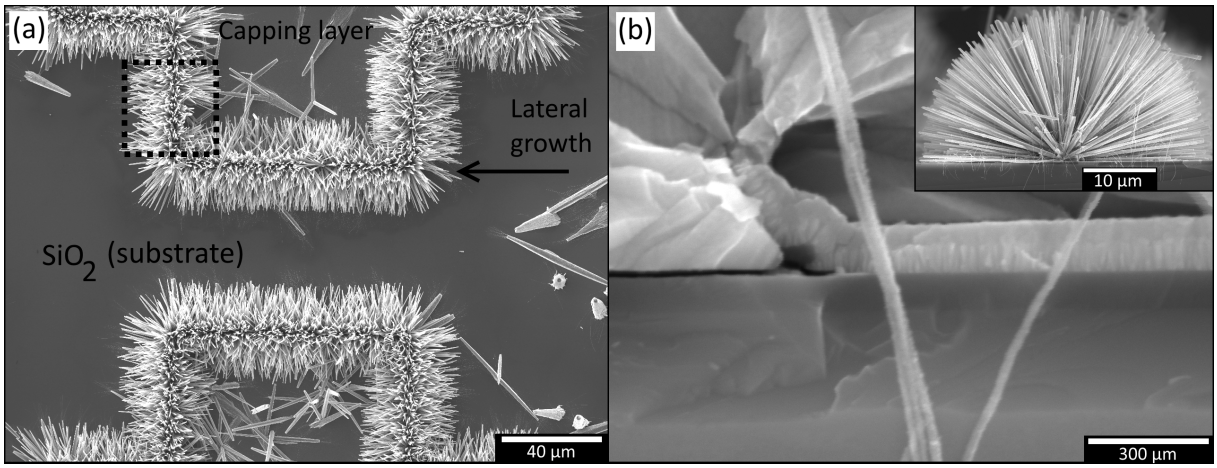

Figure 2.10: (a) A bird's eye view of a lateral array of ZnO nanowires. The capping layer has prevented vertical growth. The dashed box is shown in cross-section in (b). The seed layer has partially delaminated from the SiO_2 substrate, allowing the nanowires to grow in an arc. The large arc is shown in cross-section in the upper-right inset.

2.6 Conclusion

In conclusion, the hydrothermal growth is a powerful synthesis technique given its versatility. It can be combined with a wide variety of seeded substrates due to the low temperatures involved in the growth process. Zinc nitrate hexahydrate and HMT are the most common precursors used in the growth, although there is still some ambiguity regarding the exact growth mechanisms and chemical interactions which take place. PEI is often used as an additive, and adds another layer of complexity to the hydrothermal growth. Heterogeneous nucleation is favoured for most hydrothermal growth applications, with homogeneous nucleation intentionally suppressed.

Chapter 3

Field-effect transistors

3.1 Introduction

In this chapter, sufficient background on field-effect transistors is given to understand and contextualise the results presented in this thesis. The threshold voltage, on-off ratio, transconductance, and subthreshold swing device parameters are defined and explained. The literature regarding ZnO nanowire FETs is reviewed, with an emphasis on hydrothermally synthesised nanowires. The role of electron donors in ZnO nanowires is considered in the context of FET fabrication, and how they are addressed by high temperature annealing in the literature. The chapter concludes with a summary of the literature review, which motivates the need to reliably produce ZnO nanowire FETs which show field dependence without annealing.

3.2 FET Background

3.2.1 Mode of operation

Field-effect transistors (FETs) are a fundamental component in modern electronics, and are used in a wide variety of applications. An FET consists of a semiconducting channel, contacted by two electrodes (called the drain and source), and separated from a third electrode (the gate electrode) by an insulator. The FET can be thought of as an electronic switch, where the conductivity of the semiconducting material is modulated by applying an external electric field via a voltage difference between the gate and source electrodes. This modulation of conductivity is caused by the bending of the conduction and valence bands of the semiconductor [100]. Depending on the direction of the bending, charge carriers can be introduced or removed from the channel. This is known as the field effect.

Figure 3.1 shows a schematic of the conduction and valence bands of an n-type semiconductor as a positive voltage is applied to the gate electrode (shown to the right of the insulator.) When no gate voltage is applied, the charge carrier concentration in the semiconductor is low, as the Fermi level falls within the band gap of the material. When a positive gate voltage is applied, the conduction band of the material at the semiconductor/insulator interface is bent downwards below the Fermi level, filling those states with electrons and introducing charge carriers into the channel. This is known as an enhancement mode of operation, as a positive voltage is required to accumulate charge carriers. An alternative mode of operation is depletion mode, where the channel is populated with electrons at zero bias, and a negative bias is applied to bend the conduction band above the Fermi level.

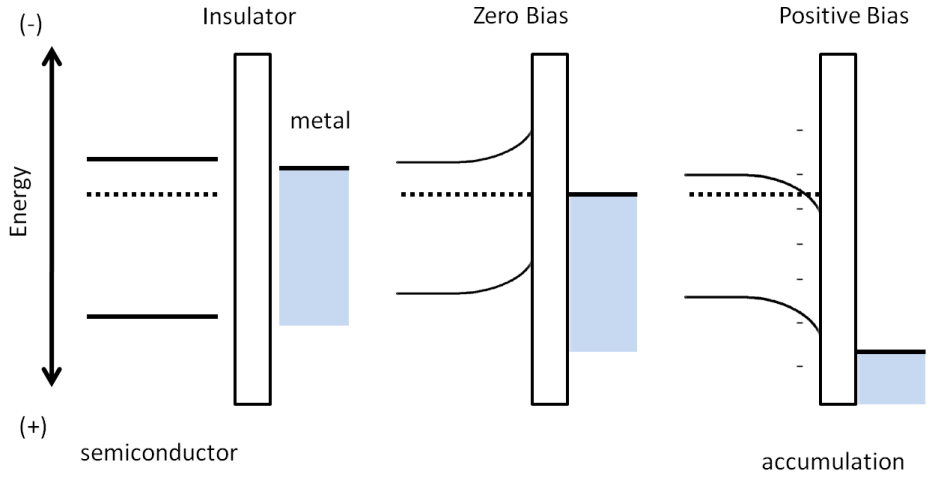

Figure 3.1: Band bending of a semiconductor via the field effect. At zero bias, the channel is depleted. At a positive bias, the conduction band is bent below the Fermi level, populating the channel with electrons. Reproduced from [101].

3.2.2 Transfer characteristics and device parameters

One of the most important measurements used to assess an FET are the transfer characteristics of the device. These are measurements of the drain-source current, I_{DS}, versus the gate-source voltage, V_G, at a fixed drain-source voltage, V_{DS}. The gate voltage can be swept in both forward and backward directions. This can sometimes result in a discrepancy in I_{DS}, which is called a hysteresis. Figure 3.2 shows the transfer measurements of a standard n-type BS20 MOSFET on a logarithmic scale. The drain-source voltage is kept at a constant value of 0.1 V. The device is clearly off when V_G is below 0 V, which is called the off regime. Similarly, the FET is clearly on once V_G is above roughly 2.5 V. The ratio of these two currents is called the **on-off ratio** of the device,

and is typically given as an order of magnitude. In this case, the on-off ratio is on the order of 10^{11}.

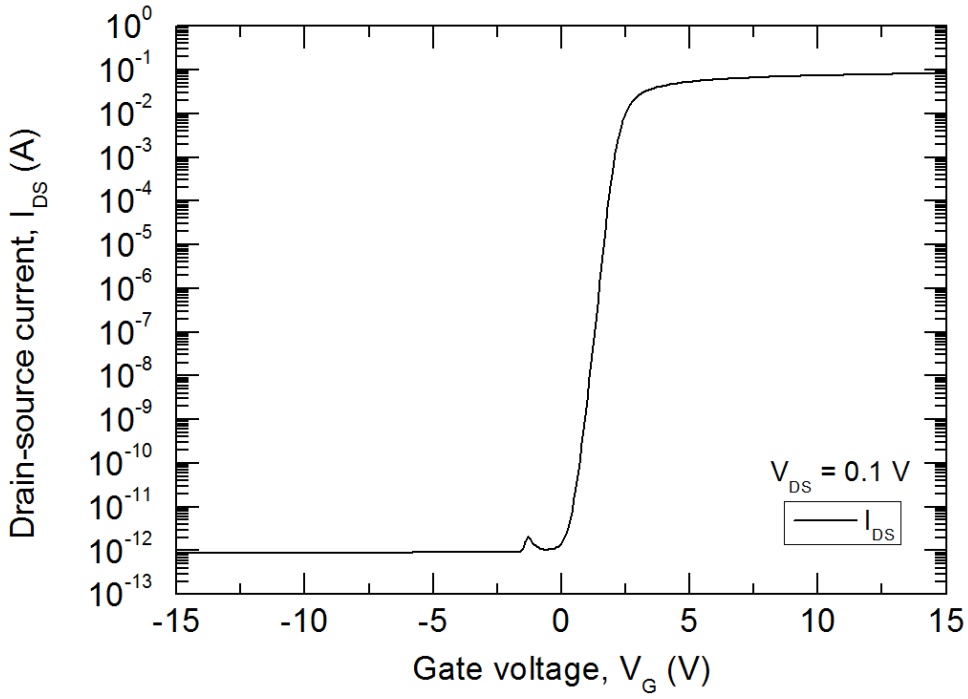

Figure 3.2: The transfer characteristics of a standard BS20 MOSFET. The device is driven at a drain-source voltage of 0.1 V

3.2.3 Threshold voltage - V_{Th}

The value of the gate voltage which turns the device on or off is called the **threshold voltage** (V_{Th}) of the device. There are many different specific definitions of the threshold voltage, and several different techniques are used to extract the threshold voltage from multiple types of measurements [102]. In this thesis, all of the threshold voltages have been extracted using the linear extrapolation method. The transfer characteristics of the FET are plotted on a linear scale, and the linear portion of the drain-source current is extrapolated to intersect with the gate voltage axis. The point of intersection is then taken to be the threshold voltage.

The sign and magnitude of the threshold voltage is affected by the charge carrier concentration of the semiconducting channel. A high charge carrier concentration means that the device operates in depletion mode, requiring a negative threshold voltage to deplete the device of electrons. Higher charge carrier concentrations necessitate lower threshold voltages to switch between on and off states. Similarly, if the charge carrier concentration of the semiconductor is low, and the device is off at V_G = 0 V, then the device operates in enhancement mode, with a positive threshold voltage

inducing electrons into the channel through Schottky band bending. Lower charge carrier concentrations require higher threshold voltages to populate the channel with electrons. The threshold voltage of the device is also affected by other aspects of the channel, such as the surface states at the semiconductor/dielectric interface [100].

Figure 3.3 shows the transfer characteristics of the FET displayed in Figure 3.2, plotted on a linear scale and restricted to V_G = 0 to 5 V. The entire transfer characteristics on a linear scale are shown in the upper-left inset. A linear line (red) is extrapolated from the linear portion of the transfer characteristics, and intersects the V_G axis at ≈2.2 V, which is taken to be the threshold voltage. This device operates in enhancement mode, as it is in the off regime at V_G = 0 V.

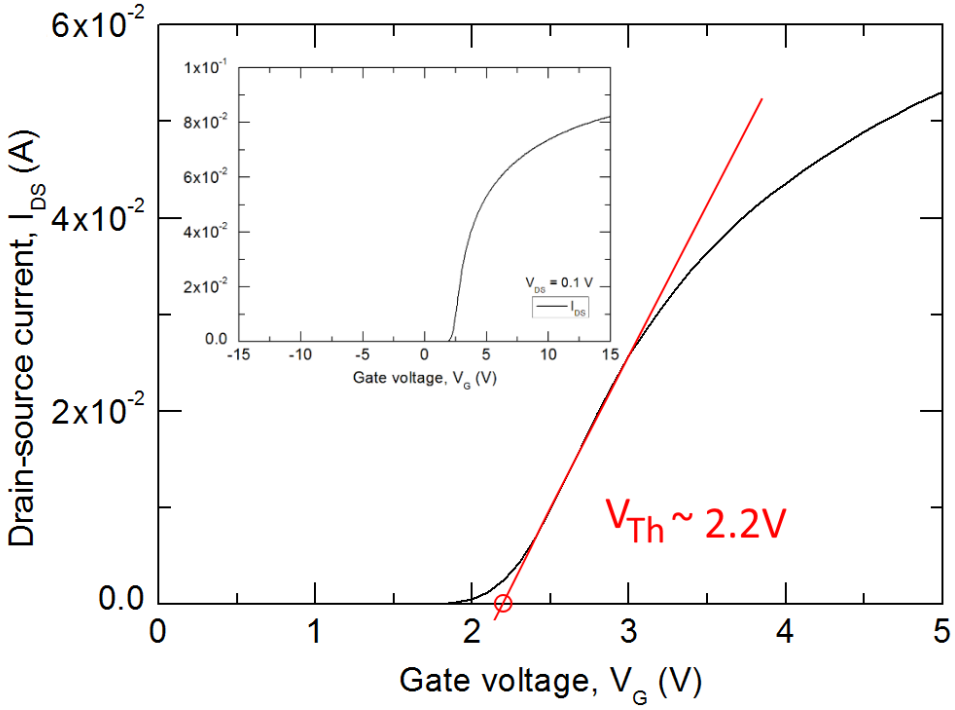

Figure 3.3: Extracting the threshold voltage of a standard BS20 MOSFET. The intercept between the linear extrapolation (red) and the V_G axis gives a threshold voltage of 2.2 V.

3.2.4 Transconductance - g_m

The transconductance of a device is defined as the change in drain-source current over a small change in gate voltage. More specifically, it is taken as the first derivative, $\frac{dI_{DS}}{dV_G}$, of the transfer curve. The transconductance is typically taken as the maximum value of the derivative. Figure 3.4 shows the transfer characteristics of Figure 3.2 plotted alongside its first derivative on a linear scale, plotted from V_G = 0 V. The maximum transconductance g_m is approximately 0.033 S.

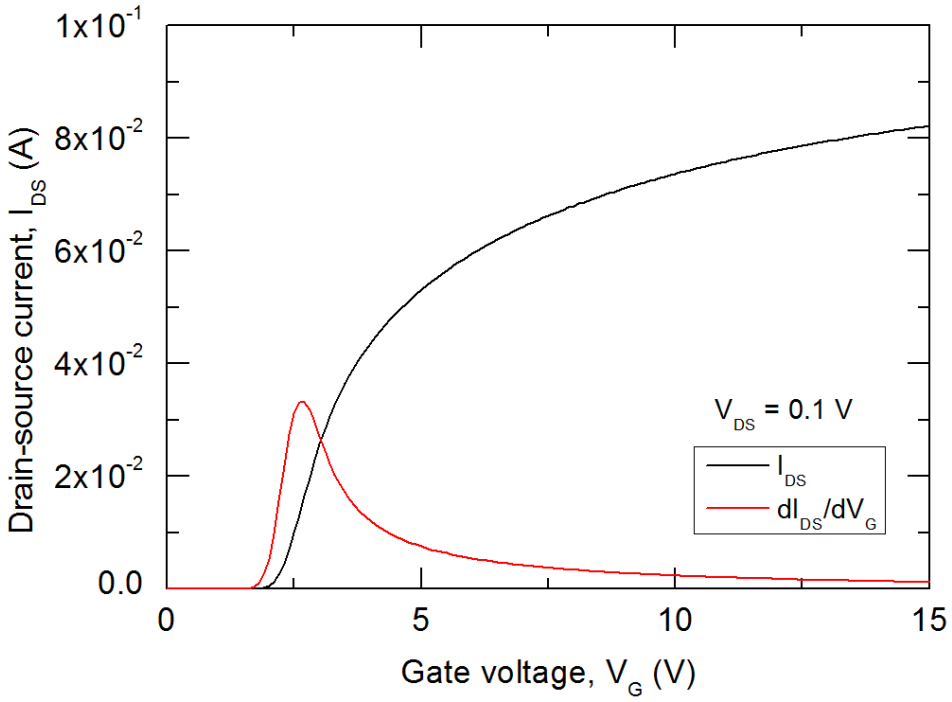

Figure 3.4: The transfer characteristics of a standard BS20 MOSFET (black) plotted against its derivative (red) in order to find the transconductance. The maximum transconductance is approximately 0.033 S.

3.2.5 Subthreshold swing - SS

The subthreshold swing of a device is a measure of how fast the FET switches from the off state to the on state. This occurs over the subthreshold regime of the transfer characteristics, which is occurs at gate voltages slightly below the threshold voltage. The logarithm is taken of the transfer characteristics, and the subthreshold swing is then the inverse of the gradient of the subthreshold regime. It is typically given in mV/decade, where a decade refers to an order of magnitude of drain-source current. Approximately 60 mV/decade is considered to be the lowest subthreshold swing theoretically achievable by typical FETs [100].

Figure 3.5 shows the subthreshold regime and subthreshold swing of the FET measured in Figure 3.2. The logarithm has been taken of the transfer characteristics, which are plotted between V_G = -0.5 V and V_G = 3.5 V. The gradient of the linear portion of the subthreshold regime has been highlighted in red. The subthreshold swing of this particular device is approximately 180 mV/decade.

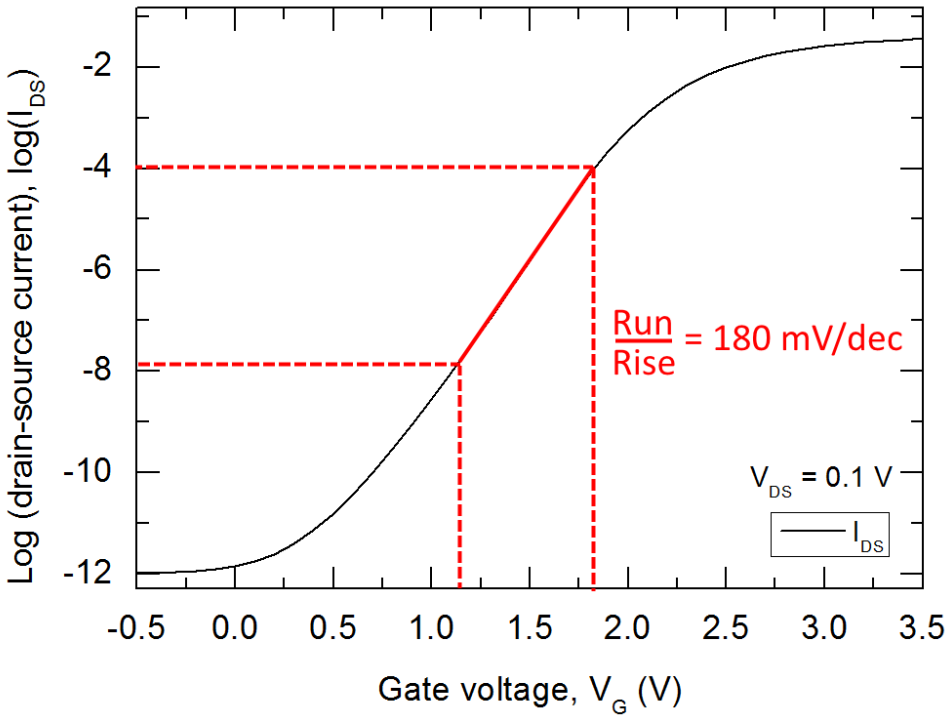

Figure 3.5: The subthreshold swing is inferred from the logarithm of the transfer characteristics. The rise and the run are highlighted in red, and the inverse of the gradient yields a subthreshold swing of ≈ 180 mV/dec.

3.2.6 Mobility - μ_{eff}

The mobility of an FET reflects how fast charge carriers can travel through the semiconducting material, and is adversely affected by electron scattering from various sources. ZnO is almost exclusively n-type, and mobility estimates are typically restricted to electrons. The mobility of an FET is typically measured by using the device in the linear region of the transfer characteristics, and is given as [103, 104, 105, 54, 106, 107]:

$$\mu = g_m \times \frac{\mathrm{L}^2}{\mathrm{V_{DS}} \times \mathrm{C}} \tag{3.1}$$

Where g_m is the transconductance of the FET, L is the length of the channel, $\mathrm{V_{DS}}$ is the drain-source voltage, and C is the capacitance of the FET. Extractions of the FET mobility therefore rely on accurately knowing the exact channel length, and calculating the capacitance of the device. Most of the devices in this thesis use lateral networks of ZnO nanowires as FETs, which makes these calculations very difficult to estimate. However, mobilities of individual nanowires are considered in Chapter 8.

3.3 Hydrothermal ZnO nanowire FETs in the literature

ZnO nanowire and nanostructured FETs synthesised by vapour phase transport (VPT) have been investigated as early as 2003 [108], while hydrothermally synthesised nanowire FETs appear as early as 2005 [109]. In general, all VPT grown ZnO NW FETs use NWs that are grown at high temperatures and then removed *en masse* from the growth substrate, prior to being randomly dispersed onto the device substrate. The hydrothermal synthesis offers the advantage of directly growing laterally aligned ZnO NWs which are in the correct position for an FET device. However, one major drawback is the need to anneal the hydrothermally grown ZnO NWs to above 400°C in order to observe semiconducting behaviour [110]. The need for an anneal stage will be discussed, along with the subsequent changes to device performances and characteristics.

Despite the inherent advantages in using in-situ laterally-aligned NW arrays as the basis for FETs, there are only a limited number of research teams who have looked at the performance of laterally aligned hydrothermal ZnO nanowires for FET applications. These can be split into devices with a dense multi-nanowire array channel, and those with a single isolated ZnO NW. Both offer insight into the behaviour of the hydrothermally grown ZnO NWs and their suitability for FET devices. Importantly, both multi-nanowire and single-nanowire FETs offer a playing ground to explore the mechanisms of conduction in ZnO, with a nanowire system presumably rich in surface defects.

3.3.1 FETs fabricated with lateral NW arrays

Park et al.

Park et al. [93] have fabricated FETs using in-situ laterally-aligned ZnO nanowire arrays synthesised by the hydrothermal method. Standard photolithography and lift-off techniques are used to pattern two ZnO seeds, separated by a small distance, on an SiO_2(300 nm)/p-Si substrate. Each ZnO seed is individually capped with Ag to deter vertical NW growth and to act as a contact metal, similar to Figure 2.9 in Chapter 2. ZnO nanowires are grown using equimolar 10 mM $Zn(NO_3)_2$/HMT solution for 6 hours at 85°C. Lateral overlapping ZnO nanowires are grown from both ZnO seed side-walls, bridging the electrodes and forming a conduction channel. The resulting nanowires had an average diameter of 100 nm, and an average length of 5 μm.

The nanowires are annealed in N_2 ambient for 2 minutes at 450 °C prior to being measured. Typical device characteristics indicated an n-type FET with an on-off

ratio of 3×10^{-4}, a threshold voltage of ≈-35 V, a field-effect mobility of ≈5.3 cm^2 V^{-1} s^{-1}, and a transconductance of 250 nS. The FET does not display a saturation regime at high gate voltages, which is attributed to increased carrier scattering caused by junction effects and the large surface area of the active channels.

Improved FETs were fabricated by first laterally growing ZnO nanowires from a single ZnO seed side-wall, and subsequently metallizing the terminating NW ends with Ag using standard lithographic and lift-off techniques. These nanowires were also annealed in N_2 ambient for 2 minutes at 450°C prior to FET characterization. The resulting output characteristics are displayed in Figure 3.6, where (a) shows I_{DS} - V_{DS} curves at different values of V_G, and (b) shows transfer characteristics. The FET exhibits typical n-type behaviour, with an on-off ratio of 4×10^5, a threshold voltage of ≈-15 V, a field effect mobility of 8.5 cm^2 V^{-1} s^{-1}, and a transconductance of ≈400 nS. Subthreshold swings were not provided, although are clearly >1 V/decade given the transfer characteristics. Similar to the original FETs, the drain-source current does not show a saturation regime, which is again attributed to surface defects. The improved device performance was attributed to the absence of the potential-energy barrier height caused by nanowire-nanowire junctions present in the channel of the original FET.

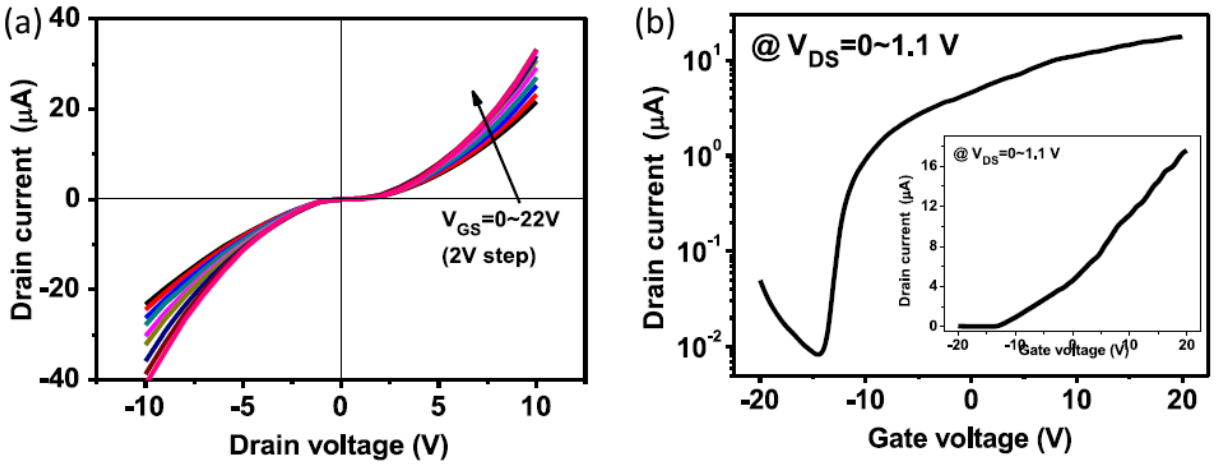

Figure 3.6: IV measurements from an improved FET fabricated by Park et al. (a) Drain current versus drain voltage curves at different gate voltages with 2 V steps (b) Logarithmic and linear (inset) scale transfer measurements taken at V_{DS} = 1.1V. Figure reproduced from [93].

Ko et al.

Ko et al. [111] have fabricated ZnO NW FETs on flexible substrates using as-grown NWs synthesised via the hydrothermal method. Gold nanoparticles were first

dispersed onto a dielectric/back-gated flexible substrate, forming a self-assembled monolayer. This monolayer was then imprinted with a PDMS mold which defined two separated electrodes, and subsequently heated to 140°C. This caused the gold nanoparticles to melt and coalesce into well-defined source and drain electrodes. The substrates were then spin-coated with a solution of ZnO quantum dots in an ethanol solution, which provide the seeds for nanowire growth.

Nanowires were grown by using an equimolar solution of 25 mM $Zn(NO_3)_2$/HMT at 65 - 95°C for 3 hours. The nanowires grown from these seeds were hexagonal wurtzite single crystals, verified by SEM and transmission electron microscopy (TEM). The average nanowire had a diameter between 150 - 300 nm, and a length between 1 - 3 μm. The electrical characteristics and field dependence of the transistors were measured. The average FET was found to be n-type with an on-off ratio of 10^4 - 10^5, a threshold voltage of -5 V, and a transconductance of $\approx$100 nS. The average subthreshold swing is provided as 8V/decade, which is a relatively high value. This may be due to the fact that the nanowires are unannealed. The field effect mobility could not be reliably estimated due to the uncertainty in the channel length of the transistors. Similar to Park et al. [93], the FET did not exhibit a clean saturation regime. This was attributed to the convoluted network of grain boundaries at the nanowire junctions, which prohibit carrier transport.

Pachauri et al.

Pachauri et al. [112] fabricated liquid-gated FETs using hydrothermally-synthesised nanowires grown in specific locations. Metal electrodes were first defined on an SiO_2(600nm)/Si substrate using standard photolithographic techniques. These electrodes were then covered in ZnO nanoparticles through dielectrophoresis by applying an alternating current to the metal electrodes. This ensures that the nanoparticles adhere to the electrodes only, to allow for site-specific growth of the ZnO nanowires.

ZnO nanowires were then grown from the ZnO nanoparticles by submerging the samples into an equimolar mixture of 0.25 mM $Zn(NO_3)_2$/HMT at 85 °C for up to 44 hours. Nanowires were grown both with and without a 4 hour preheat to the growth solution. The resulting ZnO nanowires were found to be too resistive to allow for electrical measurements, and were subjected to a rapid thermal anneal at 800°C for 30 seconds in ambient air, or a prolonged anneal at 300°C lasting a few hours. This typically decreased the resistance of the nanowires by several orders of magnitude.

Once the resistivity of the ZnO nanowires had been lowered, photolithographic

methods were used to define reservoirs and liquid channels for liquid gating measurements. Each reservoir was filled with de-ionised water as the dielectric liquid. All of the ZnO nanowire FETs showed n-type transport, with on-off ratios typically between 10^4 to 10^6. The subthreshold slopes for the FETs were typically between 100 - 200 mV/decade. The transconductance was measured on the order of 1 μS, and the field-effect mobility on the order of 1 cm^2 V^{-1} s^{-1}. Threshold voltages were not reported, although must have fallen within a V_G = -1 to +1 V range.

3.3.2 FETs fabricated with individual ZnO nanowires

Kalblein et al.

Kalblein et al. [113] fabricated FETs using individual ZnO nanowires grown using a variation of the hydrothermal method. A 1 cm$\times$1 cm 250 μm thick square of Zn foil was immersed in an aqueous solution of 480 mM sodium hydroxide and 95 mM ammonium persulfate at 150°C for 48 hours. The resulting nanowires had diameters ranging from 20 to 200 nm and aspect ratios as large as 500. The wires were sonicated in IPA and dispersed on an SiO_2 (200 nm)/Si global back-gated substrate. FETs were fabricated by contacting the ends of the nanowires using electron-beam lithography, and then employing the SiO_2/Si substrate as a dielectric and back-gate.

After depositing metal contacts, the as-grown nanowires were found to be n-type with a very high charge carrier concentration, and consequently unresponsive to gate voltages. Annealing processes were carried out in ambient air at 200°C, 400°C, and 600°C for 15 minute intervals, and the resulting field dependence was investigated. Figure 3.7(a) shows an SEM image of a single ZnO FET transistor, while (b) and (c) show output characteristics and transfer characteristics of an FET fabricated from an as-grown NW. The transfer characteristics of different FETs fabricated from NWs annealed at 200°C, 400°C, and 600°C are shown in (d), while (e) and (f) shows the transfer and output characteristics of an FET fabricated from a NW annealed at 600°C. The FETs annealed at 200°C and 400°C still exhibited metallic electrical behaviour and were not field dependent, while the FET annealed at 600°C exhibited a strong field dependence. This corroborates with theoretical calculations made by Bang et al. [114].

After annealing at 600°C, the FET exhibited an on-off ratio of 10^7, a threshold voltage of $\approx$-10 V, a field effect mobility of 40 cm^2 V^{-1} s^{-1}, and a subthreshold swing of 400 mV/decade. The transconductance was 0.2 μS. Even on a conventional Si/SiO_2 substrate with a global back-gate, the hydrothermally grown nanowires exhibit excellent device characteristics that are on par with FETs constructed using single ZnO nanowires grown via high-temperature chemical vapour deposition (CVD) techniques

[115, 116].

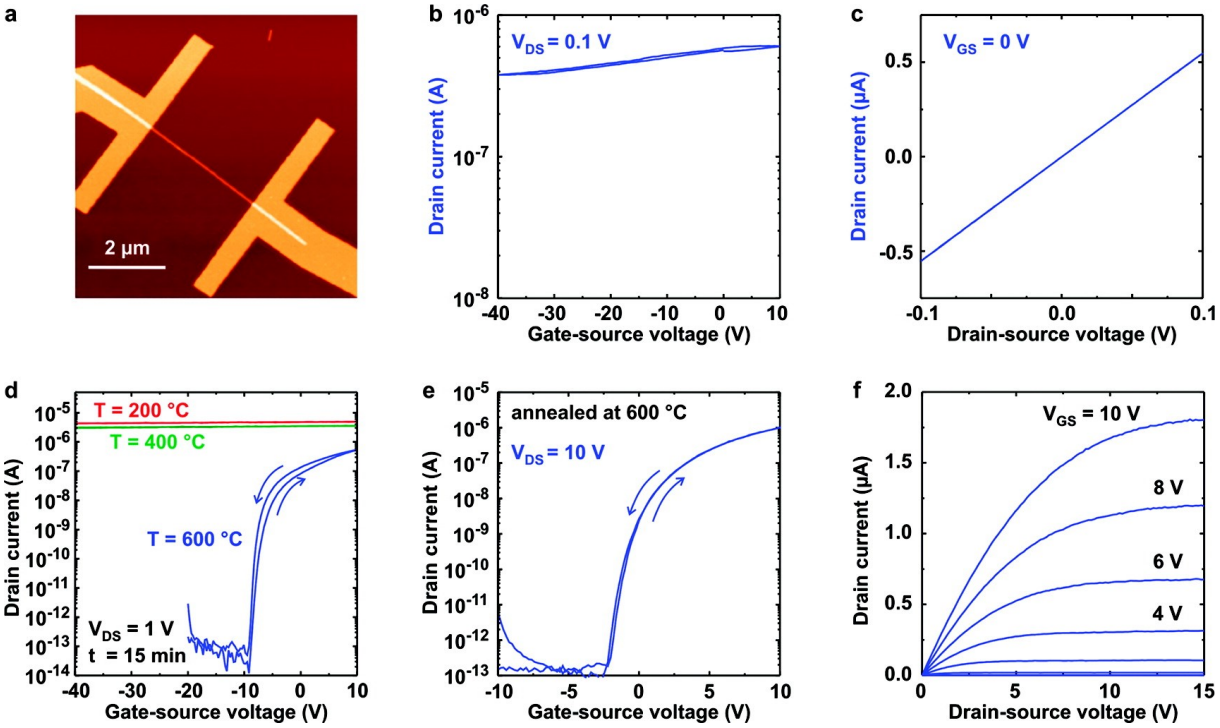

Figure 3.7: Electrical characteristics of ZnO nanowire FETs in the global back-gate configuration. (a) Atomic force microscopy image, (b) transfer characteristics, and (c) output characteristics of an as-grown ZnO nanowire with Al source and drain contacts. (d) Transfer characteristics of three ZnO nanowire FETs based on nanowires annealed at 200 °C (red), 400 °C (green), and 600 °C (blue) for a drain-source voltage VDS = 1 V. (e) Transfer and (f) output characteristics of a ZnO nanowire FET based on a nanowire annealed at 600 °C in air for 15 min. Figure reproduced from [113].

Having established optimum annealing conditions for the ZnO nanowires, top-gated FETs were fabricated by selectively depositing Al contacts onto an annealed nanowire via electron-beam lithography. The dielectric for the top-gate was fabricated by covering the nanowire with a 2 nm thick self-assembled monolayer. After the source and drain contacts were fabricated, the nanowires were exposed to an O_2 plasma. This increases the number of surface hydroxyl groups, which in turn improves the quality of the alkylphosphonic acid self-assembled monolayer (SAM) [117]. After the plasma treatment, the sample was immersed in a solution of 1 mM of octadecylphosphonic acid, forming a self-assembled monolayer which serves as the dielectric. Au was then thermally deposited on top of the ensemble, forming the top gate of the FET. Subsequent electrical measurements showed the FET had an on-off ratio of 10^7, a threshold voltage of $\approx$-1 V, and a transconductance of 1 μS. The subthreshold slope was measured to be as low as 90 mV/decade. The field-effect mobility of the SAM FET was not reported.

Kalblein et al.[118] fabricated a similar device in 2014 which coupled the self-assembled monolayer dielectric with a thin aluminium oxide layer. This oxide layer naturally formed from using Al as the contact metal for the top gate. This hybrid top-gate showed improved device performance compared with their previous monolayer-only dielectric, resulting in much lower leakage currents and higher operational voltages. Nanowires were synthesised using their previous method, and once again required annealing at 600°C to reduce the excessive charge carrier concentration.

FETs were fabricated as per the previous publication, with single-nanowire transistors showing on-off ratios of 10^7, transconductances as high as 7 μS, and subthreshold slopes of 150 mV/decade. Improvements were made to the FET architecture by arranging the source and drain electrodes in a honeycomb-like array over the nanowire. The best transistor fabricated in this architecture had an on-off ratio of 10^8, a peak transconductance of 50 μS, and a subthreshold slope of 100 mV/decade. The threshold voltage was not reported, although must fall within V_G = -1 to 1 V.

Law et al.

Law et al. [109] fabricated an FET using a single hydrothermally synthesised NW as part of their research into hydrothermally grown vertical nanowire arrays for solar cell applications. Although measurements of the FET were not part of the main manuscript, they were included in the supplementary information. ZnO nanowires were synthesised using a 25 mM equimolar $Zn(NO_3)_2$/HMT aqueous solution, with an additional 5 - 7 mM of PEI to assist NW growth. Subsequent nanowires had aspect ratios up to and greater than 125.

Nanowires were harvested from the growth substrate and distributed onto the SiO_2(300 nm)/Si device substrate via an ethanol suspension, and then annealed at 400°C in air for 30 minutes. An FET was fabricated by selecting a nanowire approximately 8-10 μm long and depositing Al contacts on the terminating ends using electron beam lithography. The FET had an on/off ratio of 10^5, a threshold voltage of $\approx$-50 V, and a field-effect mobility of 1 - 5 $cm^2\ V^{-1}\ s^{-1}$. The transconductance and subthreshold swing of the FET was not reported. Despite the high-temperature annealing step, the very large threshold voltage shows how difficult it is to thoroughly deplete the ZnO nanowire.

Opoku et al.

Opoku et al. explored the relationship between high-temperature annealing and field dependence [54]. ZnO nanowire growth substrates were prepared by coating Si substrates with a thin film of ZnO using the sol-gel method. ZnO nanowires were then grown using equimolar 25 mM $Zn(NO_3)_2$/HMT along with 5 mM of PEI (M_W = 800 g/mol) at 95 - 100°C for 12 - 15 hours. This sequence was repeated up to 5 times to grow increasingly long nanowires, typically longer than 9 μm, with diameters usually on the order of 100 nm in diameter.

Nanowires were transferred from the growth substrate to SiO_2(170 nm)/Si device substrates by sonication and flow-directed assembly. After deposition, the substrates were softbaked at 200°C to ensure that no solvent remained on the substrates. FETs were then fabricated by contacting the nanowires using 200 nm Pt contacts defined via standard electron beam lithography and photolithography.

These FETs showed very little response to applied gate voltages due to an excessive charge carrier concentration, with an on-off ratio of ≈0.6 between V_G = 0 V and V_G = -120 V. These device characteristics were improved by annealing the FET at 550°C in ambient air for 30 minutes. After annealing, the nanowire FETs did show some form of field dependence, with an on-off ratio of 10^4 and a threshold voltage of -26 V. Despite the 550°C anneal, the devices switched from on to off very gradually, and over a very broad gate voltage range. Measurements of the subthreshold slope were as high as 15 V / decade. The transconductance was measured to be ≈0.002 μS, while the field-effect mobility was ≈0.13 $cm^2\ V^{-1}\ s^{-1}$. Transfer characteristics of the as-fabricated FETs and post-anneal FETs are shown in Figure 3.8.

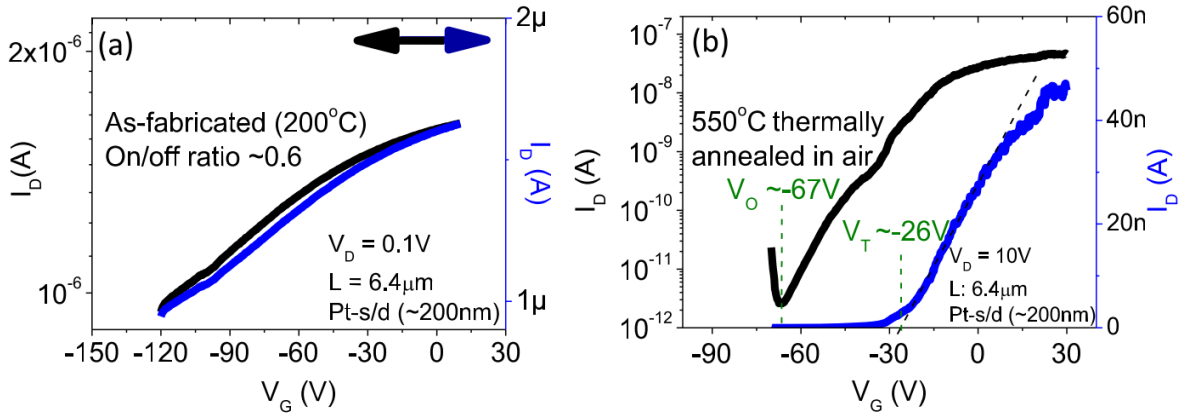

Figure 3.8: Transfer characteristics of (a) as-fabricated and (b) annealed FETs. Figure reproduced from [54].

These FETs were significantly improved upon by first annealing the nanowires af-

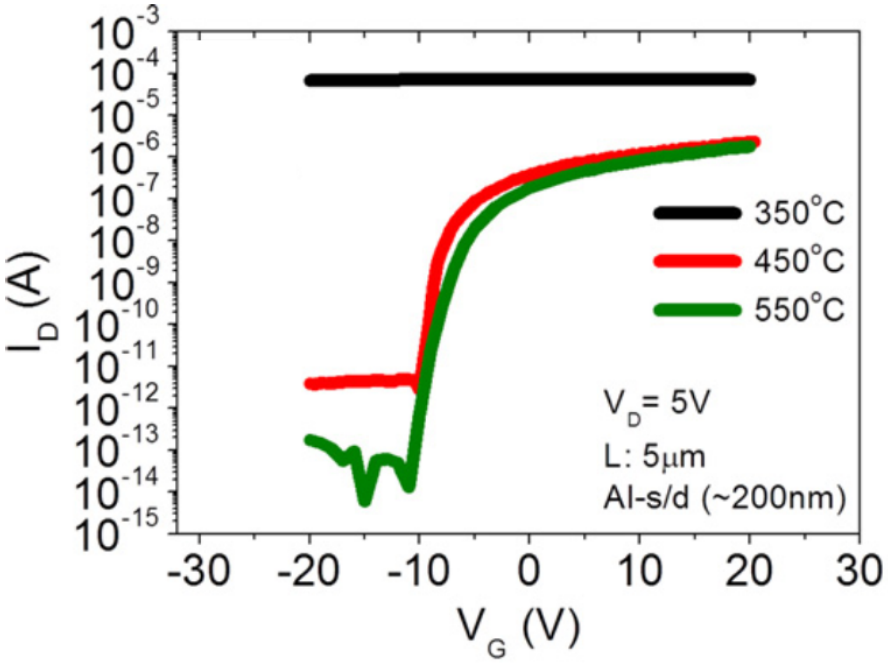

Figure 3.9: Transfer characteristics of FETs fabricated using nanowires annealed at 350 (black), 450 (red), and 550°C (green). Figure reproduced from [54].

ter transfer to the device substrate, and then contacting the nanowires using electron beam lithography. Al was also used as a contact metal instead of Pd due to its low work function. Nanowires were separately annealed at 350°C, 450°C, and 550°C to investigate between the annealing temperature and device performance. The nanowire annealed at 350°C effectively shows no field dependence, while nanowires annealed at 450°C and 550°C both show field dependence. These devices showed on-off ratios of 10^5 and 10^7 respectively, with threshold voltages of -5 and -2 V. The subthreshold swings were 550 - 580 mV/decade, and the field mobilities were 5 and 11 $cm^2\ V^{-1}\ s^{-1}$. Transfer characters of all three FETs are shown in Figure 3.9.

Despite the improved device characteristics achieved after annealing the nanowires, there is clearly some variation between devices fabricated using identical methods. Opoku et al. published a second paper [106] which used a nanowire FET fabricated as per their first publication. The nanowire was annealed at 450°C before Al source-drain contacts were defined and deposited on the nanowire ends. The FET did show clear field dependence, with an on-off ratio as high as 10^8. The subthreshold swing of the device was ≈630 mV/decade, which is similar to the FETs fabricated in the first publication. However, the threshold voltage was approximately -26 V, which differs significantly from their previous FETs.

Wang et al.

Wang et al. [119] directly compared FETs manufactured with hydrothermally-grown single nanowires and single nanowires grown using high-temperature vapour-phase transport (VPT). The exact details of the hydrothermal synthesis are left unspecified, citing Gao et al. [120] in lieu of specific concentrations of precursors. Therefore the nanowires were most likely synthesised using 100 mL aqueous solutions of equimolar (0.02M) zinc chloride ($ZnCl_2$) and HMT, with an additional 1-5 mL of ammonia (NH_3).

Hydrothermally grown nanowires were transferred from the growth substrate to the SiO_2(300 nm)/p-Si device substrate via dispersion in an ethanol solution, and subsequently annealed at 550°C in ambient air for 4 hours. A nanowire with a diameter of 200 nm and an aspect ratio of ≈17 was selected for FET fabrication. Electrodes were patterned on the ends of the single nanowire and a 200 nm thick layer of indium tin oxide (ITO) was deposited using a direct-current sputter coater. After a liftoff process to define the patterned electrodes, the entire sample was subjected to a second anneal at 400°C in ambient air for 30 minutes in order to improve the conductivity of the ITO electrodes.

Subsequent electrical measurements showed the hydrothermal NW FET was n-type, with an on-off ratio of 10^6, a threshold voltage of -48.5 V, and a field effect mobility of 18.27 $cm^2\ V^{-1}\ s^{-1}$. Neither the transconductance or subthreshold swing of the hydrothermal NW FET were reported. The FET used for comparison features a VPT-grown single NW, the synthesis details of which are cited from the paper of Yang et al. [121]. The VPT FET is fabricated using the same electrode patterning process as used in the fabrication of the hydrothermal FET.

The VPT FET was characterized and found to have an on-off ratio of 10^5, a threshold voltage of -14V, and a field effect mobility of 36.94 $cm^2\ V^{-1}\ s^{-1}$. The transconductance and subthreshold swing of the VPT FET were not reported. Therefore, while the hydrothermal NW FET had a greater on-off ratio, its threshold voltage and field effect mobility were worse than the VPT NW FET. Wang et al. conclude that the difference in device characteristics between the two different FETs arises from the different defect densities introduced into the ZnO nanowires during their respective synthesis process.

Florica et al.

Florica et al. [122] also compared FETs fabricated using both hydrothermal and high-temperature dry-oxidised nanowires. ZnO nanowires were synthesised hy-

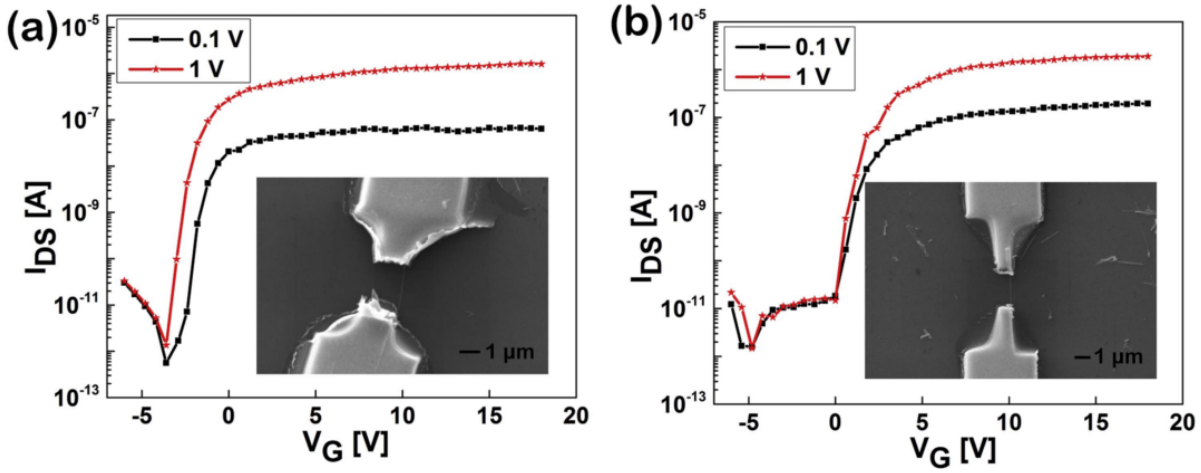

Figure 3.10: Transfer characteristics of as-fabricated hydrothermal (a) and dry-oxidised (b) FETs. Figure adapted from [122].

drothermally using thin films of Ti/Au (10/90 nm) on Si as growth substrates. Growth solutions were prepared using equimolar 0.1 mM $Zn(NO_3)_2$/HMT at 90 °C inside a convection oven. The solution was preheated for 5 hours before the substrates were introduced. The growth took place over a total of 2 days before the growth substrates were removed and rinsed. Instead of regular VPT methods, the high-temperature nanowires were synthesised by oxidising a zinc foil in a convection oven at 500°C for 12 hours.

Both hydrothermal and high-temperature nanowires were isolated from their respective growth substrates by drop-casting the nanowires onto SiO_2(50nm)/Si device substrates. Standard electron beam lithography and liftoff techniques were used to make Ti/Au (100/300 nm) source and drain contacts on the nanowires. The devices were measured after electrode fabrication, without any annealing or plasma treatments.

Both hydrothermal and dry nanowires showed field dependence when measured, with on-off ratios of approximately 10^4 - 10^5, and threshold voltages of -4 V and +0.4 V, respectively. The field-effect mobilities were inferred from the transconductance to be 76 and 132 $cm^2\ V^{-1}\ s^{-1}$ respectively, although no value for the transconductance is supplied. The subthreshold swings were 342 mV/decade and 534 mV/decade, respectively. The transfer characteristics of the as-fabricated hydrothermal and dry nanowires are shown in Figure 3.10.

After the FETs were initially measured, the nanowires were covered in a layer of polymethylmethacrylate (PMMA), which acts as a passivation layer. The threshold voltages of the modified hydrothermal and dry FETs reportedly shift by $|\Delta V_{DS}|$ = 3

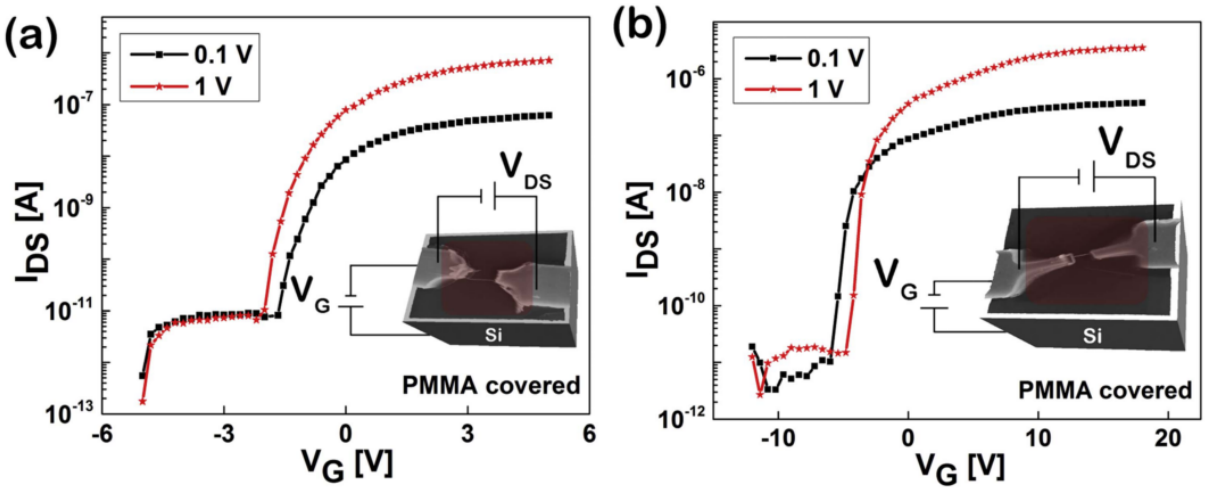

Figure 3.11: Transfer characteristics of PMMA-passivated hydrothermal (a) and dry-oxidised (b) FETs. Figure adapted from [122].

V and 1.2 V, respectively. The field-effect mobilities are reported as 87 cm^2 V^{-1} s^{-1} and 167 cm^2 V^{-1} s^{-1} post-passivation, respectively. The subthreshold swings are also improved, with post-passivation values of 269 mV/decade and 431 mV/decade, respectively. Transfer characteristics for both hydrothermal and dry nanowire FETs post-passivation are shown in Figure 3.11.

Summary of fabricated devices

The main FET characteristics of the papers presented above are summarized in Table 3.1.

Device geometry effects

All of the ZnO nanowire FETs which have been studied here are based on laterally-aligned nanowires, which ostensibly lie flush with the substrate. These nanowires are then used as FETs in conjunction with a top or bottom gate dielectric, which is usually considered to be flush and in contact with the nanowire. However, in some cases this is a simplification, as the nanowire can be separated from the gate dielectric by a small air gap. This can especially be a problem for FETs fabricated using arrays of lateral nanowires, where nanowires grow out of seeded sidewalls at angles.

ZnO nanowire FETs have previously been intentionally fabricated with air gaps between the channel and the dielectric, which provide information on how a less-than-flush geometry can affect the device performance. In general, nanowire FETs with air gaps have higher threshold voltages than those lying flush with the substrate dielectric [123]. This is due to the depleting effect of adsorbed oxygen and hydroxyl

groups on the nanowire surface; when the nanowire is separated from the dielectric by an air gap, oxygen groups are able to adsorp to entire nanowire surface, depleting them of electrons and requiring higher threshold voltages to populate the channel [123]. In comparison, surface states at the nanowire/dielectric interface can contain trapped positive charges, which locally affect the voltage and reduce the depletion width within the nanowire.

Devices with air gaps can also suffer from reduced gate effectiveness due to the additional distance between the nanowire and the gate electrode [124, 35], and epoxy or other filling layers can be required to reduce the impact of the air gap [124]. However, separating the nanowire from the dielectric layer has the advantage of reducing leakage current, meaning that low off-currents can be achieved in air-gap devices [35].

As such, the presence of air gaps in ZnO nanowire FETs can affect the device performance. Furthermore, if the FETs are fabricated by bridging lateral arrays of nanowires, then possible air gaps in the device geometry can be difficult to control, seeing as they are determined by the angle of nanowire growth from the seeded substrate. These imperfections can add a level of variation between fabricated transistors, which may be present in the devices reviewed in this chapter and presented in this thesis.

Table 3.1: Summary of the synthesis and device characteristics of the nanowire FETs presented in this chapter.

Authors	Precursors	# of NWs	Gate	V_{Th} (V)
Park et al.	10 mM $Zn(NO_3)_2$/HMT	Many	SiO_2(300 nm)	≈-35
Ko et al.	25 mM $Zn(NO_3)_2$/HMT	Many	SiO_2	-5
Pachauri et al.	0.25 mM $Zn(NO_3)_2$/HMT	Many	DI H_2O	$-1 \leq V_{Th} \leq 1$
Kalblein et al.	480 mM KOH 95 mM ammonium persulfate	1	2 nm SAM	$-1 \leq V_{Th} \leq 1$
Law et al.	25 mM $Zn(NO_3)_2$/HMT 7 mM PEI	1	SiO_2(300 nm)	-50
Opoku et al.	25 mM $Zn(NO_3)_2$/HMT 5 mM PEI	1	SiO_2(170 nm)	-2
Wang et al.	25 mM $Zn(NO_3)_2$/HMT 1 - 5 mL NH_3	1	SiO_2(300 nm)	-48.5
Florica et al.	0.1 mM $Zn(NO_3)_2$/HMT	1	SiO_2(50 nm)	-4

Authors	On-off ratio	SS (mV/dec)	g_m (nS)	μ_{eff}	Anneal
Park et al.	$\approx 4\times10^5$	≥2000	400	8.5	450 °C in N_2 for 2 min
Ko et al.	$\approx 10^4$	8000	100		n/a
Pachauri et al.	10^4 - 10^6	100 - 200	1000	1	800 °C in air for 30s
Kalblein et al.	10^7	90	1000		600 °C in air for 15 min
Law et al.	10^5			1 - 5	400 °C in air for 30 min
Opoku et al.	10^7	580		11	600 °C in air for 15 min
Wang et al.	10^6			18.27	550 °C in air for 4 hours
Florica et al.	10^4	342		76	n/a

3.4 ZnO nanowire doping and annealing

3.4.1 n-type ZnO nanowires

It is a well-established fact that the vast majority of as-grown ZnO is doped with shallow donors, giving rise to a strongly n-type behaviour [125]. The high charge carrier concentrations can be beneficial in certain applications, such as those needing transparent conductors. For FET applications, it is desirable to use high-quality intrinsic ZnO with fewer charge carriers, as this gives rise to a stronger field dependence, a threshold voltage closer to 0 V, a high on-off ratio, and better device performance overall. As is evident in the literature being studied here, as-grown hydrothermally-synthesised ZnO NWs are not necessarily suitable for FET applications due to excessively high charge carrier concentrations.

It is difficult to determine the exact charge carrier concentration where ZnO nanowires become difficult to use in FETs. However, an order-of-magnitude approximation can be estimated by considering the doping concentration required to degenerately dope the nanowires. In this regime, the distance between electron donors is sufficiently small enough for their wavefunctions to overlap, forming a defect band which can overlap with the conduction band. This means that the Fermi level constantly lies within the defect band, even at very low temperatures. The charge carrier concentration required to achieve degenerate doping in a semiconductor can approximated by setting it equal to the effective density of states in the conduction band. This can be estimated as [38]:

$$\mathrm{n_{eff}} = 2\Big(\frac{2\pi \mathrm{m_{eff}} \mathrm{k_B T}}{\mathrm{h}^2}\Big)^{\frac{3}{2}} \tag{3.2}$$

where $\mathrm{m_{eff}}$ is the effective mass of the electron, $\mathrm{k_B}$ is Boltzmann's constant, T is the temperature, and h is Planck's constant. Taking $\mathrm{m_{eff}}$ to be approximately 0.3 $\mathrm{m_0}$ [12] and T to be 293.15 K (corresponding to 20°C), the degenerately doped carrier concentration is calculated to be $\approx 4.2 \times 10^{18}$ cm^{-3}.

The necessity of a high-temperature anneal to address the excessive doping in ZnO nanowire devices negates some of the inherent advantages of the hydrothermal synthesis technique, such as the ability to grow in-situ laterally-aligned nanowire arrays on vulnerable and delicate substrates that would be destroyed in the process of VPT synthesis methods. Therefore, there is a strong motivation to unequivocally determine the cause of the naturally n-type behaviour in ZnO nanowires.

As described in the introduction to this thesis, the origin of doping in ZnO has

been a matter of intense theoretical work over the past decade. Initially attributed to intrinsic point defects [125] such as Zn interstitials and O vacancies, other theoretical treatments by Janotti et al. [126] have suggested that intrinsic point defects cannot explain the n-type behaviour of ZnO. Building on this theoretical framework, hydrogen and its interactions with native point defects has been suggested as the main shallow donor leading to n-type behaviour [127, 25, 128, 114]. The exact nature of the dopants is still a point of contention however, with continued theoretical research suggesting that native defects are responsible for the n-type behaviour [129]. An in-depth discussion of the controversial n-type doping is outside of the scope of this thesis, and has been reviewed comprehensively in the past [130].

Part of the difficulty in determining what exactly causes the doping in ZnO is the fact that theoretical predictions of what annealing temperatures are required to purge suspected dopants from the bulk are not always mutually exclusive. Bang et al. [114] have used first principals calculations, in conjunction with kinetic Monte-Carlo simulations, to model the diffusion and stability of hydrogen in ZnO. Predictions based on the simulations are displayed in Figure 3.12, with Figure 3.12(a) displaying the relationship between hydrogen diffusion and anneal temperatures, and Figure 3.12(b) displaying the relationship between defect concentration and time at room temperature.

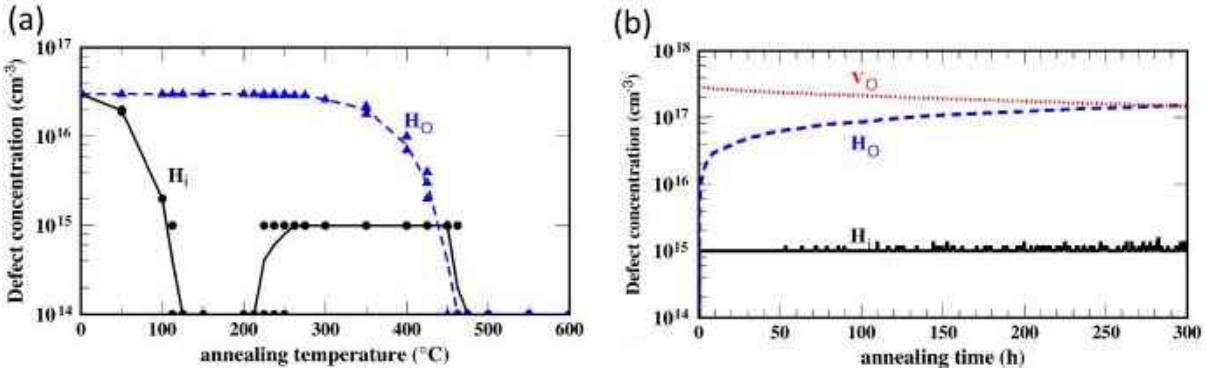

Figure 3.12: The results of kinetic Monte Carlo simulations for (a) the H diffusion at different annealing temperatures and (b) the evolution of injected H atoms at room temperature. Lines represent the average of simulations up to five, and points at the concentration of 10^{14}cm^{-3} correspond to nearly zero concentration in simulations. Figure reproduced from [114].

Systematic research into the annealing response of VPT-grown ZnO nanowires for FET applications has been conducted by Jin Jeon et al. [110]. VPT-grown ZnO nanowires were dispersed onto an SiO_2(200nm)/p-Si device substrate. Several devices were made in both global back-gated geometries, and top-gated geometries utilising

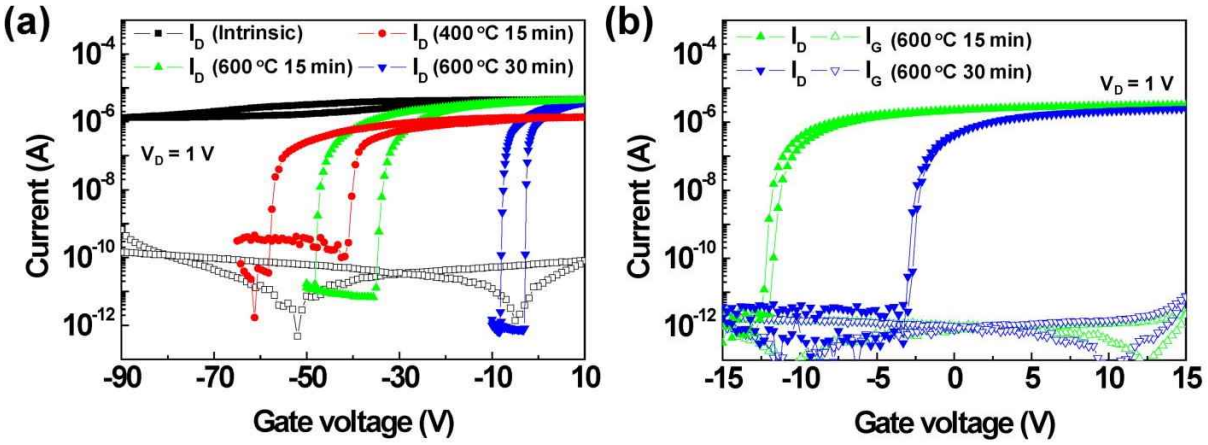

Figure 3.13: Transfer curves measured at V_{DS}=1V from the bottom-gate FETs with ZnO NWs prepared under various conditions: un-annealed (black line), air-ambient annealed at 400°C for 15min (red line), air-ambient annealed at 600 °C for 15min (green line), and at 600°C for 30min (blue line). (b) Transfer curves measured at V_{DS}=1V from the top-gate FETs with ZnO nanowires that were annealed at 600°C. Figure reproduced from [110].

a 30 nm Al_2O_3 layer as the dielectric. Individual back-gated devices were annealed at 400°C for 15 minutes, 600°C for 15 minutes, and 600°C for 30 minutes, while individual top-gated devices were annealed at 600°C for 15 minutes, and 600°C for 30 minutes. An unannealed back-gated device was also measured to serve as a control.

After annealing, the individual devices had their transfer characteristics measured. The transfer characteristics of the different back-gated FETs are displayed in Figure 3.13(a). The unannealed nanowire exhibits very low field dependence, making it unfit for use in an FET. Significantly higher field dependence is observed in the back-gated device annealed at 400°C for 15 minutes, achieving an on-off ratio of 10^4, but the associated threshold voltage (≈-65 V) makes the device unsuitable for FET applications. The back-gated device annealed at 600°C for 15 minutes shows improved device characteristics, with an on-off ratio of 10^5 and a threshold voltage of -47 V. Finally, the back-gated device annealed at 600°C for 30 minutes shows an even more pronounced improvement in device characteristics, achieving an on-off ratio of 10^6 and a threshold voltage of -8 V.

The top-gated devices show a similar trend, although for any given annealing condition the top-gated devices exhibited better overall device characteristics. 15 minute and 30 minute anneals at 600°C yielded on-off ratios greater than 10^6 and threshold voltages of -12 V and -3 V respectively. The transfer characteristics of the top-gated FETs are displayed in Figure 3.13(b).

While Jin Jeon et al. attribute this improvement of device characteristics with increasing annealing temperatures and times to a reduction of oxygen defects on the surface of the nanowires, the results of their study agree well with Bang et al.'s model of hydrogen defects and thermal stability. Bang et al.'s model also explains why Kalblein et al.'s FET does not exhibit a field dependence at 200°C and 400°C, and a pronounced field dependence at 600°C. Jin Jeon et al.'s back-gated FETs exhibit field dependence after being annealed at 400°C for 15 minutes, while Kalblein et al.'s FET does not exhibit any field dependence after being annealed at 400°C. However, Jin Jeon et al. sweep their gate voltage to -70 V, and only observe depletion at -65V, while Kalblein et al. only sweep their gate voltage to -40V.

Although the vast majority of ZnO nanowire FETs exhibit field dependence only after annealing, there are a number of reported FETs fabricated with VPT synthesised ZnO nanowires that show field dependence before annealing [131, 132]. The reason why ZnO nanowires exhibit field dependence without the need of an anneal is currently unknown, and should warrant great attention. It may be that many of the VPT methods in the literature that take place at high temperatures actually incorporate the necessary anneal stage post-growth. For example, in a paper by Sohn et al. [131], NWs are grown at 900°C, and subsequent FETs utilizing said NWs require no annealing step for good device performance. However, in the above mentioned paper by Jeon et al. [110], the NW synthesis temperature is lower, at 760°C.

3.5 Hysteresis and passivation in ZnO nanowire FETs

Transfer characteristics of FETs are acquired by fixing the drain-source voltage at a given value while sweeping the gate voltage, as described in the beginning of this chapter. The gate voltage can be swept towards the positive or negative direction, although comprehensive transfer characteristic measurements sweep the gate voltage in both directions. These measurements can reveal a discrepancy in the drain-source current at a given gate voltage depending on the direction of the gate voltage sweep, which is known as hysteresis. Hysteresis has been observed in many FETs which use nanomaterials, including nanowire devices such as carbon nanotubes [133] and germanium nanowires [134], and 2D semiconducting materials, such as graphene [135] and molybdenum disulphide [136].

Hysteresis has also been recorded in ZnO nanowire FETs, although comprehensive transfer characteristic measurements of hydrothermally synthesised nanowires are rarely reported, and most measurements are taken by sweeping the gate voltage only in a single direction. For example, of the results reproduced in this chapter, only

Kalblein et al [113] (shown in Figure 3.7) and Jin Jeon et al [110] (shown in Figure 3.13) show transfer characteristic measurements comprehensive enough to gauge the hysteresis of the fabricated devices. Nevertheless, the literature on hysteresis and passivation in ZnO FETs is worth examining in the context of this thesis, as some of the transistors fabricated in later chapters show hysteretic behaviour.

Hysteresis in nanoelectronics is typically attributed to charges trapped or otherwise present in the vicinity of the semiconducting channel, which alter the local voltage and the band bending of the device. Hysteresis is desirable for some applications, and several publications have investigated using hysteretic ZnO nanowires for memory storage. These applications benefit from increasing the hysteresis through introducing or increasing charge trapping sites such as Al_2O_3 layers deposited directly onto the nanowire [137], ferroelectric liquid crystals [138] or polymers [139], ferroelectric nanoparticles deposited on the nanowire surface [131], or SiO_2 back-gate dielectrics treated by high-pressure hydrogen annealing [140].

Although these measures all increase the hysteresis of the FETs, many ZnO nanowires show an inherent hysteresis that is typically attributed to intrinsic charge traps on the nanowire surface [141, 142], or the nanowire/dielectric interface [141, 143, 144]. The surface states of the nanowire are thought to be electron-trapping oxygen or hydroxyl groups which are chemisorbed to the nanowire surface [141, 142], while the local charges located at the nanowire/dielectric interface have been attributed to adsorbed oxygen on the surface [143], mobile protons present in the substrate [140], or mobile negative charge carriers [137]. A definitive single cause of hysteresis likely does not exist, and ZnO nanowire FETs may be affected by several different charge trapping mechanisms simultaneously.

Hysteretic behaviour can cause serious problems for FETs, as the device performance can significantly change over time in unpredictable ways. Hysteresis driven by interactions between the ZnO nanowire surface and measurement atmosphere can cause transient effects in FETs [145], and the hysteresis has been shown to depend on the range and rate of the gate voltage sweep [142, 146]. Passivation techniques can be used to reduce the hysteresis, which typically involves encapsulating the ZnO nanowires in an inert material, preventing reactions with the atmosphere at the nanowire surface [141, 147, 148]. However, passivation doesn't always prevent hysteresis, as charge traps can remain at the nanowire/substrate interface, and interactions between the passivation layer and atmosphere can drive further hysteresis [137, 147, 142, 146].

Further reduction in hysteresis can be achieved by annealing ZnO nanowire devices at high temperatures and in different atmospheres. The work by Kalblein et al [113] and Jin Jeon et al [110] reproduced in this chapter clearly demonstrates the reduction in hysteresis with high-temperature annealing. This is attributed to a passivation or removal of defect states, which is also the same mechanism relating field dependence to high-temperature annealing. Other research has combined passivation layers with annealing to minimise hysteresis [144] or annealing in specific atmospheres [143].

In summary, hysteresis has been documented in ZnO nanowire FETs, similar to other nanomaterials used for FET applications. Despite this, the exact causes and origins of the hysteresis vary, and the hysteresis of a given device is likely compounded by several types of charge traps located on the nanowire surface and nanowire/substrate interface. Passivation techniques involve encapsulating the nanowire to remove nanowire/atmosphere interactions, although this does not necessarily compensate for charge traps at the nanowire/substrate interface. High-temperature annealing can also be used to expel and passivate charge traps in the device, reducing the overall hysteresis.

3.6 Conclusion

In conclusion, the fundamental device parameters used to characterise FETs have been described. While there are several publications which use hydrothermally-synthesised ZnO nanowires as FETs, the majority of these devices require high-temperature annealing at or above 400°C in order to show field dependence. In some cases, the nanowires show poor device characteristics even after being annealed, requiring high threshold voltages (up to -50 V) to sufficiently deplete the channel, or very high subthreshold swings (up to 8 V/dec.) The need to anneal devices before field dependence is likely due to excessive charge carrier concentrations in the ZnO nanowires, which are caused by unintentionally incorporated dopants. The exact nature of these dopants is still uncertain, although theoretical models implicating interstitial hydrogen or oxygen defects on the nanowire surface both agree with the relationship between field dependence and annealing which is recorded in the literature.

As such, there is a strong motivation to reliably fabricate FETs which show field dependence without requiring high-temperature annealing. The necessity of the high-temperature anneal strongly restricts the choice of substrates that the devices can be fabricated on. ZnO is otherwise well-suited for emerging nanoelectronic applications which are based around flexible, transparent, and disposable substrates,

but their full potential will not be realised until this impasse has been addressed.

Chapter 4

Experimental details

4.1 Introduction

This chapter details the experimental methods and processes used throughout the work presented in this thesis. It aims to describe the various pieces of equipment and the way in which they are used sufficiently enough for the interested reader to reproduce the experimental results reported in this work.

4.2 Fabrication of substrates for lateral nanowire growth

In order to use ZnO nanowires as field-effect transistors, the nanowires must be in contact with (or very close to) a dielectric layer, which itself is in contact with a gate electrode. One common approach is to use a heavily doped silicon wafer as the device substrate, and to consequently use the entire substrate itself as a gate electrode. In order to electrically isolate the substrate from the nanowires and source/drain electrodes, the silicon is thermally oxidised to produce a thin layer of SiO_2 on the surface.

SiO_2 (100 nm) / p^+-Si substrates (sourced from Silicon Quest International) were used as device substrates for lateral nanowire FETs. The wafers are 3" in diameter, and must be cleaved into smaller pieces to be used for device fabrication. As this cleaving process physically breaks the wafer into pieces, care must be taken not to ruin the thin SiO_2 dielectric on the wafer surface, or the device will leak and be unusable. To protect the wafer as much as possible, we first use a spin-coater to deposit a sacrificial layer of AZ1518 (Microchem) on the uncleaved wafers at 900 RPM for 60 seconds. AZ1518 is a photosensitive resin used for photolithography, although it is used here simply as a thin layer of material (on the order of 5 μm) that is soluble in acetone. The wafer is then baked on a hotplate at 95°C for a few minutes to expunge the AZ1518 of excess solvent.

We then spin a layer of polydimethylsiloxane (PDMS) at 600 RPM for 60 seconds to add a further level of protection to the wafer. PDMS is a robust organic two-part polymer made by mixing an elastomer curing agent with a silicone base (Sylgard 184 Incor) at a 1:10 mass ratio. The thickness of the PDMS layer on the wafer is on the order of hundreds of microns. The wafers are placed on a hotplate at 95°C for 15 minutes after the PDMS is spun on, which speeds up the curing process.

Although the p^+-Si wafers are highly doped and have a very low resistivity, it can be difficult to make good electrical contact to them as their back surfaces are unpolished. To ensure good contact to the back gate, the backs of the protected wafers are coated with Cr/Au (5/50 nm) via resistive resistive evaporation using our in-house Angstrom Engineering NexDep evaporator. The Cr serves as an adhesion layer for the Au, which is used as a contact metal because it doesn't corrode and has a high conductivity.

After the backs of the protected wafers have been metallised, they are cleaved into 1.1 $\times$ 1.1 cm squares using a diamond scribe and a metal ruler. The combined photoresist/PDMS layers confines the dust created when cleaving the wafer into pieces, leaving the SiO_2 surface largely free of particulates. After the wafer is cleaved, the individual squares are peeled away from the PDMS layer and placed in acetone, which dissolves the AZ1518 protective layer. The substrates are then individually sonicated in acetone and then IPA, which removes any residual contaminants or debris.

4.2.1 Photolithography

The fabrication of lateral ZnO nanowires relies on patterning electrodes/seed layers at specific locations on the substrate. We use optical photolithography to define our electrodes, which is a very common technique used in microfabrication. A photosensitive resin (known as a photoresist) is applied to the surface of the substrate via spin-coating. When the photoresist is exposed to ultraviolet (UV) light, it becomes soluble (or insoluble, depending on the specific photoresist,) to a chemical called a developer. In order to expose only specific parts of the photoresist to UV light, the UV light is filtered through a mask, which is typically a chrome stencil on a plate of soda lime glass.

After exposure, the substrates are washed in developer which dissolves and removes the unwanted parts of the photoresist. Once metal or other thin films have been

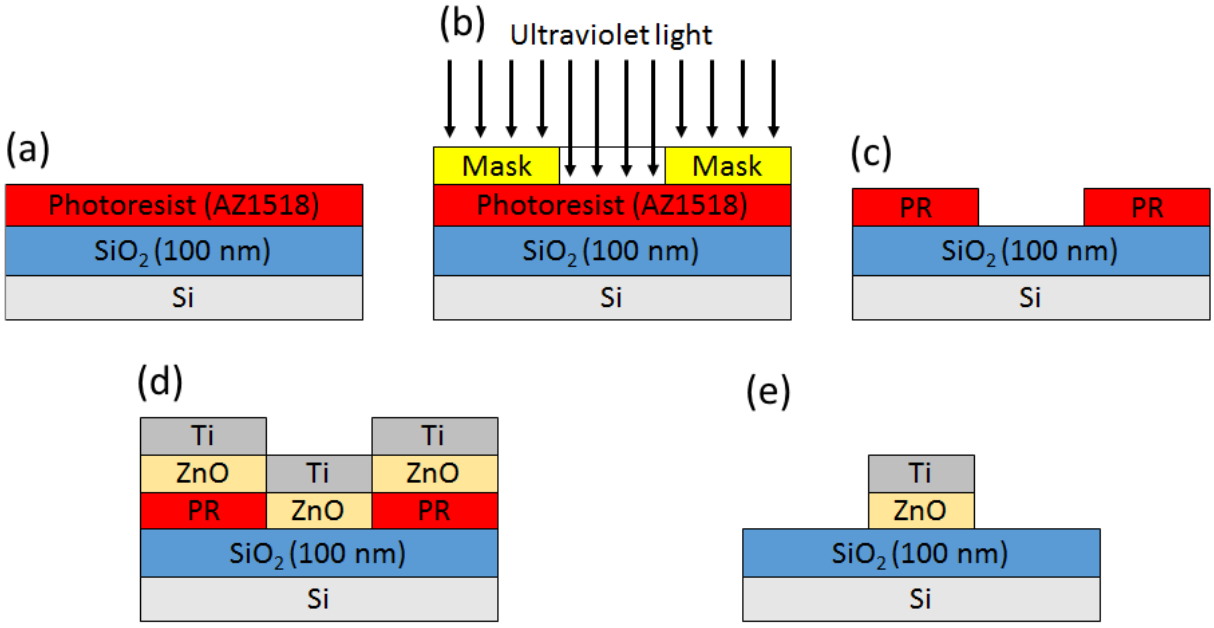

Figure 4.1: The photolithography process. (a) SiO_2 (100 nm)/Si substrates are spin-coated with AZ1518 photoresist. (b) Portions of the photoresist are selectively exposed to UV light using a mask aligner. (c) The substrates are developed, which dissolves the exposed photoresist. (d) Material (in this case, ZnO/Ti) is deposited onto the patterned substrates. (e) The substrates are lifted off, removing excess material.

deposited on the photolithographically patterned samples, the remaining photoresist is removed by submerging the substrates in acetone (otherwise known as a liftoff.) This dissolves the remaining photoresist and removes the deposited material that sits on its surface. The deposited material remains adhered to the parts of the substrate which were defined in the initial exposure and development stage. The entire photolithography process is depicted schematically in Figure 4.1.

All of the photolithography undertaken in this thesis was completed using a Karl Suss MJB3 mask aligner, equipped with an USHIO SHP 350W lamp. The masks used for fabricating lateral ZnO nanowires were custom-made at the University of Canterbury, using a Heidelberg μPG 101 mask writer. The mask .GDS files were designed using LayoutEditor. A schematic of the lateral nanowire mask is shown in Figure 4.2, with 30 - 50 μm gaps between pairs of electrodes. We have also made use of a mask with 8 pairs of electrodes, with gaps varying from 10 to 80 μm (not pictured.)

AZ1518 was spun on cleaned and cleaved wafers at 4000 RPM for 60 seconds. The substrates were then soft-baked at 95°Cs on a hotplate to remove residual solvent from the AZ1518 layer. AZ1518 is a positive-tone photoresist, meaning that it is insoluble in developer by default, and becomes soluble after UV exposure. The substrates are exposed for 10 seconds using the mask aligner, before being developed in AZ326 (Microchem), a common and widely-used developer which uses tetramethylammonium

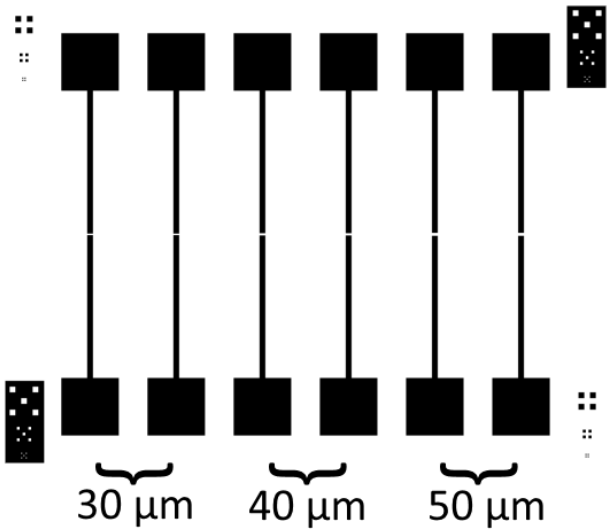

Figure 4.2: A schematic of the mask used to photolithographically define substrates for lateral ZnO nanowire growth. The size of the channel gaps is indicated at the bottom of the schematic. The array of squares on each corner of the schematic are used for alignment purposes.

hydroxide (TMAH) as its active ingredient. The AZ326 was diluted at a 3:1 AZ326:DI H_2O ratio before being used. Substrates were developed for 40 seconds and rinsed twice in DI H_2O to remove any residual scum.

4.2.2 Seed layer/electrode deposition

After the substrates have been patterned using photolithography, thin films of ZnO and Ti are deposited on the substrates using radio-frequency (RF) sputter coating. Sputter coating is a process where a 'target', or source, is bombarded with energetic gas molecules. The gas molecules are ionised by applying a high-voltage bias between the target and a cathode, which forms a plasma. The plasma is localised and confined near the surface of the target by strong electric and magnetic fields generated by a magnetron, which sits underneath the target. The applied voltage between the target and the anode causes the ionised gas molecules to ballistically collide with the target, which consequently ejects atoms. These ejected atoms make their way to the chuck via random walks, eventually depositing on the surface of the substrate.

The cleanroom at VUW is equipped with an HHV Auto500 sputter coater, coupled with an Advanced Energy Cesar 136 600W RF generator. The Auto500 has 3 separate sources, which allows us to deposit three separate materials without venting the chamber. Instrument grade argon (BOC, Ar >99.99%) is used as the processing gas for all of the sputter coating referenced in this thesis. The Auto500 chamber is

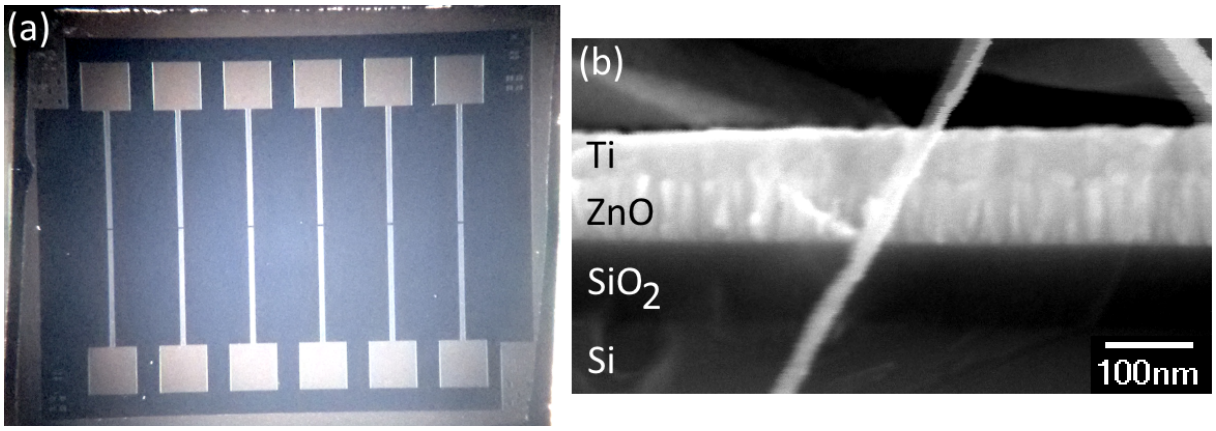

Figure 4.3: (a) A top-down optical image of a lateral substrate. The ZnO/Ti electrodes are clearly defined. (b) A cross-section SEM image of the lateral substrate.

evacuated with an initial roughing pump coupled with a turbomolecular pump.

After the substrates have been patterned using photolithography, the Auto500 sputter coater is used to deposit 100 nm of ZnO (target: 99.99%, Plasmaterials), which serves as the seed layer for nanowire nucleation during the hydrothermal growth. The initial ZnO deposition is followed by a capping layer of Ti (target: 99.99%, Plasmaterials), which can be deposited without venting the chamber due to the multiple sources in the Auto500. The Ti layer covers the surface of the ZnO seed, leaving only the sidewall of the ZnO layer exposed once the excess material is lifted off. It also serves as a contact material for source/drain electrodes. The role of the ZnO seed layer in the hydrothermal growth process is discussed in detail in Chapter 2.

After the Ti layer has been deposited, the substrates are lifted off in a bath of acetone to dissolve the photoresist pattern. This removes the excess material deposited on the photoresist surface, leaving ZnO/Ti on the areas of the substrate where the photoresist was dissolved away during the development step. Sometimes the liftoff process leaves small amounts of residual material at the edges of the patterns, which are removed using brief sonication in acetone or IPA. The substrates are then ready for hydrothermal growth.

Figure 4.3(a) shows an optical microscope image of a substrate post-liftoff. Figure 4.3(b) shows a cross-sectional image taken using SEM of a substrate used for lateral nanowire growth. The Si, SiO_2, ZnO, and Ti layers can be individually be seen on the substrate.

4.3 Fabrication of substrates for vertical nanowire growth

The fabrication of substrates for vertical nanowire growth is significantly simpler than fabricating substrates for lateral nanowire growth. A p^+-Si substrate (Silicon Quest international) is cleaved into 1.1 cm $\times$ 1.1 cm squares, which are consequently cleaned via sonication in acetone and IPA. Because the substrate isn't used for any electrical measurements, the wafers do not require a dielectric layer of SiO_2 on the surface, or any photoresist/PDMS protective layers. Similarly, the exact dopants of the Si wafer do not matter, although we have used p^+-Si wafers out of convenience.

After the substrates have been cleaved, 100 nm of ZnO is deposited via sputter coating, as described in Section 4.2.2 of this chapter. The ZnO film uniformly covers the substrates, as we don't require any photolithographic patterning of the seed layer. After the deposition, substrates coated with the ZnO seed layers are removed from the sputter coater and are ready for use.

4.4 Electrical measurements

Electrical measurements of all the devices contained in this thesis are performed using an Agilent 4156C parameter analyser in conjunction with a Rucker and Kolls probe station. Titanium tri-axial probes are used to make contact to the photolithographically defined pads. Data is retrieved from the parameter analyser using a laptop with an in-house developed Python script. All transfer characteristic measurements involving gate voltage sweeps go from negative to positive to negative, unless otherwise stated. The gate voltage is typically changed in 10 mV increments. Device parameters are extracted from transfer characteristics taken on the upscan or downscan depending on the mode of FET operation. Similarly, the drain-source voltage in output characteristic or diode measurements is swept from negative to positive values. These are also typically measured in 10 mV increments, although diode measurements in Chapter 8 are performed using 1 mV increments.

The rate at which the voltage is swept is determined by the parameter analyser, using a combination of the measurement mode and the magnitude of the drain-source current being measured. For reference, all electrical measurements presented in this thesis are taken in the "Long" measurement mode. The time taken to acquire a measurement of the drain-source current at a specific voltage ranges from 2 seconds (when I_{DS} is in the range of 10 pA) to 0.02 seconds (when I_{DS} is in the range of 10 nA

to 100 mA.) Details of exactly how the integration time is determined can be found in the Agilent 4155C/4156C User's Guide [149].

Similarly, the uncertainties in the applied voltages and measured currents depend on the current/voltage regime used by the parameter analyser. Applied voltages within +/- 2 V have an output resolution of 100 μV, while applied voltages within +/- 20 V have an output resolution of 1 mV, which applies to the majority of measurements presented in this thesis. Applied voltages within +/- 40 V and +/- 100 V have a 2 mV and 5 mV output resolution, respectively.

Uncertainties in the currents measured by the parameter analyser depend both on the magnitude of the current and the integration time, and the relationship is non-trivial. Uncertainties in the measured currents presented in thesis are shown in Table 4.1. These uncertainties only represent the measurement resolution of the parameter analyser, and do not account for other uncertainties which may be introduced by other components of the measurement set-up (such as the capacitive effects of the tri-axial cables, probe/contact effects, etc.) A full and detailed relationship between the measurement resolution, the current range, and the integration time can be found in the Agilent 4155C/4156C User's Guide [149]

Table 4.1: Current measurement resolution of the 4156C parameter analyser

Measurement range	Measurement resolution
10 pA	1 fA
100 pA	1 fA
1 nA	10 fA
10 nA	10 fA
100 nA	100 fA
1 μA	1 pA

Similarly, uncertainties in FET device characteristics extracted from electrical measurements - such as the threshold voltage, transconductance, subthreshold-swing, and electron mobility - are often overlooked in literature, and uncertainty values are very rarely provided. Uncertainties of device parameters are first determined by uncertainties in the electrical measurements, and then compounded by uncertainties in their processing.

For example, threshold voltages are determined by taking the intercept of the linear portion of the drain-source current, and this intercept can be influenced by uncertainties in the drain-source current itself. Similarly, the transconductance is defined

as the maximum value of the derivative of the transfer characteristic measurements. Small amounts of noise in the transfer characteristics can be clearly identified as spurious data, but these small spikes can have very large derivatives. This leads to a certain level of subjectiveness in the definition of the transconductance, as spurious values may have to be discarded by hand. These problems lead to a certain level of uncertainty in the device parameters which is very difficult to accurately quantify.

As such, no specific uncertainties in the device parameters are provided in this thesis, which is in line with published literature in the field. However, some level of uncertainties in these values must be acknowledged. In lieu of specific errors for each value presented in this thesis, it would be prudent to consider the values as having an uncertainty on the order of +/- 5%.

4.5 Scanning electron microscopy

All scanning electron microscopy (SEM) images that are presented in this thesis are taken from a JEOL 6500F at Victoria University. The exact accelerating voltage and other specific parameters vary between images, and are not presented here.

4.6 Transmission electron microscopy

Transmission electron microscopy measurements are presented in Chapters 6 and 7. These measurements were performed by Dr. Jerome Majimel and Uli Castanet at ICMBC Bordeaux as part of a collaboration. Primary and secondary ZnO nanowires were collected from growth substrates by using a scalpel, and then suspended in alcohol by ultrasonication. Drops of the suspension were then deposited onto a copper grid covered with a carbon film. This grid was finally air-dried for 15 minutes. TEM and high resolution TEM observations were performed using a JEOL 2200 FS equipped with a field emission gun, operating at 200 kV and with a point resolution of 0.23 nm. High-resolution transmission electron microscopy micrographs were acquired with a Gatan Ultrascan CCD 2k - 2k and digital diffractograms were calculated using the Gatan Digital Micrograph program. In order to be representative and statistically meaningful, many images from several regions of various samples were recorded, and the most characteristic results are presented here. Due to the thickness of the nanorods, high-resolution TEM observations were almost exclusively performed on the nanorod terminating ends. Only Electron Diffraction (ED) patterns have been recorded all along the nanorods.

Chapter 5

Hydrothermal growth of vertical ZnO nanowires

5.1 Introduction

ZnO nanowires can be easily and reproducibly grown en masse from seeded substrates using the hydrothermal method [48]. The simplicity and scalability of this synthesis route offers significant advantages over comparatively difficult or expensive nanowire synthesis techniques [10]. As described in Chapter 2, nanowires grow approximately normal to the plane of the seeded substrate, giving rise to dense vertical arrays of nanowires from flat substrates. Vertical arrays of ZnO nanowires have already been used in a wide variety of opto-electronic applications, such as solar cells and piezoelectronic power generators [10, 18, 109, 150, 151, 121, 152, 132]. Vertical nanowires can also be removed from the growth substrate, and then used individually for device fabrication.

Whether used individually or as arrays, the nanowire morphology can have a significant impact on device performance. High aspect ratios (the length of the nanowire divided by its width) are often desirable, which places an emphasis on synthesising longer ZnO nanowires without a corresponding increase in diameter. To this end, polyethylenimine (PEI) is a polymer commonly used as an aspect-ratio enhancer in the hydrothermal growth [68, 69, 70, 71, 72, 73, 74], as outlined in Chapter 2. While there are published reports which focus on optimising the PEI concentration to give the longest nanowires [68, 69, 74], there has been comparatively little research on how the molecular weight of the polymer might affect the hydrothermal synthesis.

In this chapter, the effects of using different concentrations and molecular weights of PEI (M_W = 800, 1300, and 2000 g/mol) on the morphology of the nanowires is

investigated. These results are contrasted with a control sample, grown without any PEI. The inclusion of PEI can drastically alter the final hydrothermal product, either etching the growth substrate, depositing a homogeneous thin film of ZnO, growing hierarchical ZnO nanowires, or resulting in homogeneous nanowires. Growth mechanisms for ZnO thin films and for hierarchical ZnO nanowires are put forward. Finally, the length, diameter, and aspect ratios of the homogeneous nanowires are compared. All of the PEI-assisted nanowires are longer than the control nanowires, and also have better aspect ratios. The longest nanowires are grown using 8 mM of PEI(M_W = 800 g/mol), while the highest aspect-ratio nanowires are grown using 6 mM of PEI(M_W = 800 g/mol). These results give valuable information on optimising vertical ZnO nanowire growth for the fabrication of individual field-effect transistors, and the proposed growth mechanism for the hierarchical nanowires is important for the results presented in later chapters.

5.2 Experimental details

Growth substrates were first fabricated by cleaning and cleaving p^+-Si wafers (sourced from Silicon Quest International) into 1 cm $\times$ 1 cm squares. After cleaving, the growth substrates were covered in a 100 nm uniform thin film of ZnO via RF sputtering, to serve as the seed layer for hydrothermal growth of vertical nanowires. The substrates were annealed at 500 °C for 60 minutes in ambient atmosphere using a hotplate. Annealing RF-sputtered thin films of ZnO improves their crystallinity, leading to longer nanowires after the hydrothermal growth [153, 154, 155, 156]. Thorough experimental details for the substrate fabrication are provided in Chapter 4.

In order to independently determine how the concentration and molecular weight of included PEI affects the hydrothermally grown nanowires, all of the other hydrothermal growth variables were kept constant. To this end, each hydrothermal growth was prepared by first making a control solution using 25 mM of $Zn(NO_3)_2$ (Sigma Aldrich, 98% purity) and hexamethylenetetramine (HMT) (Sigma Aldrich, 99% purity) mixed with 250 mL de-ionised (DI) water ($\geq$ 18.2 M $\Omega \cdot$ cm). These control solutions were then mixed with PEI to complete the hydrothermal growth solution. Three different varieties of PEI were used, with molecular weights of 800, 1300, and 2000 g/mol, which are referred to as PEI(800), PEI(1300), and PEI(2000), respectively. Each PEI variety was used at a concentration of 2, 4, 6, and 8 mM. Three separate growth substrates were included in each hydrothermal growth to ensure that the results were reproducible.

After the hydrothermal growth solutions were thoroughly mixed together in

borosilicate glass bottles, they were placed in a waterbath held at 95 °C to preheat for one hour. After the preheat, growth substrates were placed into each hydrothermal growth solution and allowed to grow for 19 hours at 95 °C. The general theory and experimental techniques underpinning the hydrothermal growth of ZnO nanowires is described in detail in Chapter 2. After the 19 hour growth was complete, the substrates were removed from the growth solution and rinsed thoroughly in DI water ($\geq$ 18.2 M $\Omega \cdot$ cm) before being dried with nitrogen at room temperature.

Finally, the hydrothermally grown ZnO nanowires were imaged using a JEOL6500F SEM, also described in Chapter 4. Images were taken at three different locations on each sample to ensure that the imaged nanowires were representative. These locations were intentionally chosen to span the entire length of each sample in cross-section, in order to account for any possible localised variation in the nanowire morphology. The length and diameter of the imaged nanowires were measured using ImageJ. Selection bias was avoided by measuring the dimensions of every nanowire in each SEM image. The uncertainties in these measurements are compounded by the uncertainties introduced by the JEOL6500F, the resolution of the SEM images (as ImageJ measures dimensions on a pixel-by-pixel basis), and human error in using ImageJ. The uncertainties in the nanowire diameters are taken to be +/- 1 nm, while the uncertainties in the nanowire lengths are taken to be +/- 10 nm.

The three separate substrates included within each hydrothermal growth were individually compared using SEM, and in each instance their morphologies were found to be in agreement with one another. This lends credence to the overall reproducibility of the results presented within this chapter. For the sake of brevity, only one sample for each growth condition is presented here.

5.3 Effects of PEI molecular weight and concentration

Vertical ZnO nanowires were first hydrothermally grown without any PEI included in the precursors, to serve as a control. These are shown from a top-down and side-on perspective in Figure 5.1. The nanowires uniformly cover the surface of the substrate, and are relatively normal to its surface. The median diameter of the nanowires is 50 nm, and their median length is 1.46 μm. As stated in the introduction to this thesis, ZnO almost exclusively forms in the hexagonal wurtzite structure, unless grown under very high pressures [12]. This causes the profiles of the nanowires to be hexagonal in cross-section, which is consistent with the literature. The nanowires have grown preferentially and anisotropically in the c-axis direction.

In comparison to the predictable outcome of the control hydrothermal growth, the

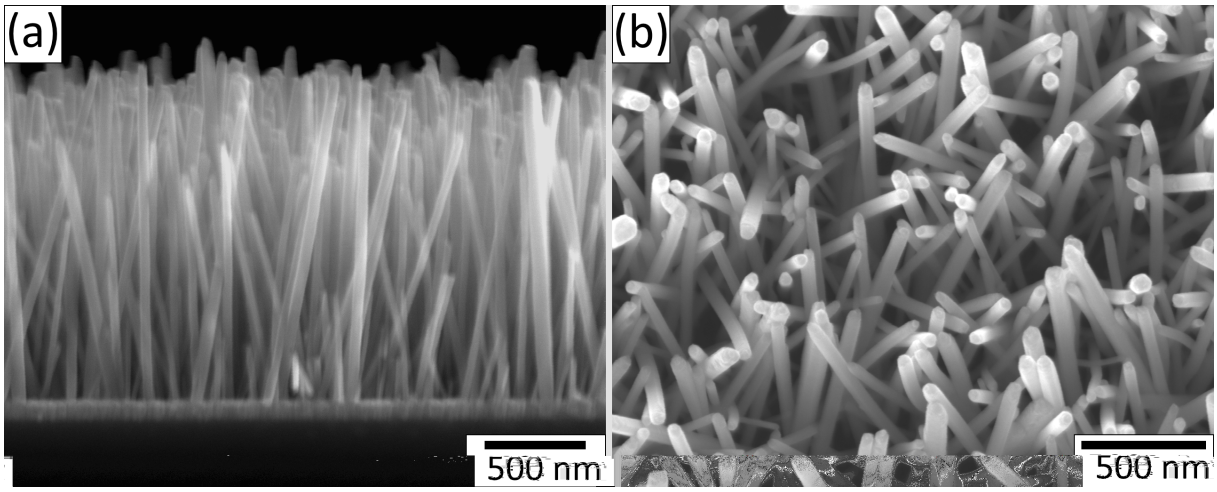

Figure 5.1: Cross-section (a) and top-down (b) SEM images of ZnO nanowires hydrothermally grown without any PEI.

inclusion of PEI in growth precursors can produce a wide variety of different outcomes, depending on the molecular weight and concentration of PEI used. The morphology of the resulting nanowires (or nanocrystals) can vary quite significantly from the regular nanowires grown without PEI, or nanowire growth can be suppressed altogether. Specifically, the results of the PEI-mediated hydrothermal growth can be categorised into the following:

- **Homogeneous nanowires**: Regular nanowires which grow uniformly across the surface of the substrate.
- **Homogeneous hierarchical nanowires**: Hierarchical nanowires which grow uniformly across the substrate surface. These are composed of large, primary nanowires which quickly transition much thinner, secondary nanowires
- **Thin ZnO film**: Rather than growing nanowires, a thin film of ZnO forms over the entire substrate
- **Growth supression**: ZnO nanowire growth is strongly suppressed over the entirety of the substrate, but the seed layer remains intact
- **Substrate etching**: The PEI removes the ZnO seed layer and etches into the silicon substrate

A summary table of the different PEI molecular weights/concentrations and their outcomes are presented in Table 5.1. Examples of these morphologies are given in the following subsections, which describe the effects of the PEI on the hydrothermal growth in detail.

Table 5.1: Summary of results depending on concentration and molecular weight of PEI used in growth.

	PEI(800)	PEI(1300)	PEI(2000)
8 mM	Homogeneous nanowires	Substrate etching	Substrate etching
6 mM	Homogeneous nanowires	Thin film deposition	Substrate etching
4 mM	Growth suppression	Hierarchical nanowires	Thin film deposition
2 mM	Homogeneous nanowires	Homogeneous nanowires	Homogeneous nanowires

5.3.1 PEI(800)

Hydrothermal growths were carried out using 8, 6, 4, and 2 mM of PEI(800) included with the standard $Zn(NO_3)_2$/HMT precursors. SEM images of the nanowires grown using 8 mM and 6 mM of PEI(800) are shown in Figure 5.2 from both a top-down and cross-sectional perspective. The highest concentration of PEI(800) used (8 mM) results in long and thin homogeneous ZnO nanowires, which grow uniformly over the substrate surface. The nanowires are roughly normal to the surface of the substrate, as seen in Figure 5.2(a), although they show some bowing and bending due to their high aspect ratio. The top-down perspective shown in Figure 5.2(b) suggests that the nanowires partially fall into one another due to their length, forming upright bundles. The median length of these nanowires is 10.5 μm, while the median diameter is 89 nm.

Using 6 mM of PEI(800) also results in homogeneous nanowires which more or less uniformly cover the substrate surface, although there are small areas where nanowire growth has been suppressed. The top-down and cross-section images shown in Figure 5.2(c) and (d) respectively suggest that the 6 mM PEI(800) nanowires also collapse into one another and form bundles; the top-down perspective in particular suggests that this happens to a greater extent than the 8 mM PEI(800) nanowires, despite the fact that the aspect ratio of the 6 mM nanowires is lower. The median length of the 6 mM PEI(800) nanowires is 7.98 μm, and the median diameter is 51 nm.

Nanowires grown using 4 mM and 2 mM of PEI(800) are shown in Figure 5.3. Unlike the previous two results, including 4 mM of PEI(800) with the regular precursors in the growth solution strongly suppresses all nanowire growth across the entire sample. Figure 5.3(a) and (b) show cross-sectional and top-down views of the substrate after growth. The seed layer is still visible, but is almost totally devoid of all nanowires. Despite this, there are small, localised patches of the substrate where nanowire growth has taken place, although the growth has been heavily suppressed. An example of such a patch is visible in Figure 5.3(b). The nanowires which grow from these patches are typically 100 to 200 nm in length, with diameters on the order of tens of nanometres. Rather than growing normal to the seed layer, these small nanowires

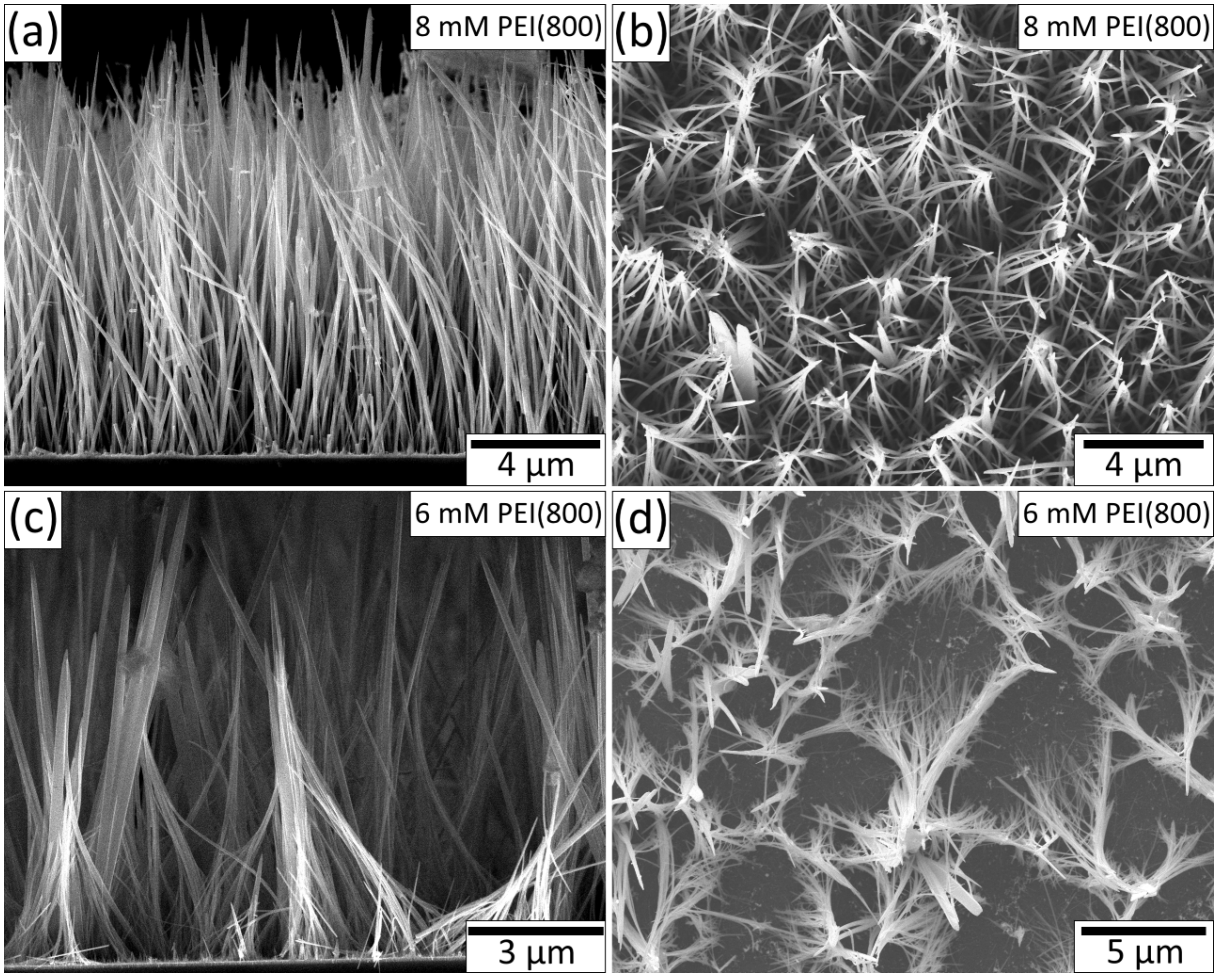

Figure 5.2: (a) & (b): Cross-sectional and top-down SEM images of ZnO nanowires grown using 8 mM of PEI(800). (c) & (d): Cross-sectional and top-down SEM images of ZnO nanowires grown using 6 mM of PEI(800).

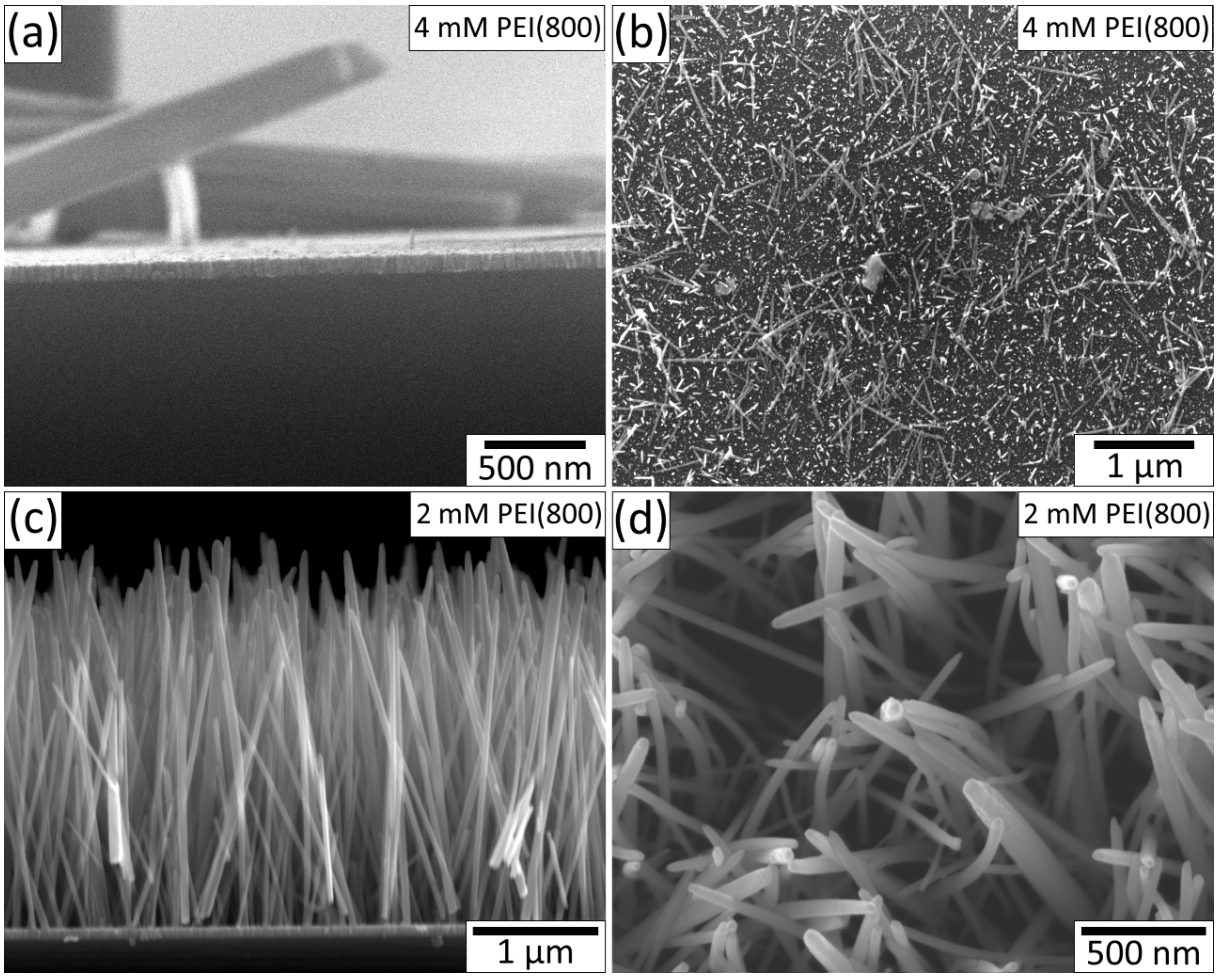

Figure 5.3: (a) & (b): Cross-sectional and top-down SEM images of the sample grown using 4 mM of PEI(800). Nanowire growth has been considerably suppressed. (c) & (d): Cross-sectional and top-down SEM images of ZnO nanowires grown using 2 mM of PEI(800)

lie at random orientations to the substrate.

Finally, nanowires grown using 2 mM of PEI(800) are shown in 5.2(c) and (d). This concentration of PEI results in the growth of homogeneous nanowires normal to the ZnO seed layer, which are uniform across the entire substrate. These nanowires closely resemble the control sample grown without any PEI, although they have better aspect ratios and more desirable dimensions. The nanowires have some variation in their diameter, with the thinner nanowires partially collapsing and forming bundles. The median length of the 2 mM PEI(800) sample is 2.6 μm, and the median diameter is 58 nm.

Although the heavy suppression of nanowire growth at 4 mM of PEI(800) is incongruous with the other results presented here, the results are demonstrably reproducible. Figure 5.4 shows another substrate grown under identical conditions in a sep-

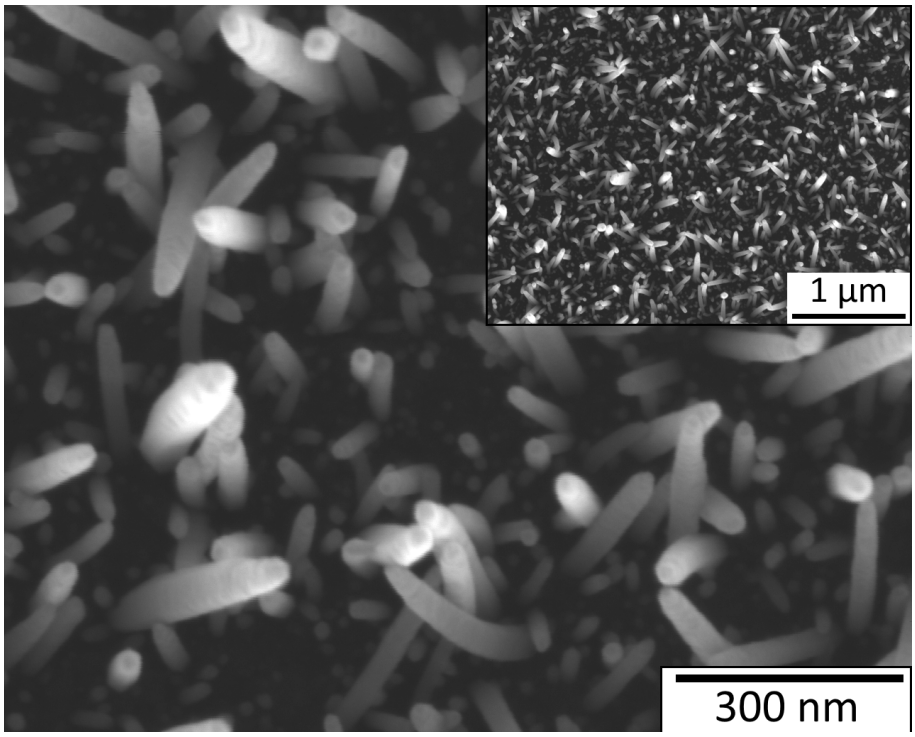

Figure 5.4: Another sample grown using 4 mM of PEI(800). Nanowire growth has been considerably suppressed. The inset shows a lower magnification image of the same sample.

arate growth bottle. Despite the fact that the seed layer is intact, this sample also shows the strong suppression of nanowire growth, suggesting that the growth suppression is a genuine phenomenon at this particular concentration.

5.3.2 PEI(1300)

SEM images of nanowires grown using 8 mM and 6 mM of PEI(1300) are shown in Figure 5.5. The sample grown using 8 mM of PEI(1300), shown in Figure 5.5(a) and (b), shows significant etching from the excessive concentration of PEI. The ZnO seed layer has been totally etched away from the Si substrate, which has in turn been anisotropically etched in the [111] direction. This concentration of PEI is clearly unusable for ZnO nanowire growth.

The sample grown using 6 mM of PEI(1300) is shown in Figure 5.5(c) and (d). Instead of growing ZnO nanostructures, this concentration of PEI causes the growth of a thin film of ZnO uniformly over the seed layer. The original seed layer can be seen as a thin layer at the very bottom of the ZnO film. The thin film is uniform and homogeneous, with little texture to the surface of the film.

Figure 5.6 shows SEM images of the samples grown using 4 mM and 2 mM of PEI(1300). Hierarchical ZnO nanowires are grown when 4 mM of PEI(1300) is included with the regular hydrothermal growth solution. These hierarchical nanowires are shown in cross-section and from a top-down perspective in Figure 5.6(a) and (b). The primary portion of these nanowires resemble regular nanowires synthesised using the hydrothermal growth. However, unlike regular hydrothermally-synthesised nanowires, the tips of these primary nanowires terminate in very fine secondary nanowires which have grown in the c-axis direction. These secondary nanowires can be up to tens of microns long and have diameters smaller than 50 nm. The secondary nanowires collapse due to their very high aspect ratio, forming a lateral network of nanowires which intersects the vertical array of primary nanowires which grow from the substrate.

When 2 mM of PEI(1300) is included in the growth solution, regular homogeneous nanowires grow from the substrate surface, similar to those grown with 2 mM of PEI(800). These nanowires are shown from a cross-sectional and top-down perspective in Figure 5.6(c) and (d). The nanowires have uniformly grown across the substrate surface at a 90° angle. The median length of the nanowires is approximately 2.6 μm, while their median diameter is roughly 50 nm.

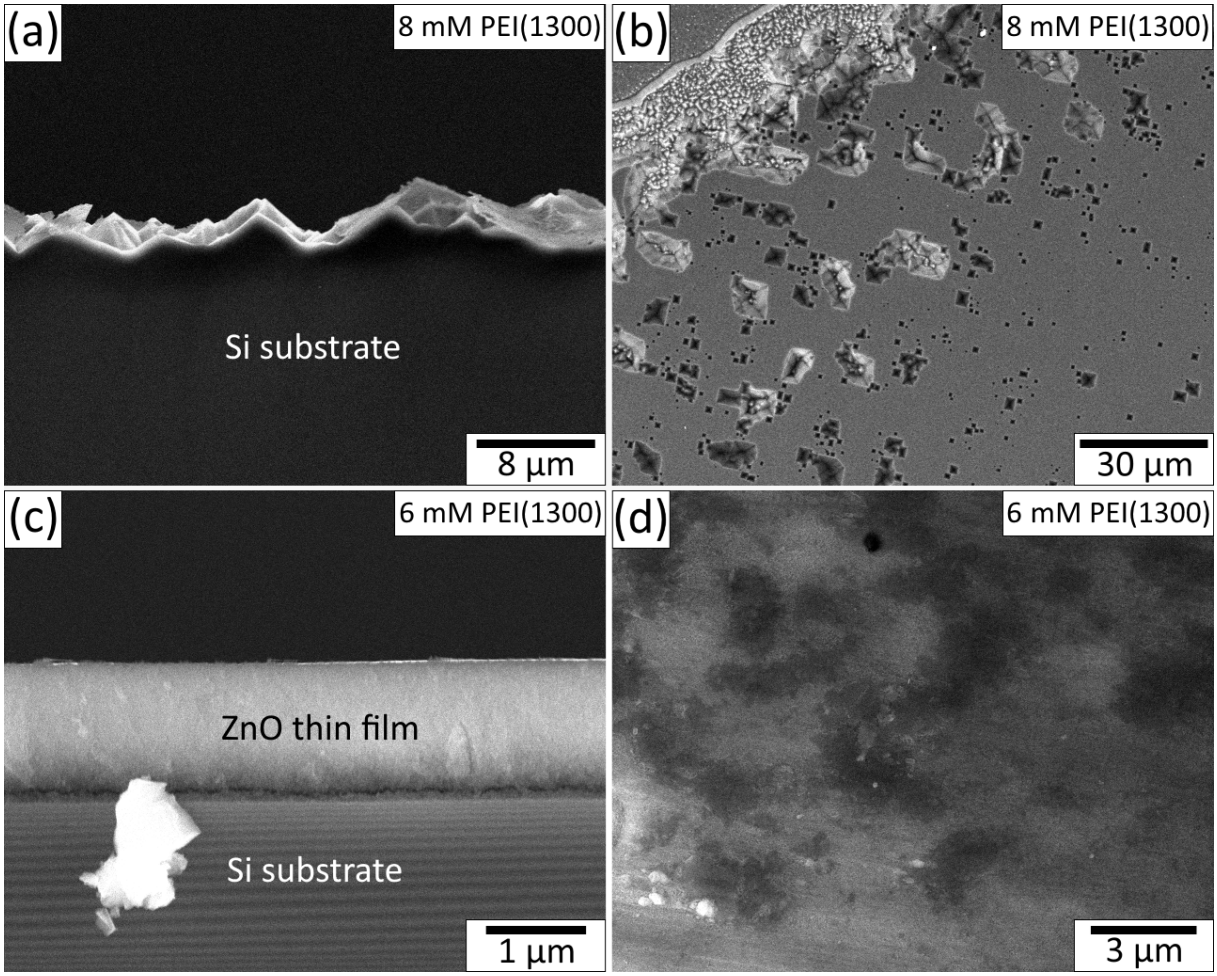

Figure 5.5: (a) & (b): Cross-sectional and top-down SEM images of the sample grown using 8 mM of PEI(1300). The growth substrate has been significantly etched during growth. (c) & (d): Cross-sectional and top-down SEM images of the sample grown using 6 mM of PEI(1300). A homogeneous thin film of ZnO has grown from the seed layer, covering the substrate.

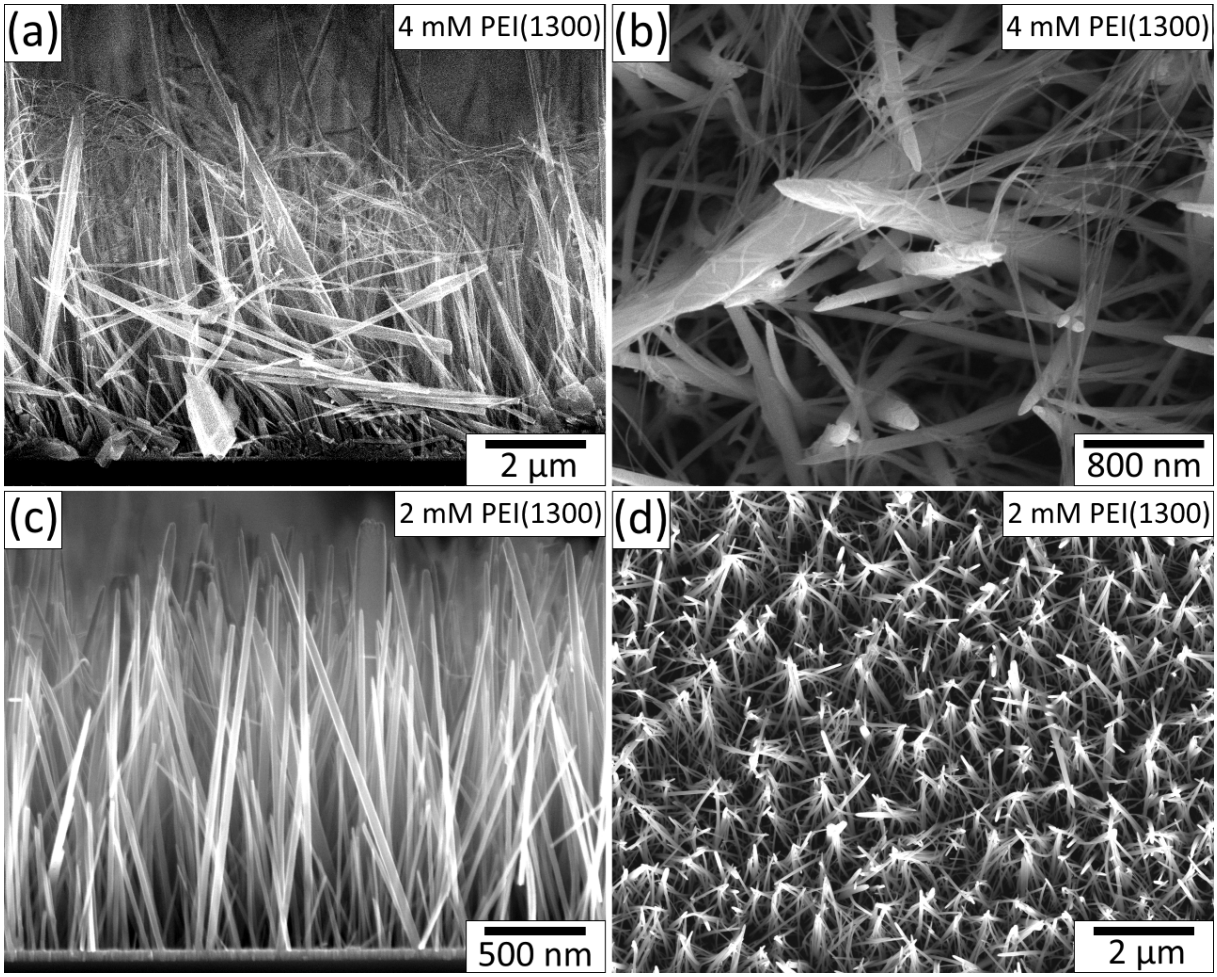

Figure 5.6: (a) & (b): Cross-sectional and top-down SEM images of the nanowires grown using 4 mM of PEI(1300). These ZnO nanowires are hierarchical, with distinct primary and secondary components. (c) & (d): Cross-sectional and top-down SEM images of ZnO nanowires grown using 2 mM of PEI(1300).

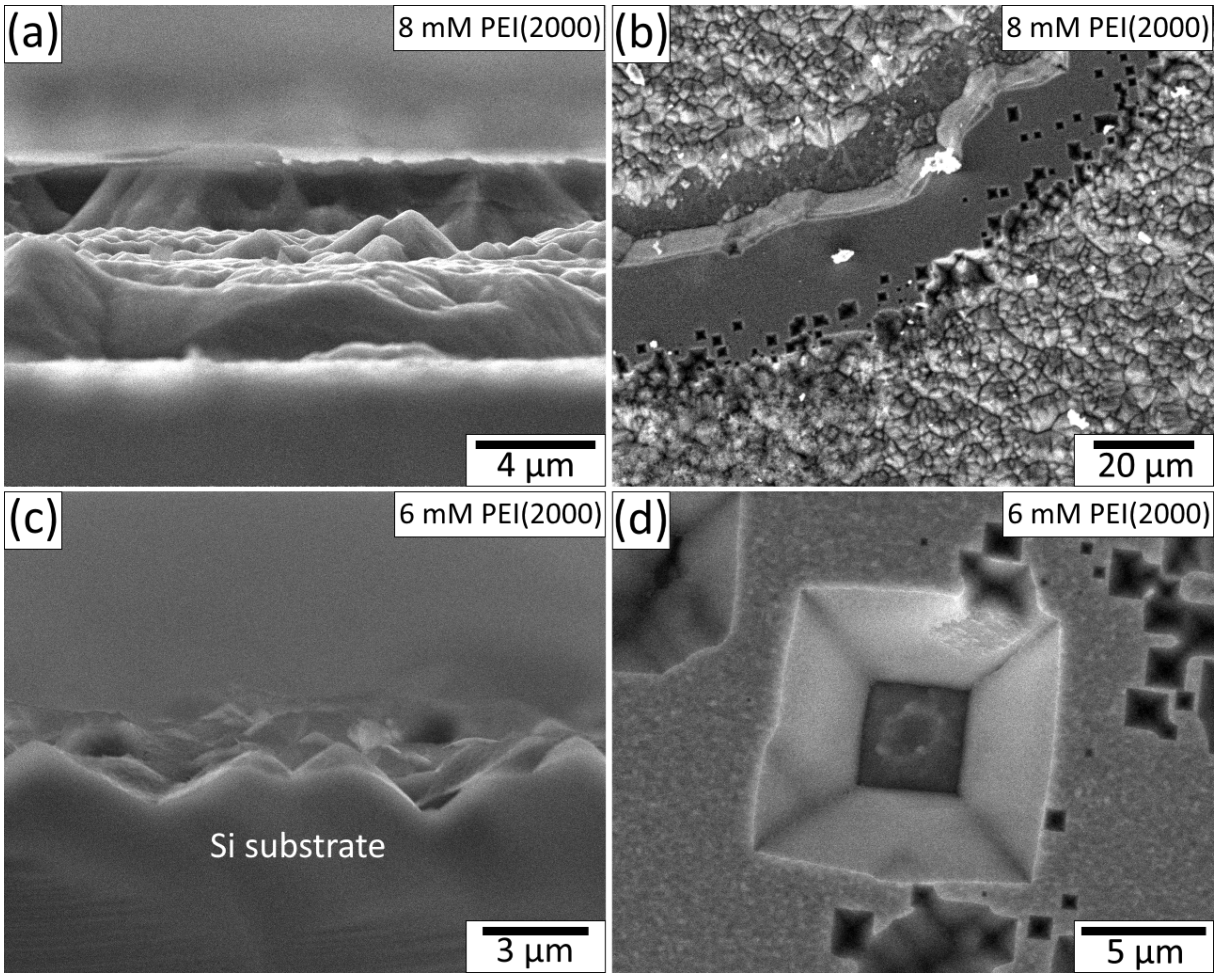

Figure 5.7: (a) & (b): Cross-sectional and top-down SEM images of the nanowires grown using 8 mM of PEI(2000). The PEI concentration has etched the Si growth substrate in the [111] direction. (c) & (d): Cross-sectional and top-down SEM images of ZnO nanowires grown using 6 mM of PEI(2000). This concentration has also etched the Si growth substrate.

5.3.3 PEI(2000)

Samples grown using 8 mM and 6 mM of PEI(2000) are shown in Figure 5.7. When 8 mM of PEI(2000) is included in the hydrothermal growth, the ZnO seed layer originally deposited on the substrates is completely removed and the Si substrate itself is heavily etched. These results are shown in Figure 5.7(a) and (b). The anisotropic etching of the Si substrate in the [111] direction mirrors the results obtained from including 8 mM of PEI(1300), previously shown in 5.5(a) and (b). Unlike the case for PEI(1300), substrate etching is still observed at a lower concentration of 6 mM of PEI(2000), due to the higher molecular weight of the PEI. This is shown from a top-down and cross-sectional perspective in Figure 5.7(c) and (d).

Figure 5.8 shows samples grown using 4 mM and 2 mM of PEI(2000). When 4

mM of PEI(2000) is included in the growth solution, a thin film of ZnO is deposited uniformly across the surface of the substrate, as in Figure 5.8(a) and (b). This result is similar to the thin film obtained by including 6 mM of PEI(1300), which is shown in Figure 5.5(c) and (d). As is the case with the 6 mM PEI(1300) thin film, the 4 mM PEI(2000) thin film doesn't show any kind of texture in its cross-section. However, unlike the film grown using PEI(1300), the 4 mM PEI(2000) thin film does have a textured surface. This texture consists of small circular nodules with diameters on the order of tens of nanometres which are flush with the thin film surface. Small ZnO nanospheres have grown from a portion of the nodules which texture the film surface. These nanospheres protrude from the surface of the film, with diameters comparable to the circular nodules. As these nanospheres sit atop the surface of the film, they have clearly nucleated at the end of the hydrothermal growth, after the bulk of the thin film has been deposited.

Finally, including 2 mM of PEI(2000) into the hydrothermal growth solution results in a homogeneous array of ZnO nanowires which grow vertically from the sputtered ZnO seed layer. These nanowires are shown from top-down and in cross-section in Figure 5.8(c) and (d). The nanowires grow uniformly across the surface of the substrate, similar to the control sample grown without any PEI. The nanowires have an median length of approximately 3.8 μm, and an median diameter of 45 nm. The nanowires have grown normal to the substrate, although their high aspect ratio has caused them to partially collapse into one another, forming upright bundles. When seen in cross-section, it is apparent that the nanowires have some variation in their length, although their diameters are fairly uniform.

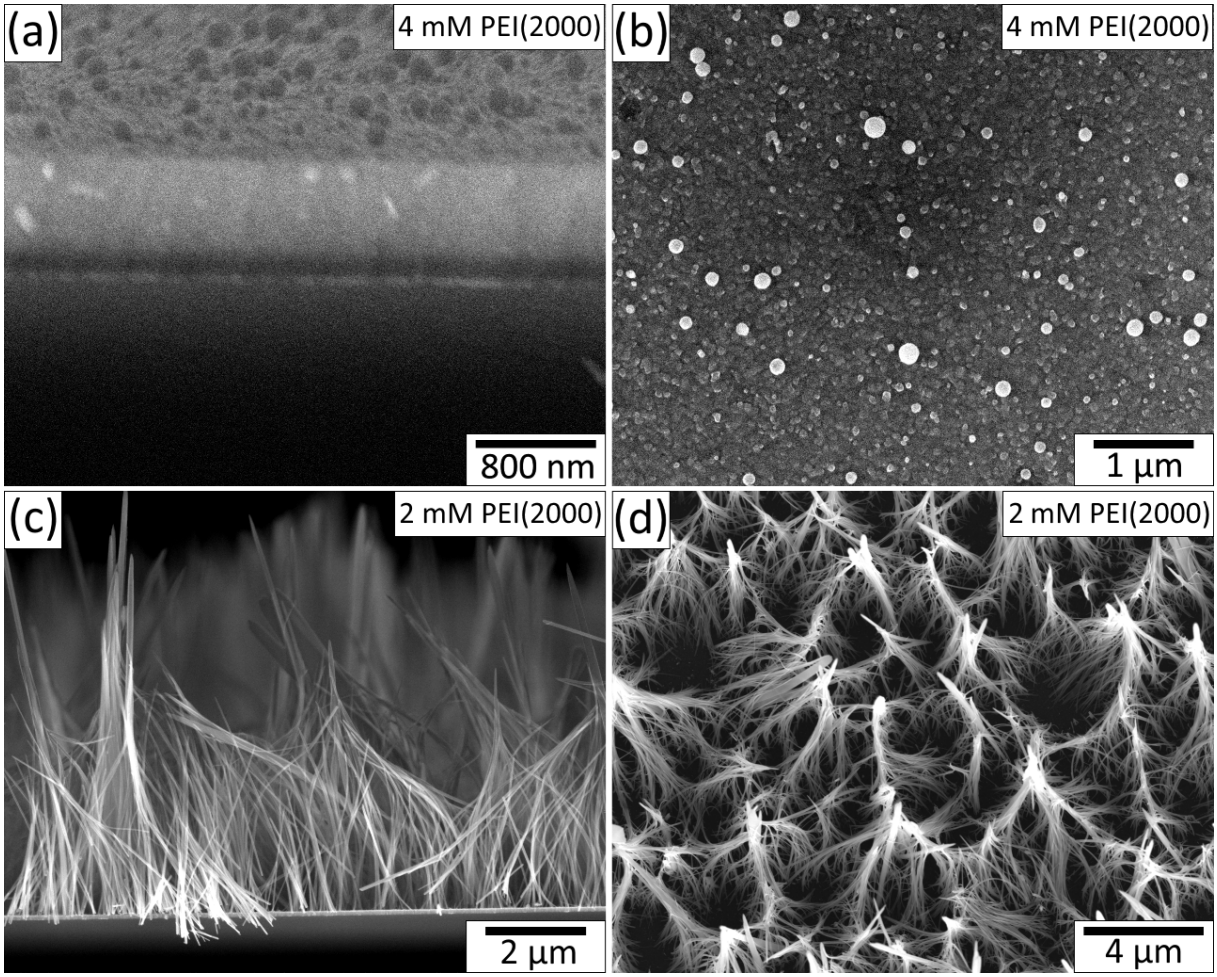

Figure 5.8: (a) & (b): Cross-sectional and top-down SEM images of the sample grown using 4 mM of PEI(2000). A homogeneous thin film of ZnO has grown from the seed layer. (c) & (d):Cross-sectional and top-down SEM images of ZnO nanowires grown using 2 mM of PEI(2000).

5.4 Influence of PEI on morphology

As shown in the previous section, including PEI with the standard growth precursors can cause the morphology of the hydrothermal growth products to significantly deviate from homogeneous nanowires. Specifically, we observe thin films of ZnO when 6 mM of PEI(1300) or 4 mM of PEI(2000) is included in the growth solution, and hierarchical ZnO nanowires when 4 mM of PEI(1300) is included. These unusual morphologies are not seen when standard growth precursors are used in the absence of PEI, and the control sample shows the predictable homogeneous nanowires one would expect from a hydrothermal growth.

5.4.1 ZnO thin film growth mechanism

Hydrothermally synthesised thin films of ZnO have been reported in a number of publications over the past few decades [157, 158, 159, 160, 161, 162, 163, 164]. Thin films typically arise when ZnO nanowires grow towards one another in non-axial directions, coalescing into large agglomerates and eventually forming an uninterrupted film. This process is depicted schematically in Figure 5.9. Nanowires can nucleate and grow spatially separated, eventually coalescing as the gaps between neighbouring nanowires grow smaller and smaller, as in Figure 5.9(a). Alternatively, the nanowires can nucleate in very close proximity and grow side-by-side, forming a continuous film from the beginning of the nanowire growth, as in Figure 5.9(b). A transition from regular nanowire growth to coalescence and thin film formation usually occurs when axial growth is suppressed or restricted in favour of non-axial growth. Although PEI usually encourages axial growth and restricts non-axial growth, we have synthesised clear and reproducible thin films of ZnO when using 6 mM of PEI(1300) or 4 mM of PEI(2000).

Further evidence for this growth mechanism is shown in Figure 5.10. This nanowire sample is grown at a slightly reduced concentration of 3 mM of PEI(2000), along with the regular 25 mM of standard $Zn(NO_3)_2$/HMT. This sample has grown inhomogeneously, with growth totally suppressed at some areas of the growth substrate. Other portions of the substrate have given rise to broad, flat-faced nanowires which are orientated roughly normal to the ZnO seed layer. These nanowires have grown in very close proximity to one another, partially overlapping one another and forming a rough and uneven thin film. The structure of the uneven film is highlighted by imaging the sample in cross-section, shown in the inset to Figure 5.10. Thin film formation has progressed one step further in some areas of the substrate, where nanowires have coalesced into extremely flat and even thin films. These thin films are untextured and homogeneous, and are directly comparable to the thin films synthesised with 4 mM of PEI(2000) and 6 mM of PEI(1300), as shown in Figures 5.8 and 5.5, respectively. This strongly suggests that a similar coalescence mechanism is responsible for the growth

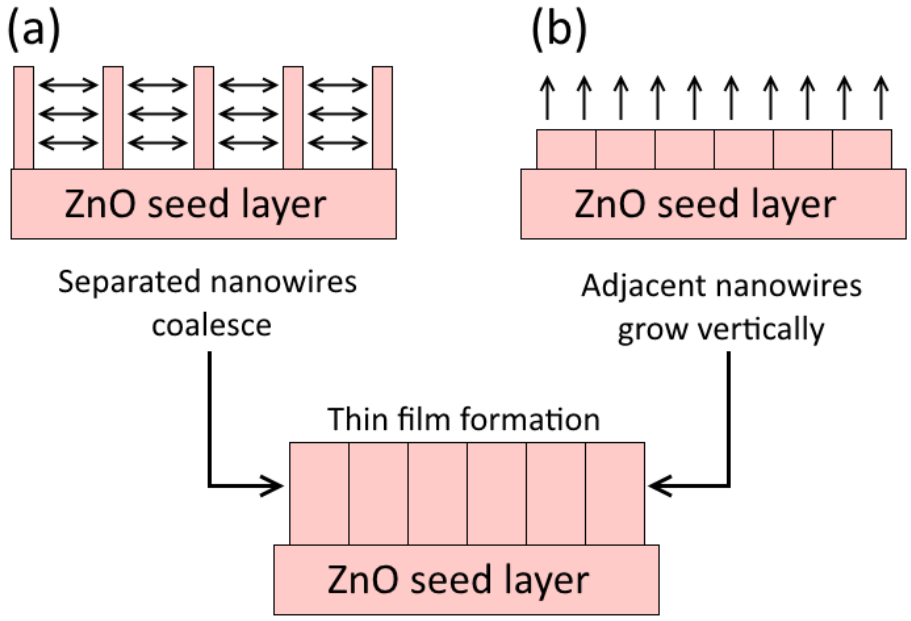

Figure 5.9: A schematic depiction of the hydrothermal growth of a thin film of ZnO. Thin films can either start (a) as separated ZnO nanowires which coalesce, or (b) as adjacent nanowires which grow vertically.

of the thin films studied here, although it is not clear exactly how the PEI mediates this non-axial growth.

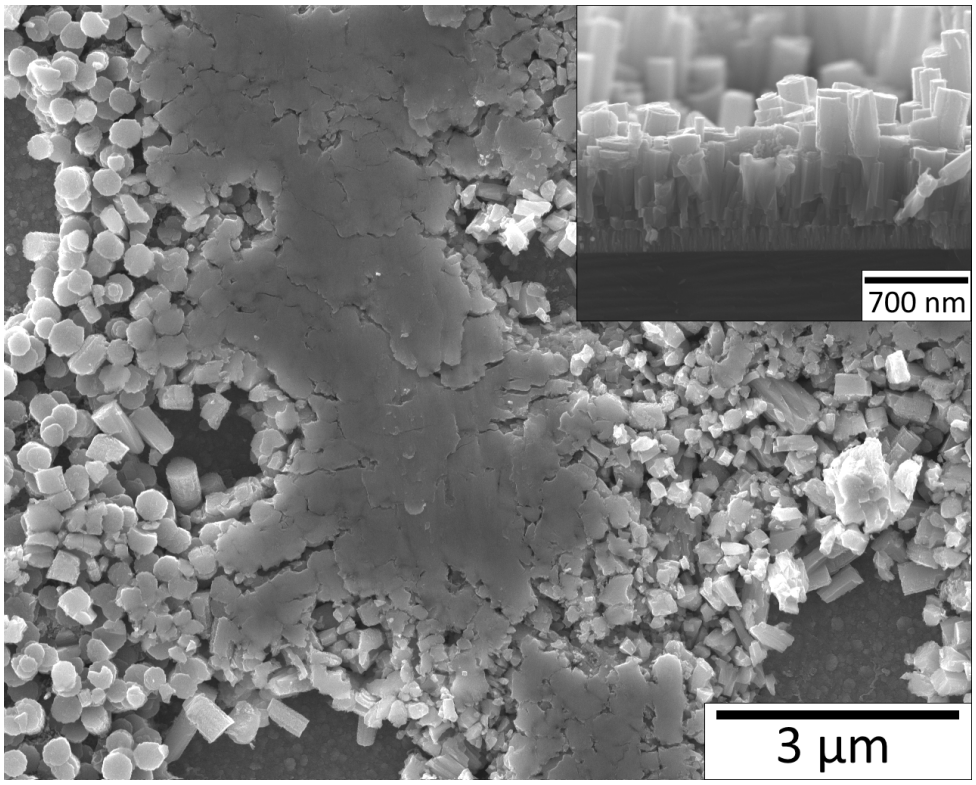

Figure 5.10: A sample grown using 3 mM of PEI(2000). Large adjacent ZnO nanowires have grown vertically, forming a rough thin film (shown cross-sectionally, inset). Portions of the substrate have gone on to grow homogeneous flat films, as depicted in the middle of the image.

5.4.2 Hierarchical nanowire growth mechanism

When 4 mM of PEI(1300) is included in the hydrothermal growth solution, hierarchical nanowires grow vertically from the ZnO seed layer. These hierarchical nanowires consist of comparatively large primary nanowires which abruptly transition into significantly thinner and longer secondary nanowires. The c-axis of the primary and secondary nanowires are aligned, and both share the same axial direction. Arrays of hierarchical nanowires have previously garnered significant interest due to their potential applications in a wide variety of devices [165, 166, 167, 168, 169, 170, 171, 172, 173, 174], although most of the hierarchical nanowires are not co-aligned along the c-axis. Hierarchical nanowires are especially useful in situations where a high surface area is required, such as dye-sensitised solar cells, or where a large degree of interconnectivity between nanowires is required [165, 166, 168, 169, 170, 171, 172, 174].

However, most of the previous reports on the synthesis of hierarchical nanowires use two separate and distinct growth steps, where the primary nanowires are grown in the initial step, and the secondary nanowires are grown in a separate second step. In comparison, the hierarchical nanowires shown here are grown in a single hydrothermal growth. Due to the distinct differences between the primary and secondary nanowires, and the fact that the secondary nanowires clearly grow after the primary nanowires have finished growing, we can conclude that the single hydrothermal growth consists of two distinct growth phases, both of which must be mediated through PEI.

As outlined in Chapter 2, PEI plays a complex role in the hydrothermal growth. In addition to possibly binding to the non-polar facets of ZnO nanowires during the hydrothermal growth, PEI strongly chelates with Zn^{2+} ions in solution [75]. The chelated Zn^{2+} ions ions are gradually released back into the growth solution by PEI-Zn complexes interacting with formaldehyde via a Mannich reaction [75]. These reactions provide another source of Zn^{2+} ions for continued nanowire growth which is otherwise absent when PEI is not included in the growth solution [75]. The formation of hierarchical nanowires suggests that this PEI-mediated source of Zn^{2+} allows for further nanowire growth after other Zn^{2+} sources have been exhausted, which allows for the growth of secondary nanowires.

The hierarchical growth process is depicted schematically in Figure 5.11. Zn^{2+} ions, initially provided by the $Zn(NO_3)_2$ precursor, directly and indirectly crystallise into primary nanowires, as shown in Figure 5.11(a). Once these initial precursors have been consumed, the PEI-chelated Zn^{2+} ions are the only source of Zn^{2+} available.

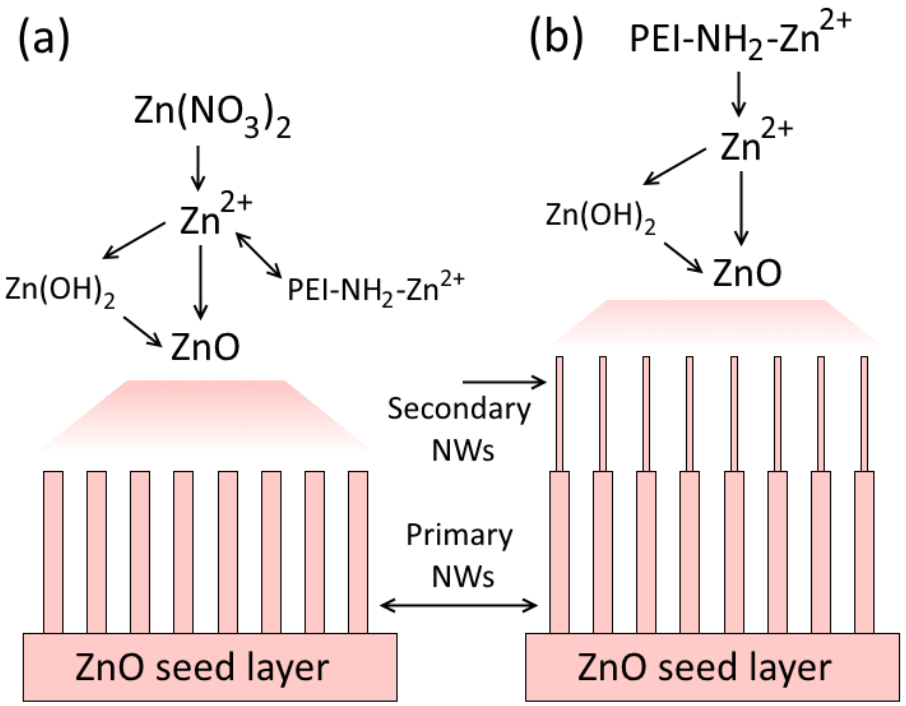

Figure 5.11: A schematic depiction of the growth mechanism of hierarchical ZnO nanowires. (a) The primary nanowires are grown through direct and indirect ZnO crystallisation from numerous Zn^{2+} ion sources. (b) After the primary ZnO nanowires have grown, a comparatively slow PEI-mediated Zn^{2+} ion source causes further growth of the nanowires. The difference in Zn^{2+} concentration causes the secondary nanowires to have a much smaller diameter than the primary nanowires.

These ions in turn directly and indirectly crystallise into secondary nanowires, depicted in Figure 5.11(b). The difference in diameters between the primary and secondary nanowires can be explained by the significantly reduced concentration of Zn^{2+} in the growth solution once the bulk of ions have been consumed. The chemical interactions between the precursors within the growth solution are thoroughly explained in Chapter 2, in addition to the direct and indirect routes of ZnO crystallisation.

Further evidence for the PEI-mediated growth mechanism of secondary nanowires can be seen in cases where the PEI has been inhomogeneously distributed throughout the hydrothermal growth solution. Although every effort is made to thoroughly mix the PEI into the growth solution, agglomerates and clumps can form as the polymer settles in the bottle. These agglomerates can then deposit on the substrate or vertical nanowires during the growth. In some cases, the deposited PEI agglomerates lead to highly localised secondary nanowire growth, causing portions of otherwise homogeneous nanowires to grow as hierarchical nanowires.

Examples of localised hierarchical nanowire growth are shown in Figure 5.12. Figure 5.12(a) and (b) show a portion of a sample grown using 2 mM of PEI(800). An amorphous agglomerate of PEI rests on the surface of the nanowire array indicated by an arrow, in the centre of the image. Secondary nanowires have grown from the tips of the regular nanowires which are nearby the agglomerate, as shown in Figure 5.12(b). Part of the PEI agglomerate is visible in the upper-right corner of the image. Likewise, Figure 5.12(c) and (d) show localised secondary nanowire growth from a sample grown using 5 mM of PEI(800). The PEI agglomerate is located near the top of the image, and indicated with an arrow. Figure 5.12(d) shows the edge of the localised secondary nanowires, where there is a clear transition from hierarchical and regular vertical nanowires. These samples strongly suggest that PEI-chelated Zn^{2+} ions reintroduced into the growth solution are responsible for secondary nanowire growth.

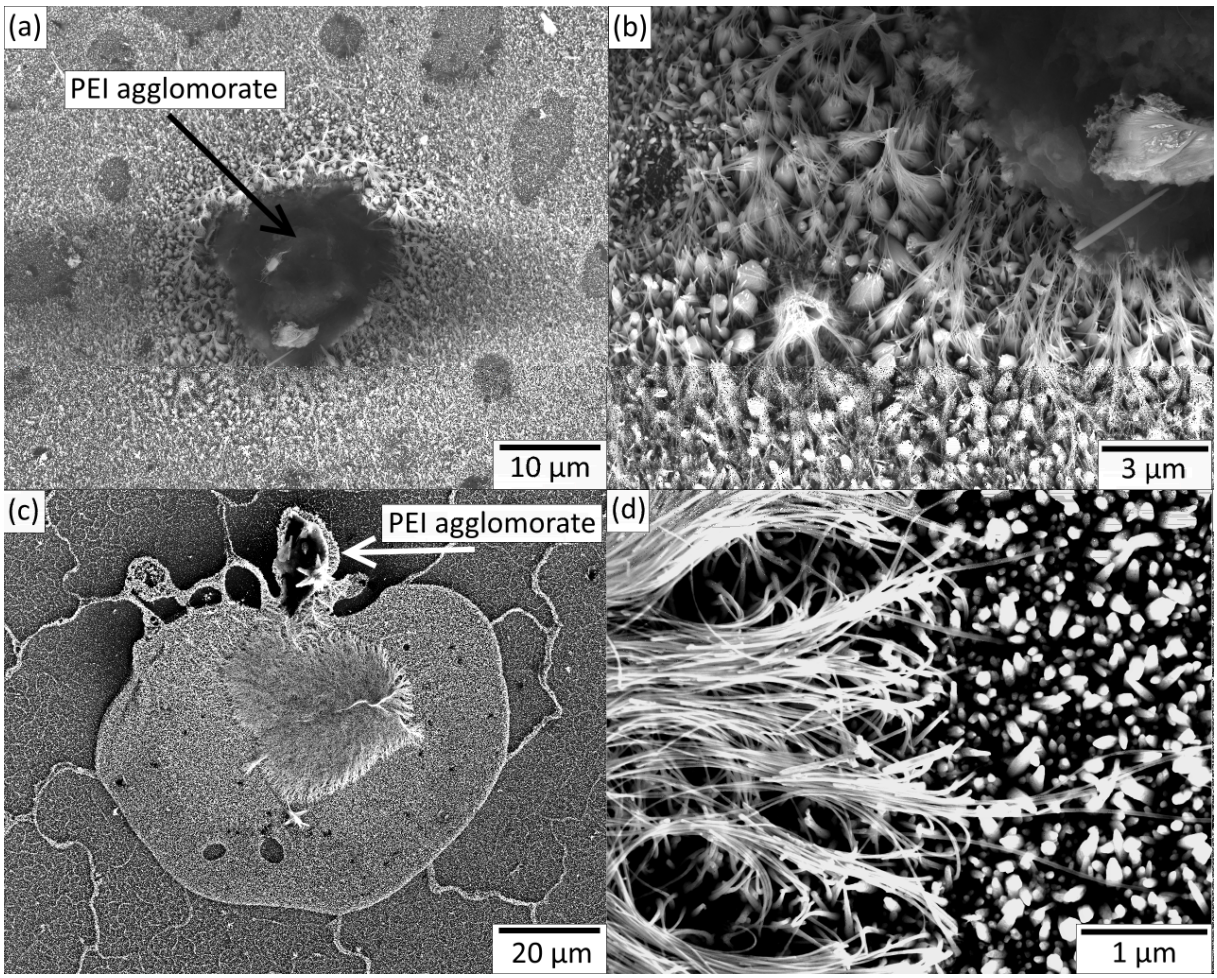

Figure 5.12: Localised secondary nanowire growth caused by agglomerations of PEI. (a) & (b) show a sample grown using 2 mM of PEI(800), while (c) & (d) show a sample grown using 5 mM of PEI(800). The hierarchical nanowires caused by the agglomerated PEI are clearly demarcated from the rest of the nanowires, which are homogeneous.

5.5 Comparison of homogeneous nanowires

As seen in the control sample shown in Figure 5.1, homogeneous nanowires grow when PEI is omitted from the hydrothermal growth solution. Homogeneous nanowires are also grown when 2 mM of PEI(2000) or PEI(1300) is included in the growth solution, or when PEI(800) is included over a range of concentrations. Generally speaking, longer, thinner nanowires are preferable to shorter, wider nanowires, and PEI is primarily used in the hydrothermal growth to increase their aspect ratio. To compare the effects of PEI on the length and diameter of homogeneous nanowires, SEM images of nanowires grown at different concentrations and molecular weights were taken and measured using ImageJ.

Figure 5.13 shows a box and whisker plot of the measured lengths of all of the homogeneous nanowires grown in this chapter, including the control nanowires grown without PEI. This graph shows the lengths of the individual nanowires measured (marked as diamonds on the graph), and the median length, represented by the centre line of each box. The upper and lower bounds of each box represent the upper and lower quartiles of the measurements, indicating the variation observed across the measured nanowires. The values of the median lengths are shown in the upper-right inset.

Homogeneous nanowires grown using 8 mM of PEI(800) (black) are the longest on median, with a median length of 10.5 μm. However, they also show the largest variation in length, with some nanowires being several microns shorter than the median. Nanowires grown using 6 mM of PEI(800) (red) are slightly shorter on median, with a median length of 7.9 μm. Their variation is comparable to nanowires grown using 8 mM of PEI(800), although the standard deviation in length is slightly smaller. In comparison, nanowires grown with 2 mM of PEI(800) (blue) are significantly shorter, with a median length of 2.6 μm. The variation in length is significantly reduced compared to nanowires grown using higher concentrations of PEI(800), with the majority of measured nanowires falling within +/- 0.5 μm of the median.

Nanowires grown using 2 mM of PEI(1300) (magenta) are directly comparable in length to those grown with 2 mM of PEI(800), also having a median length of 2.6 μm. However, they show a higher degree of variation in their length, with some nanowires differing from the median by +/- 1 μm. Nanowires grown with 2 mM of PEI(2000) (green) are measurably longer on median, with a median length of 3.8 μm. These nanowires also show a higher degree of variation in their length, with some nanowires differing from the median by +/- 2 μm. However, this variation is still

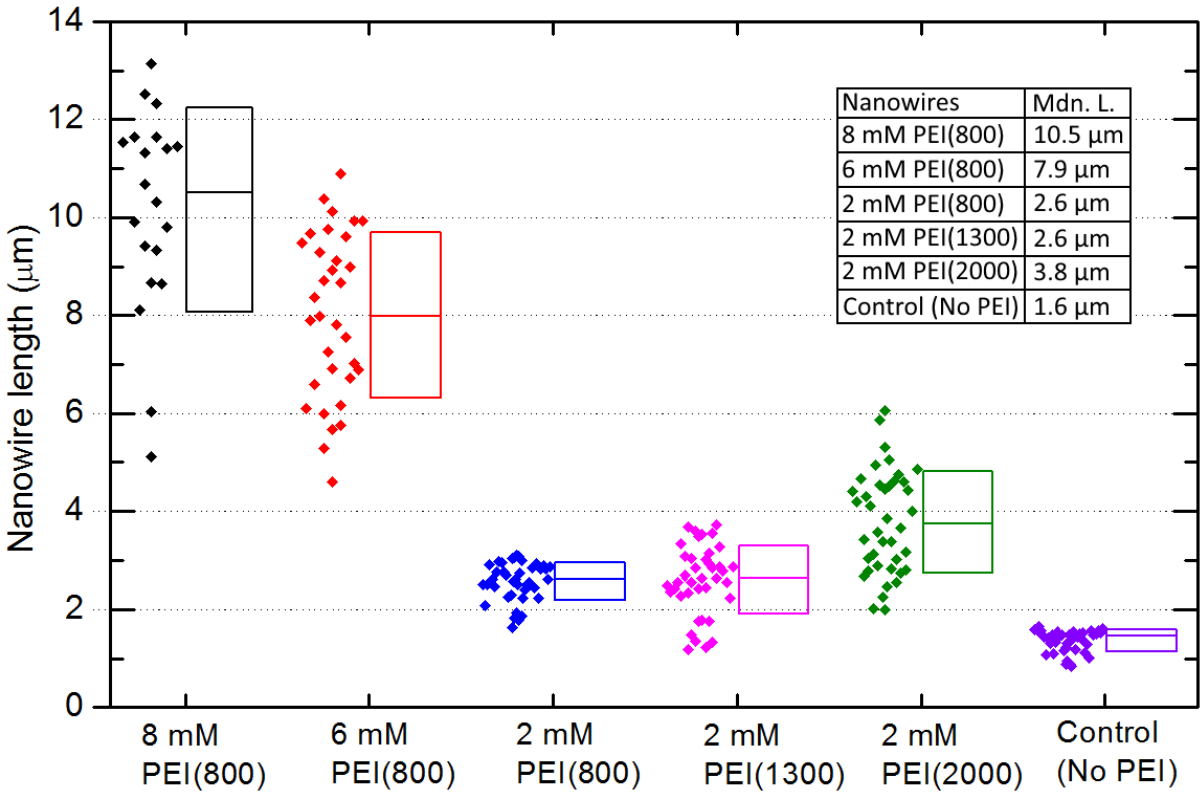

Figure 5.13: Lengths of homogeneous nanowires. Individual measurements are shown as coloured symbols. The median of each recipe is indicated by the centre line of the box graph, while the upper and lower lines of the box indicate the upper and lower quartiles. The median length of each recipe is shown in the upper-right of the graph.

significantly lower than the nanowires grown using 8 mM and 6 mM of PEI(800). Finally, the control sample grown without PEI (purple) has the shortest nanowires, with a median length of 1.6 μm. These nanowires also have the smallest degree of variation in length out of all those studied here, with the large majority of nanowires falling within +/- 0.25 μm of the median.

Figure 5.14 shows the measured diameters of the homogeneous nanowires studied here, following the same convention as Figure 5.13. The median values of the diameters are shown in the upper-right inset, along with the median aspect-ratios (defined as the median length of each nanowire divided by the median width.) Nanowires grown with 8 mM of PEI(800) (black) have a median diameter of 89 nm, and the majority of the nanowires fall within +/- 25 nm of this value. In comparison, nanowires grown using 6 mM of PEI(800) (red) are narrower on median, with a median diameter of 52 nm. The nanowire diameters show a considerably asymmetric variation about the median, with the upper quartile reaching 126 nm. The majority of the thinner nanowires fall within 25 nm of the median.

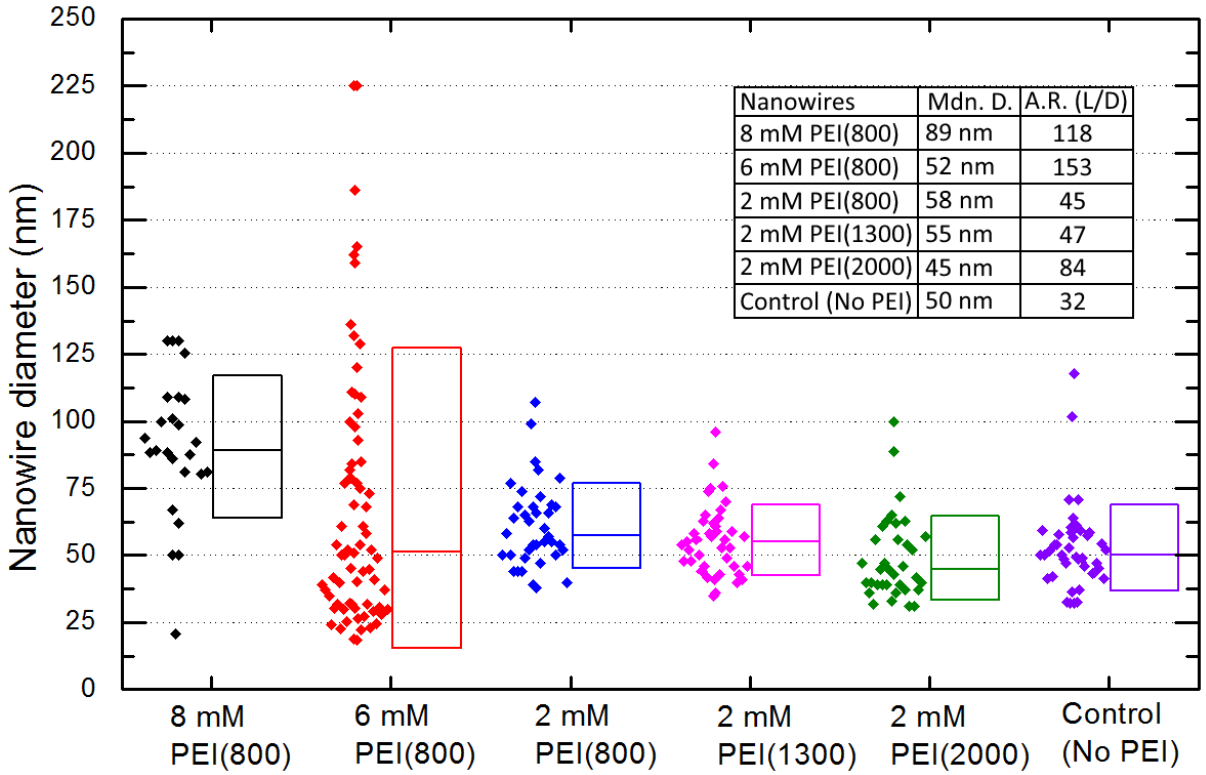

Figure 5.14: Diameters of homogeneous nanowires. Individual measurements are shown as coloured symbols. The median of each recipe is indicated by the centre line of the box graph, while the upper and lower lines of the box indicate the upper and lower quartiles. The median diameter of each recipe is shown in the upper-right of the graph, along with the median aspect ratio (taken as the median length divided by the median diameter.)

Nanowires grown using 2 mM of PEI(800) (blue) have a slightly wider diameter on median than those grown using 6 mM, with a median diameter of 58 nm. The variation in diameter is fairly restricted, with most nanowires falling within +/- 25 nm of the median. The diameters of the nanowires grown using 2 mM of PEI(1300) (magenta) and PEI(2000) (green) are very similar, with median diameters of 55 and 45 nm, respectively. These are comparable to the median diameter of the control sample (purple), which is 50 nm. All of the nanowires grown using 2 mM of PEI have a similar degree of variation in diameter to the control sample, despite the different variations in their length.

5.5.1 Summary

The above results indicate that all varieties of PEI produce nanowires with higher aspect ratios than regular nanowires grown without, provided the concentration of PEI causes homogeneous nanowires to grow in the first place. Different concentrations and molecular weights of PEI can be chosen to suit the requirements of the nanowire morphology. For example, in the hypothetical case where the length of the nanowires is the most important variable, using 8 mM of PEI(800) in the nanowire growth is clearly ideal. However, if a high aspect ratio is prioritised, then growing nanowires using 6 mM of PEI(800) is preferred. If a minimal diameter is preferred over both length and aspect ratio, then 2 mM of PEI(2000) is the ideal concentration and molecular weight of PEI to include in the growth.

Variations in the diameters and lengths of the nanowires may be important as well, depending on their applications. Nanowires grown at 8 mM and 6 mM of PEI(800) clearly show the most variation in both length and diameter, with 8 mM of PEI(800) causing the most variation in the length of the nanowire, and 6 mM of PEI(800) causing the most variation in diameter. Conversely, minimal variation in the diameters and lengths of the nanowires are seen when using low concentrations of PEI, or omitting PEI entirely. All of these variables must be carefully weighed and considered when choosing what PEI to use, depending on the requirements and applications of the final ZnO nanowires.

5.6 Conclusion

In conclusion, the molecular weight of the PEI used in the nanowire growth process is of critical importance, despite often being overlooked. Different molecular weights of PEI can produce drastically different results, even when used at identical concentrations. Excessively high concentrations of high molecular weight varieties of PEI can etch and destroy the growth substrate, and are unsuitable for nanowire growth. Specifically, 8 mM and 6 mM of PEI(2000) etches the Si growth substrates in the [111] direction, as does 6 mM of PEI(1300).

Different molecular weights and concentrations of PEI can also result in irregular nanostructures, which differ significantly from regular homogeneous nanowires grown without PEI. Homogeneous thin films of ZnO are grown at 4 mM of PEI(2000) and 6 mM of PEI(1300), which are caused by large nanowires coalescing together. Hierarchical nanowires are grown at 4 mM of PEI(1300), which have distinct primary and secondary nanowire components. The primary nanowires resemble regular

homogeneous nanowires, transitioning into ultra-thin secondary nanowires. These secondary nanowires are grown through a PEI-mediated source of Zn^{2+} ions which are still present in the growth after the bulk of ions have been consumed.

Homogeneous nanowires are grown at 8 mM, 6 mM, and 2 mM of PEI(800), and at 2 mM of PEI(1300) and PEI(2000). All of these nanowires have higher aspect ratios than nanowires grown without any PEI. The ideal concentration of PEI depends on the requirements of the nanowires. The longest on average nanowires are grown using 8 mM of PEI(800), with a median length of 10.5 μm. The thinnest on average nanowires are grown using 2 mM of PEI(2000), with a median diameter of 45 nm. Finally, the highest aspect-ratio nanowires are grown using 6 mM of PEI(800), with a median aspect ratio of 153.

Chapter 6

PEI-mediated growth of hierarchical ZnO nanowire FETs

While hydrothermal ZnO nanowires have been used in field-effect transistors (which are reviewed extensively in Chapter 3), they are typically field-independent when used as-is due to excessive charge carrier concentrations caused by unintentionally incorporated electron donors. This can be addressed by annealing the nanowires at high temperatures (typically $\geq$400°C) [113, 114, 118, 54, 106, 11, 93] at the expense of losing the advantage of low-temperature synthesis. With future electronics trending towards the use of delicate substrates [175], low-temperature processes will be necessary for fabricating devices at the wafer scale. Further development of ZnO nanowire FETs will therefore benefit from being able to synthesize field-dependent nanowires in situ, whilst also taking full advantage of low-temperature processing and device fabrication [118].

As we have seen in Chapter 5, the hydrothermal growth can be significantly affected by including different concentrations and molarities of PEI. Motivated by these previous results, lateral ZnO nanowires are grown using a range of different concentrations and molecular weights of PEI. A portion of these recipes yield distinctly hierarchical primary/secondary ZnO nanowires, similar to the hierarchical morphology reported in Chapter 5. Significantly, these secondary nanowires are field dependent in their as-grown state, and do not require post-growth annealing or processing before use. This is in direct contrast to the primary nanowires, which are unresponsive to applied fields. Several FETs are fabricated by growing hierarchical nanowires which bridge ZnO/Ti electrodes. All of the FETs fabricated with secondary nanowires show good device performance, with on-off ratios of 10^3 to 10^5 and threshold voltages between -7.5 V to 5 V . Transmission electron microscopy shows the secondary nanowires hierarchically nucleate from the larger ZnO nanorods, with both sharing a common c-axis. Persistent photoconductivity measurements suggest

that depleting surface states on the nanowires play a significant role in determining the threshold voltage of the devices.

6.1 Motivation and background

In order to use ZnO nanowires in field-effect transistors, they must first be synthesised on a growth substrate, and then electrically contacted on an appropriate FET device substrate. While the hydrothermal synthesis of ZnO nanowires is rapid and scalable, making electrical contact to the nanowires poses a challenge. One method of electrically contacting nanowires is to initially grow them on a dedicated substrate, transfer them to a separate device substrate, and then perform electron beam lithography to pattern a resist for metallisation, as described in Chapter 8. However, this contacting process is resource-intensive and laborious, and cannot be effectively scaled up to higher throughputs.

A solution to this problem is to use a ZnO nanowire growth substrate which also doubles as the FET device substrate. This is most easily accomplished by synthesising intersecting lateral networks of ZnO nanowires from patterned seed layers, as described in Section 2.5.3 in Chapter 2. The patterned seed layers consist of thin ZnO films which are capped with Ti. Only the sidewall of the ZnO layer is exposed during the hydrothermal growth due to the Ti capping layer, which restricts the nanowires to grow laterally from the sidewall and parallel with the substrate. The ZnO/Ti layers are patterned in pairs, which are separated by a small gap on the order of tens of microns. Lateral ZnO nanowires intersect in the middle of this gap, which forms the FET channel. The Ti capping layers can then be electrically contacted as drain and source electrodes, and current passed through the intersecting wires. The entire SiO_2/Si substrate can then be used as a global back gate to switch the FET on and off. A thin layer of Cr/Au ($\approx$ 5/50 nm) is typically applied to the back of the substrate to improve electrical contact to the Si bulk. The architecture of the final device is shown in Figure 6.1.

Nanowires can be hydrothermally grown with or without using polyethylenimine (PEI), as described in Chapter 2. In Chapter 5, it was shown that varying the molecular weight and concentration of PEI in the growth solution can drastically affect the nanowire morphology. Three different molecular weights are of PEI are used (M_W = 2000 g/mol, 1300 g/mol, and 800 g/mol) at a variety of concentrations to grow lateral nanowires, and to assess their viability as FETs.

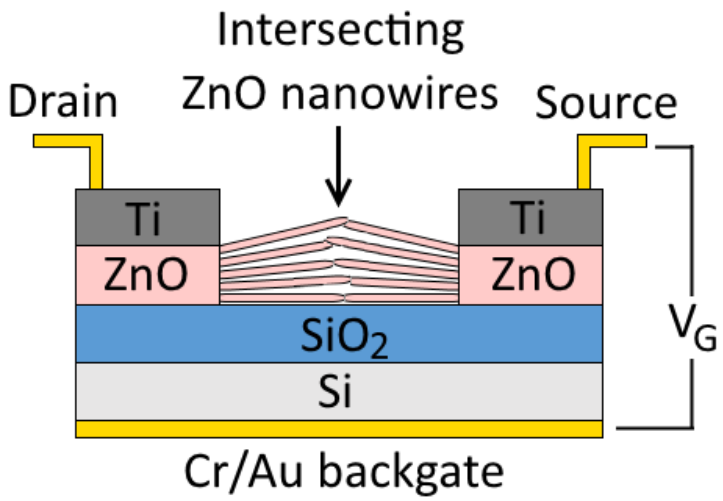

Figure 6.1: A schematic of an FET with an intersecting network of ZnO nanowires as the channel material. The Ti capping layer ensures that the nanowires grow laterally, and also act as a source and drain. The SiO_2/p-Si substrate can then be used as a dielectric and back gate, completing the FET.

6.2 Hydrothermal growth and hierarchical nanowire FET fabrication

Standard photolithographic processing was used to define sets of pairs of electrodes on 1.2 cm $\times$ 1.2 cm SiO_2(100 nm)/p^+-Si wafers, sourced from Silicon Quest International. The inter-electrode spacing of the electrode pairs ranged from 10 μm to 80 μm, in 10 μm increments. After the photoresist was patterned and developed, 100 nm of ZnO was deposited via RF sputtering, followed by a further 60 nm of Ti. The initial ZnO layer serves as a seed for hydrothermal growth. The layer of Ti caps the top of the ZnO seed layer, which prohibits vertical nanowire growth and provides an electrical contact for device measurements, while the sidewall of the ZnO seed layer remains uncovered. This geometry allows for the lateral growth of ZnO nanowires, described in Chapter 2. Photolithographic and RF sputtering processes are described in detail in Chapter 4.

6.2.1 Hydrothermal growth

All of the growth solutions were prepared using an equimolar mix of 25 mM of $Zn(NO_3)_2$ (Sigma Aldrich, 98% purity) and 25mM of HMT (Sigma Aldrich, 99% purity) in 250 mL of de-ionized (DI) water ($\geq$ 18.2 M$\Omega \cdot$ cm), and a variable amount of PEI. PEI was used in concentrations between 2 - 12 mM with molecular weights of 800, 1300, and 2000 g/mol, similar to the range of variables explored in Chapter 5. These varieties of PEI are referred to as PEI(800), PEI(1300), and PEI(2000), respectively.

Each molecular weight of PEI was included in the hydrothermal growth solution at an initial concentration of 2 mM, and was incrementally increased in subsequent hydrothermal growths by 1 mM amounts. The concentration of PEI in subsequent hydrothermal growths was increased until the ZnO seed layer was etched away. In the case of PEI(800), the concentration of PEI was increased by 2 mM increments after reaching 6 mM.

After the precursors were thoroughly mixed, borosilicate glass bottles containing the growth solutions were put in a water bath and left to preheat for 1 hour at a constant temperature of 95°C. After the preheat, the growth/device substrates were submerged in the growth solutions for 19 hours at a constant 95°C before being removed. The samples were then rinsed with DI water ($\geq$ 18.2 M$\Omega \cdot$ cm) and then dried with nitrogen at room temperature. The general theory and experimental techniques underpinning hydrothermal growth of ZnO nanowires are described in detail in Chapter 2.

6.2.2 ZnO nanowire synthesis results

The concentration and molecular weight of PEI used in the hydrothermal growth has a significant effect on the synthesised lateral ZnO nanowires, and can result in a range of distinctly different nanowire morphologies. This is similar to the PEI-mediated growth of vertical nanowires presented in Chapter 5, which also have variable morphologies based on the concentration and PEI used in the hydrothermal growth. The final morphology of the lateral nanowires can be categorised as:

- **Nanowires** - Regular ZnO nanowires which grow laterally from the patterned seed layers. These are typically 1 - 10 μm in length and 100 nm - 1 μm in diameter
- **Hierarchical nanowires** - Hierarchical nanowires which grow laterally from the patterned seed layers. These consist of large primary nanowires which abruptly terminate in long, thin secondary nanowires. The primary nanowires have dimensions on the order of the regular, non-hierarchical nanowires, while the secondary nanowires are typically 5 - 10 μm long. These are morphologically very similar to the hierarchical nanowires synthesised in Chapter 5.
- **Nanowire growth suppression** - Nanowire growth is suppressed from the ZnO seed layers, which remain intact after the hydrothermal growth. Nanowire growth suppression typically occurs at high concentrations of PEI.
- **Substrate etching** - Etching of the ZnO seed layers or the SiO_2/Si substrate from excessive PEI concentration.

The influence of the PEI concentration and molecular weight on the morphology of the ZnO nanowires is summarised in Table 6.1.

Table 6.1: A summary of the lateral nanowire morphologies which result from a given PEI concentration and molecular weight

	PEI(800)	PEI(1300)	PEI(2000)
2mM	Nanowires	Nanowires	Hierarchical NWs
3 mM	Nanowires	Hierarchical NWs	Hierarchical NWs
4 mM	NW growth suppression	Hierarchical NWs	Nanowires
5 mM	Nanowires	Nanowires	Substrate etching
6 mM	Nanowires	Substrate etching	
8 mM	Hierarchical NWs		
10 mM	NW growth suppression		
12 mM	Substrate etching		

The range of possible nanowire morphologies is similar to those obtained from the PEI-mediated growth of vertical nanowires, which is reported in Chapter 5. Figure 6.2 shows SEM images of (a) hierarchical lateral nanowires and (b) regular lateral ZnO nanowires. The lateral hierarchical nanowires strongly resemble the vertical hierarchical nanowires grown in Chapter 5, although their orientation differs due to the geometry of the ZnO sidewall. Hierarchical nanowires are grown when using 4 mM of PEI(1300), which is also the same concentration/molecular weight used to grow vertical hierarchical nanowires. Lateral hierarchical nanowires are also grown when using 8mM of PEI(800), 3 mM of PEI(1300), and 2 - 3 mM of PEI(2000). In comparison, the regular nanowires are very similar in dimension to the primary portion of the hierarchical nanowires, although lack the hierarchically-nucleated secondary nanowires.

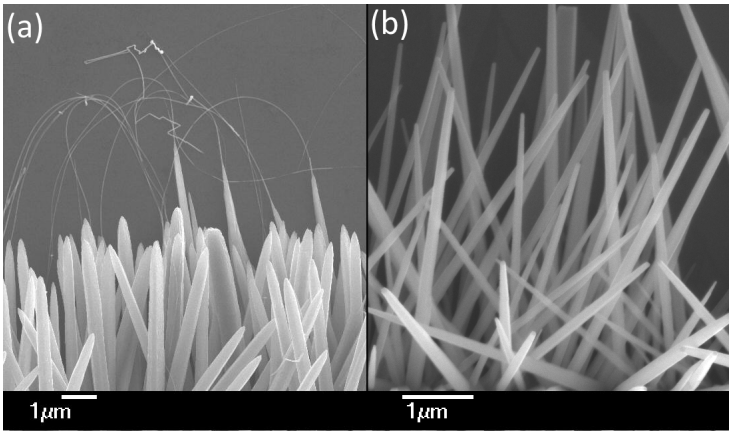

Figure 6.2: SEM images of (a) hierarchical lateral ZnO nanowires and (b) regular lateral nanowires. The seed-layer is not shown in these images.

It is also worth noting that the growth of lateral ZnO nanowires is suppressed when using 4 mM of PEI(800), which also occurs during the vertical growth of nanowires. Figure 6.3 shows an optical image of a lateral substrate grown with 4 mM of PEI(800). The distance between the two electrodes is 50 μm. The source and drain ZnO/Ti electrodes still clearly remain on the substrate, but minimal nanowires have nucleated and grown from the sidewalls. Growth suppression of nanowires typically occurs as the concentration of PEI becomes excessive, chelating the Zn ions out of solution and preventing homogeneous/heterogeneous ZnO nucleation. When the concentration of PEI is increased further, the ZnO seed layers are etched away from the substrate, and the substrate itself is etched. In comparison, the growth suppression at 4 mM of PEI(800) occurs at a much lower concentration of PEI. Although the mechanism behind the growth suppression at this concentration is currently not known, it is clearly a reproducible and real phenomenon.

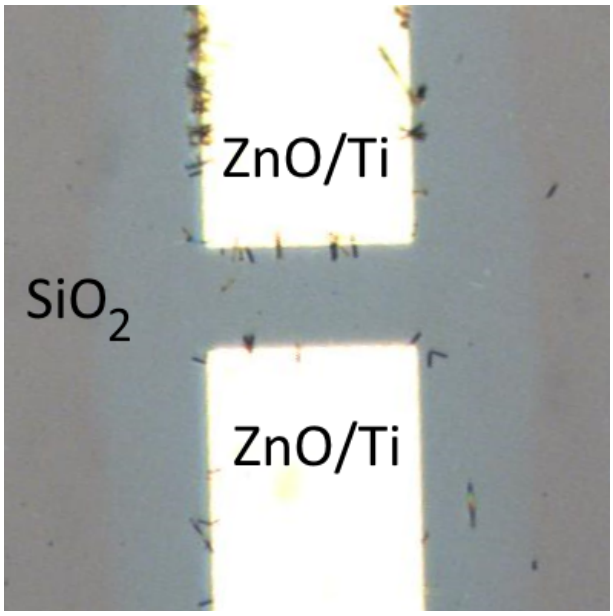

Figure 6.3: Optical image of a lateral sample grown using 4 mM of PEI(800). Nanowire growth has been strongly suppressed.

The most significant result of the PEI concentration/molecular weight experiments is the distinct hierarchical nanowire morphology which occurs under the right growth conditions. The concentration and molecular weight of PEI used in the hydrothermal growth has a definite effect on the dimensions of the regular lateral nanowires, just as it has an effect on the dimensions of the vertical nanowires. However, FETs fabricated using these lateral nanowires are shown to be field-independent, while FETs fabricated using the hierarchical nanowires show pronounced field dependence. As such, an in-depth analysis of the relationship between the PEI used and the dimensions of the regular lateral nanowires is omitted here, and the remainder of this chapter focuses on

the fabrication and electrical characterisation of the hierarchical nanowire FETs.

6.2.3 Hierarchical nanowire device fabrication

Eight pairs of ZnO/Ti electrodes are deposited on each growth/device substrate, and are separated by 10 μm to 80 μm channel distances. When hierarchical nanowires are synthesised from the ZnO seed layers, the shorter electrode channels are bridged by large primary nanorods which meet in the middle of the channel gap. The range of channel distances ensures that a portion of the longer channels are bridged by the secondary nanowires, which grow hierarchically from the primary nanowires. The longest channel gaps are typically left unbridged after the nanowire growth.

Figure 6.4 shows a schematic and SEM image of a pair of electrodes bridged by the secondary nanowire portion of the hierarchical nanowires after the hydrothermal growth process. Lateral arrays of secondary nanowires have grown horizontally along the surface of the substrate from the opposing electrodes, meeting and intersecting in the middle of the channel to bridge the electrodes and form a conduction pathway. These secondary nanowires nucleate hierarchically from the primary nanowires which grow directly from the ZnO sidewall, as shown in Figure 6.4 (b). Figure 6.4 (c) and (d) show corresponding SEM images of an actual device, which is grown with 4 mM of PEI(1300). The primary nanowires are from 150 to 300 nm in diameter and 10 - 15 μm in length. They project radially in a 3 dimensional brush-like structure from the exposed ZnO sidewall. Secondary nanowires, with diameters from 10 to 50 nm and lengths of up to 10 μm, emerge from the tips of the primary nanowires, as shown in Figure 6.4 (d).

Although the secondary nanowires are only 10 to 50 nm in diameter, it's possible to image their diffraction patterns against the SiO_2 substrate using regular optical microscopy. Figure 6.5 shows an optical image of an FET bridged with hierarchical nanowires from a top-down perspective. These hierarchical nanowires are grown using 8 mM of PEI(800). The two large electrodes ZnO/Ti are labelled as 'S' and 'D' (for 'source' and 'drain'.) Large primary nanowires grow laterally from the exposed ZnO sidewall, fringing the electrodes. The inset of Figure 6.5 shows a magnified view of the channel gap. The secondary nanowires can clearly be discerned despite their diameter – optical microscopy is therefore an efficient way to quickly determine whether the hydrothermally-grown nanowires are regular nanowires or whether they're hierarchical. The large image of the FET is taken at 10x magnification, while the magnified inset is taken at 100x.

SEM images of several secondary nanowire FETs are shown in Figure 6.6. Figure 6.6(a) and (b) shows an FET fabricated using 3 mM of PEI(2000). The channel gap of

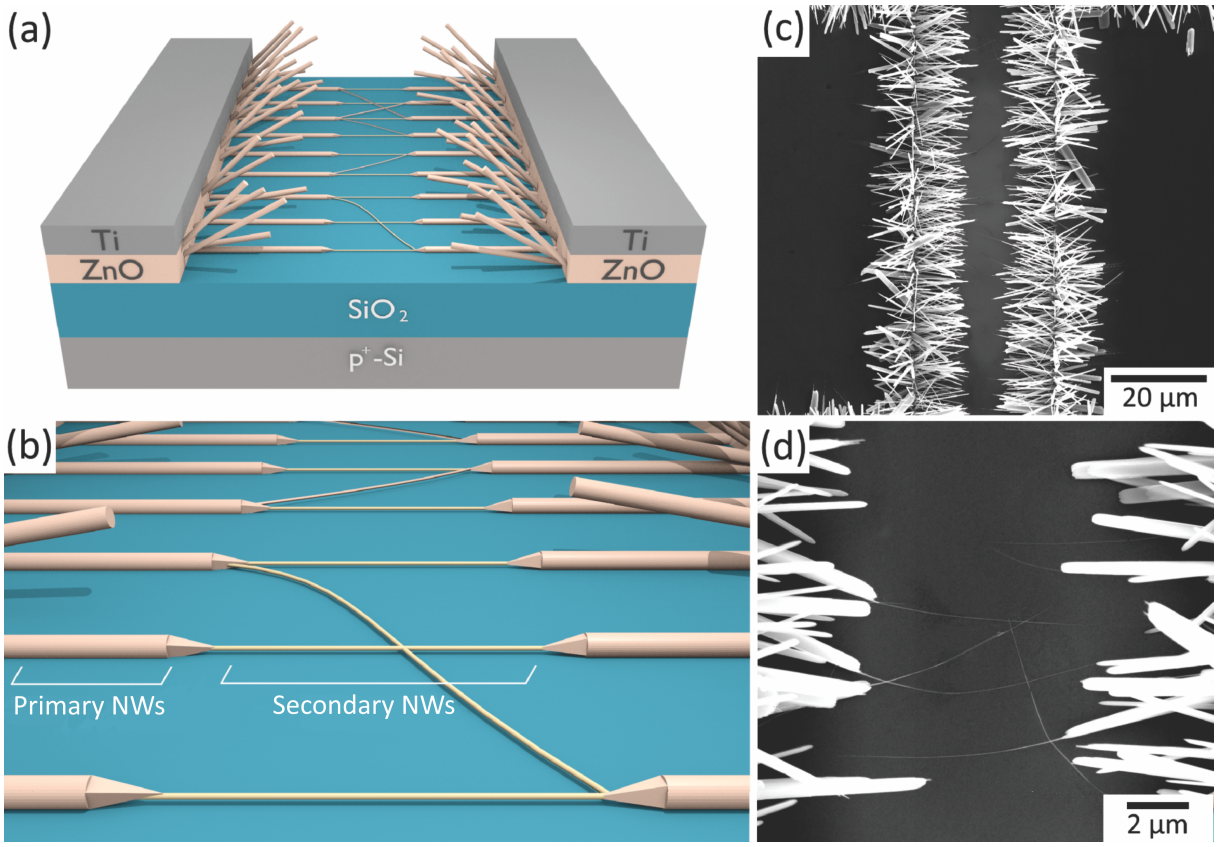

Figure 6.4: (a) A schematic of the hierarchical nanowire FET, showing the seed layers/electrodes and bridging nanowires. (b) A close-up of the primary/secondary nanowires. (c) An SEM image of an actual device. (d) A close-up of the channel of the device, showing the primary/secondary nanowires.

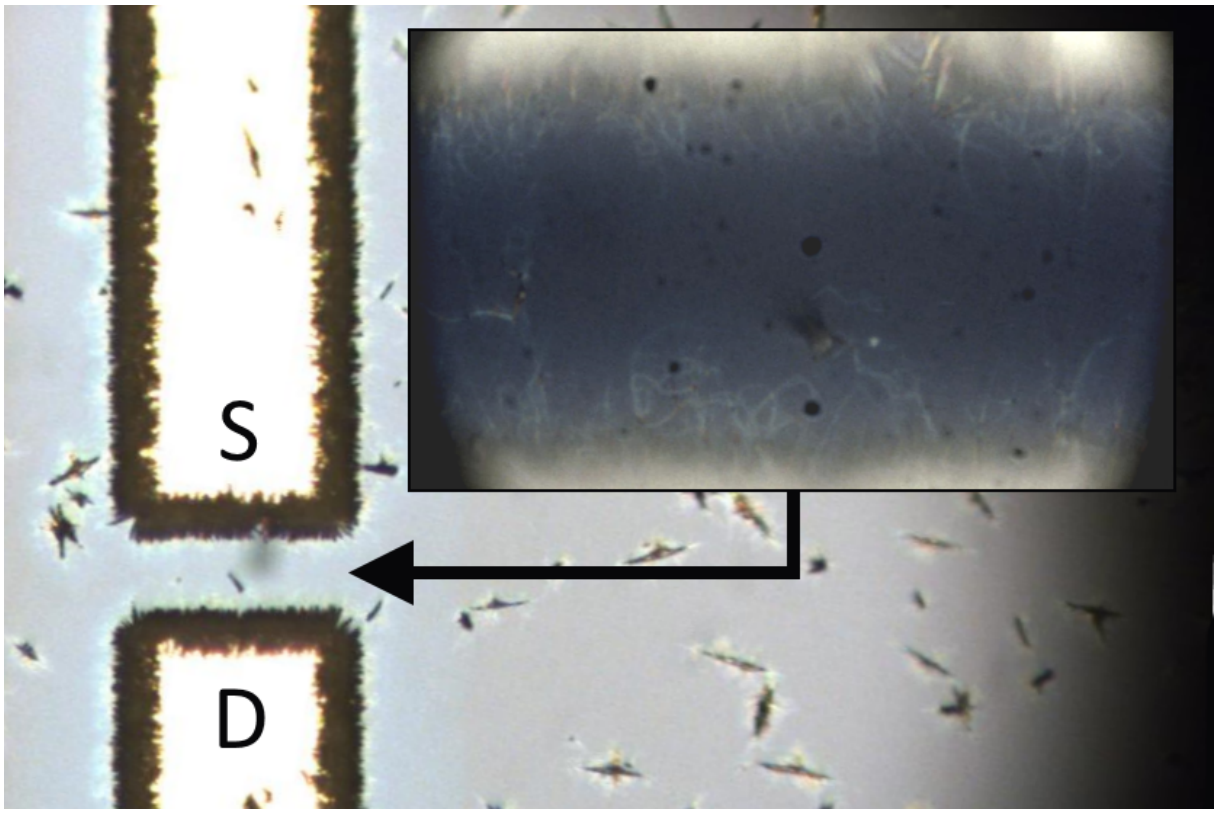

Figure 6.5: Optical image of a PEI-mediated hierarchical nanowire FET grown with 8 mM of PEI(800). Both primary and secondary nanowires can be discerned. The source and drain electrodes are marked 'S' and 'D' respectively. The gap between the electrodes is 80 μm.

the FET is too wide for the primary nanowires to intersect in the middle, while the secondary nanowires readily bridge the gap, highlighted in Figure 6.6(b). Figure 6.6(c) and (d) show two different FET devices grown using 4 mM of PEI(1300). Although the length of the secondary nanowires is similar between the two devices, they have nucleated and grown from the primary nanowires in distinctly different densities. Figure 6.6(e) and (f) show two FETs fabricated using 8 mM of PEI(800). This recipe yields large numbers of secondary nanowires, creating very dense and complicated intersecting networks.

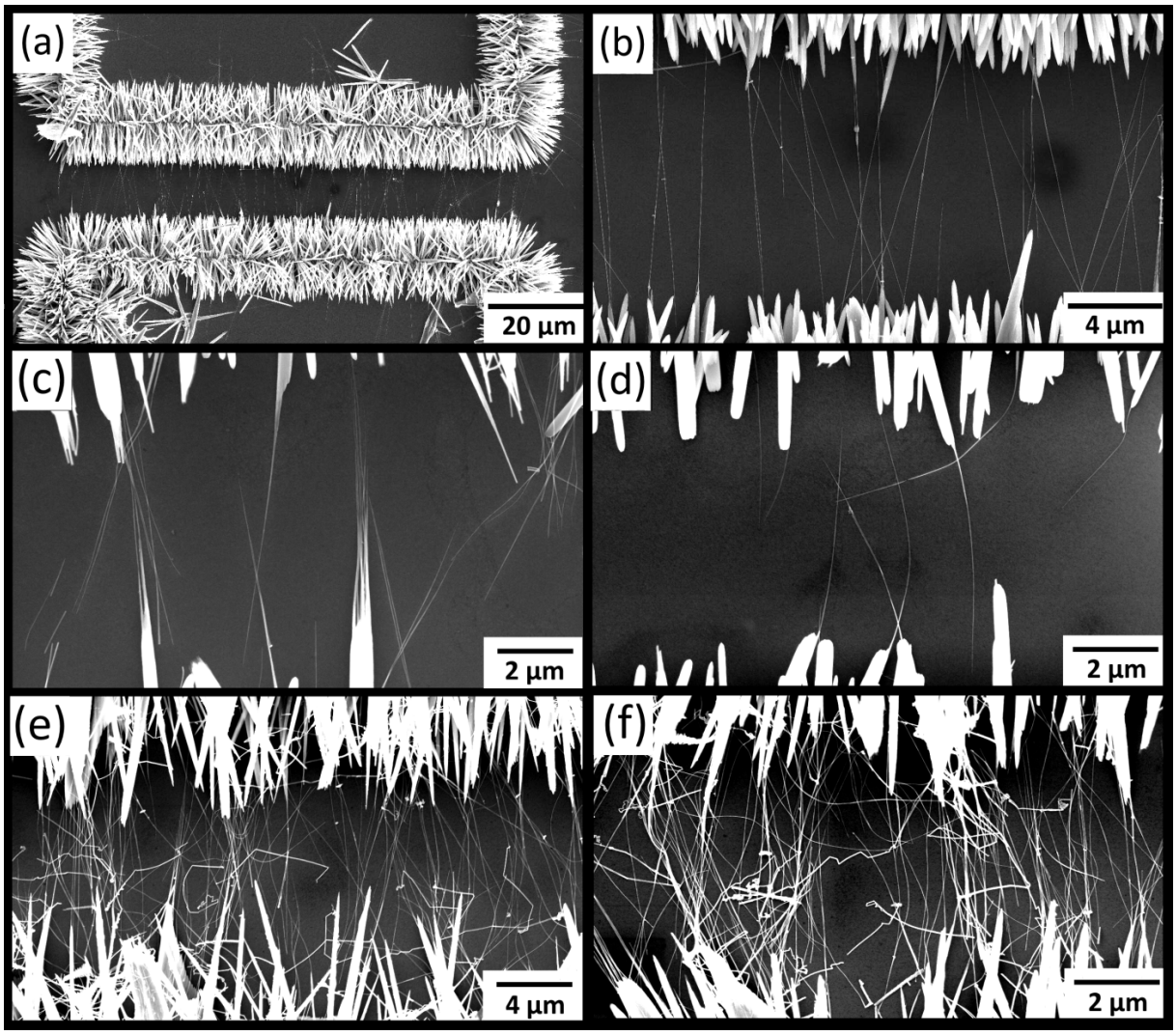

Figure 6.6: SEM images of hierarchical nanowire FETs synthesised using: (a),(b) 3 mM of PEI(2000), (c),(d) 4 mM of PEI(1300), (e),(f) 8 mM of PEI(800).

6.2.4 Hierarchical nanowire growth mechanism

Although the hydrothermal growth process only involves a single growth step, two distinct nanostructures grow hierarchically from the seed layers. As noted in Section

6.2.2, the lateral hierarchical nanowires grown here strongly resemble the vertical hierarchical nanowires grown in Chapter 5. Both vertical and lateral hierarchical nanowire growths use PEI at similar or identical concentrations, and neither growth methods yield hierarchical nanowires when PEI is omitted. It is therefore very likely that the lateral and vertical hierarchical nanowire growth is driven by the same PEI-mediated mechanism, described in Section 5.4.2 in Chapter 5.

The growth of lateral hierarchical nanowires is shown in Figure 6.7. The primary nanowires are first grown during an initial growth phase, shown in Figure 6.7(a). During this phase, the Zn^{2+} ions are provided exclusively by the decomposition of $Zn(NO_3)_2$ precursors, which directly and indirectly crystallise into the primary nanowires. A portion of these Zn^{2+} ions form PEI-Zn complexes through chelation. As the hydrothermal growth continues, the concentration of Zn^{2+} precursor in the solution decreases as it crystallises out. Eventually the only source of Zn^{2+} ions are the remaining Zn-PEI complexes. These Zn-PEI complexes gradually release the Zn^{2+} ions back into solution via a Mannich reaction with formaldehyde in solution [75]. This drives the second growth phase, shown in Section 5.4.2(b). As the concentration of Zn^{2+} in solution is comparatively lower than during the primary growth phase, the released ions crystallise into the much thinner secondary nanowires, which nucleate and grow from the terminating ends of the primary nanowires.

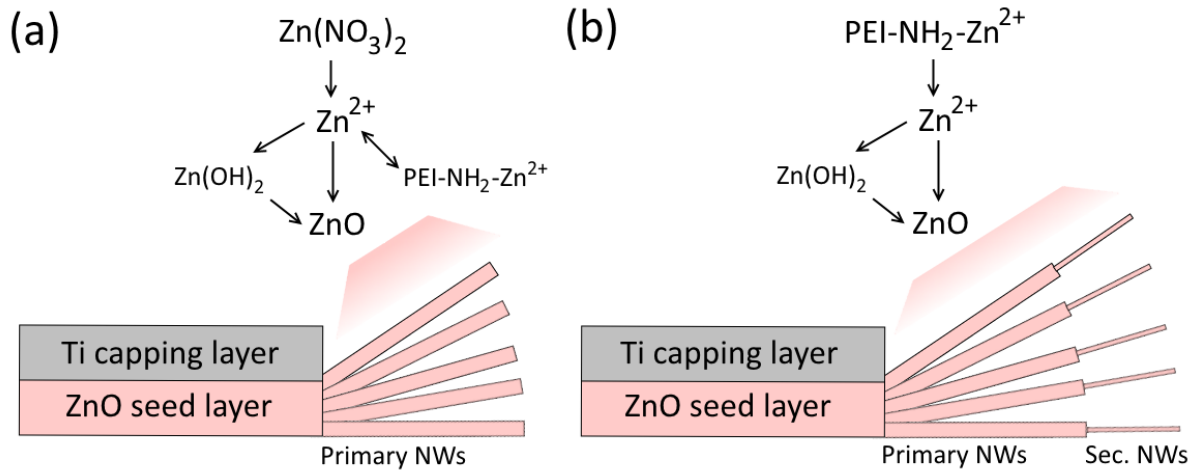

Figure 6.7: A schematic of the PEI-mediated hierarchical nanowire growth mechanism. Primary and secondary nanowires are grown in two distinct phases.

6.2.5 Hierarchical nanowire crystal structure

High resolution transmission electron microscopy (HRTEM) was performed to investigate the crystal structure of the hierarchical nanowires. These measurements were

undertaken by Dr. Jerome Majimel at ICMCB Bordeaux - the specific parameters used are detailed in Chapter 4. The hierarchical nanowires were grown using 4 mM of PEI(1300). These measurements show that the primary and secondary nanowires are monocrystalline, and both are orientated along the [001] c-axis. Figure 6.8(a) shows the hexagonal wurtzite structure of the primary nanowires, with corresponding electron diffractogram shown inset. A representative HRTEM measurement of the secondary nanowire is shown in 6.8(b), confirming the hexagonal wurtzite crystal structure and c-axis orientation of the secondary nanowires.

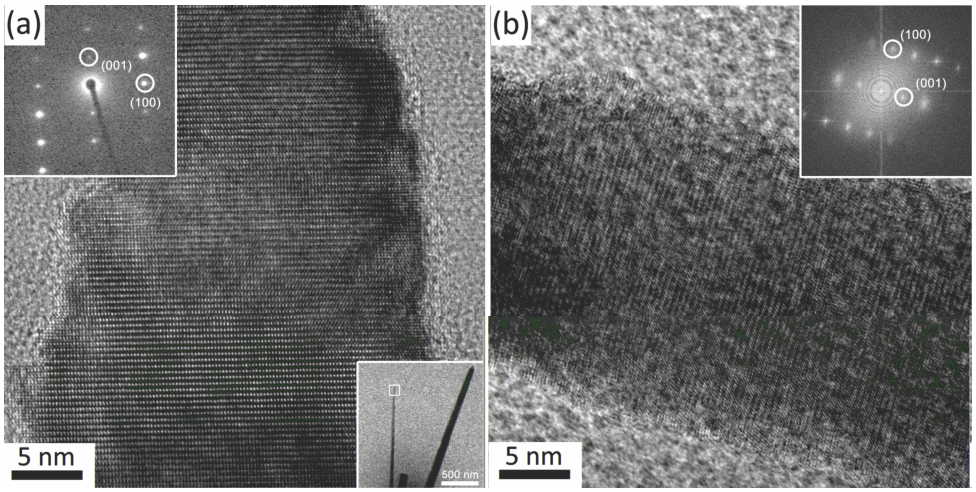

Figure 6.8: TEM images of (a) primary and (b) secondary nanowires from hierarchical nanowires.

HRTEM images of the primary/secondary nanowire interfaces also confirm that the secondary nanowires nucleate and grow epitaxially from the primary nanowires. Figure 6.9(a) shows a secondary nanowire growing from the side face of a primary nanowire, with the interface between the two highlighted. Figure 6.9(b) shows an HRTEM image of the highlighted interface, displaying the common c-axis orientation between the two. Although the primary and secondary nanowires have grown epitaxially in relation to each other, there are small areas at the interface where the crystal orientation slightly deviates from the common c-axis. Figure 6.9(c) highlights these deviations, which appear as contrast variations in the micrographs.

6.3 Electrical measurements

The architecture of the growth/device substrates used in the hierarchical nanowire FET fabrication allows for bridged ZnO/Ti electrodes to be used as an FET, as described in Section 6.1. In these measurements, the ZnO/Ti electrodes are used as the transistor source and drain, while the SiO_2/Si substrate is used as a dielectric and global

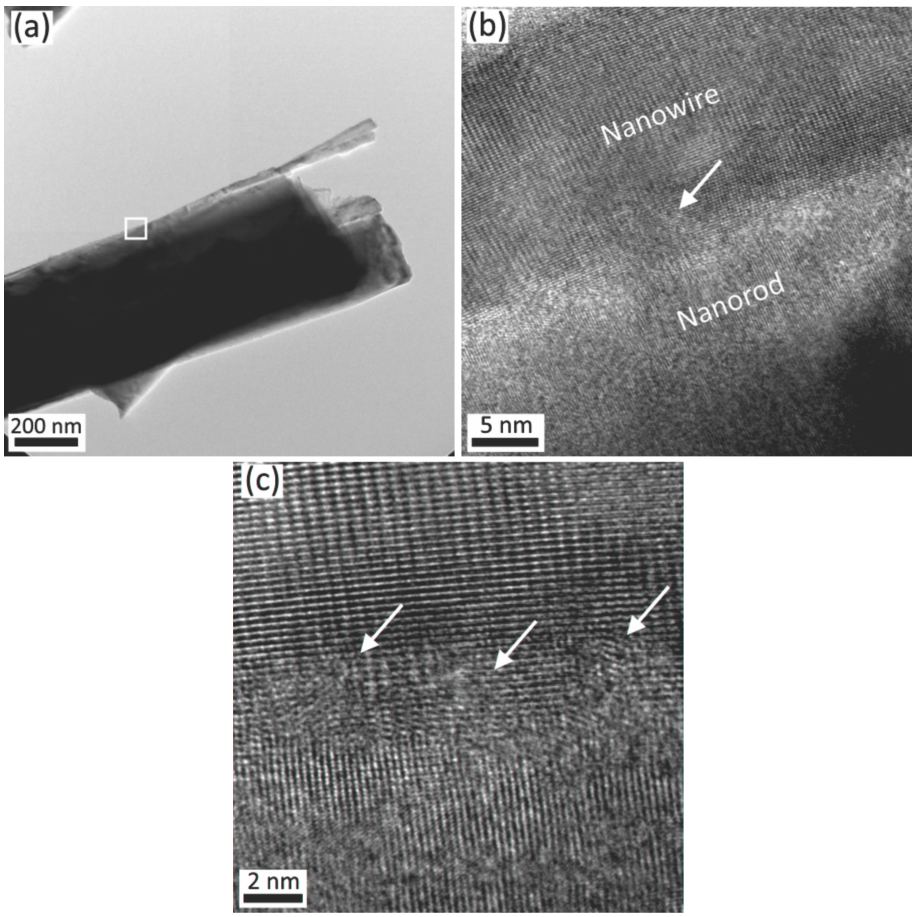

Figure 6.9: (a) Secondary nanowires hierarchically nucleating from primary nanowires. (b) TEM images of the highlighted primary/secondary nanowire interface. Arrows highlight small deviations in the shared c-axis, which are shown in (c).

backgate. The measurements of the hierarchical nanowire FETs in this section are organised by the molecular weight of the PEI used in their synthesis. The experimental techniques used to electrically measure the devices are described in Chapter 4, while the device characteristics which are measured are described in Chapter 3. All of the transfer characteristics in this section are obtained by sweeping the gate voltage from the negative to the positive direction, and then back in the negative direction.

6.3.1 PEI(2000) devices

As noted in Table 6.1, hierarchical nanowires are synthesised when 3 mM of PEI(2000) is included in the growth. Because the spacing of the ZnO/Ti electrodes ranges from 10 μm to 80 μm, some devices are bridged by intersecting secondary nanowires, while other devices are bridged by intersecting primary nanowires. Both of these were electrically measured to contrast the difference in field dependence between the two. The devices were measured immediately after the hydrothermal growth, with no annealing or post-growth processing.

Figure 6.10 shows drain-source current vs. gate voltage measurements (transfer characteristics) for FETs bridged with secondary nanowires (black, circles) and with primary nanowires (red, squares) grown using 3 mM of PEI(2000). Both devices have been fabricated on the same device substrate, and are driven at a drain-source voltage of 1 V. Despite the fact that the devices are unannealed, the secondary nanowire FET shows clear field dependence between V_G = -10 V and 10 V. The FET operates in enhancement mode, with a threshold voltage of 2 V and an on-off current ratio of 10^5. The transconductance of the device is 3.7×10^{-8} S, and the subthreshold swing is 547 mV/decade. The mobility of the device is very difficult to calculate, as the channel length is uncertain given the multiple wires which make up the channel. Furthermore the capacitance is difficult to estimate, which is also necessary to accurately determine the device mobility.

In contrast, the primary nanowire FET shows very little field dependence over the same range of gate voltages. Although the primary and secondary nanowires have different sizes (which may affect their response to an applied gate voltage), the difficulty in gating the primary nanowire FET is consistent with other examples of as-grown ZnO nanowires [113, 114, 118, 54, 11], even with diameters directly comparable to the secondary nanowires [113, 118].

Although the field dependence of the as-grown secondary nanowires is surprising, it is consistent across all of the secondary nanowire devices measured. The transfer characteristics from two additional FETs fabricated using 3 mM of PEI(2000) are shown

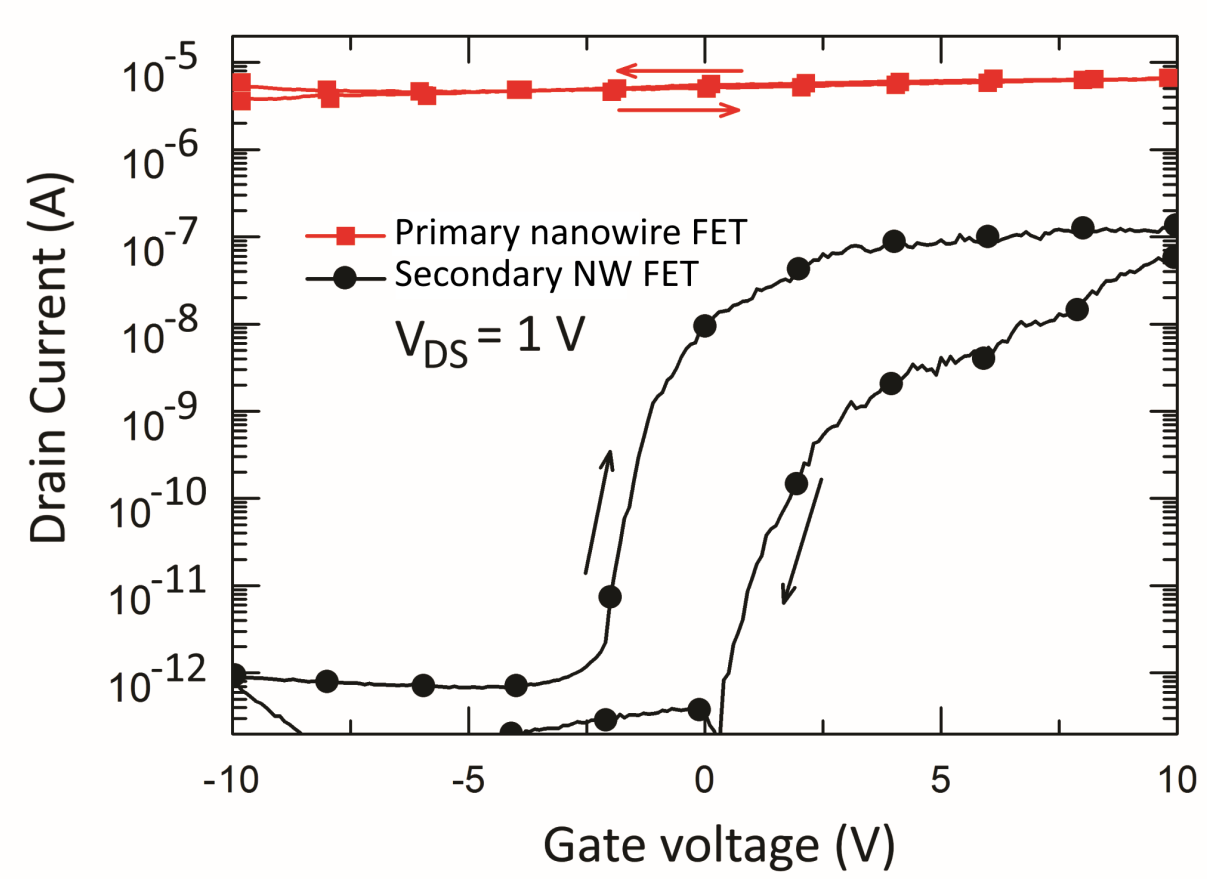

Figure 6.10: Transfer characteristics of secondary-nanowire (black, circles) and primary-nanowire FETs (red, squares) fabricated using 3 mM of PEI(2000). Both devices are driven at V_{DS} = 1 V.

in Figure 6.11. Both of these devices are driven at V_{DS} = 0.1 V. In contrast to the previous FET, both of these devices operate in depletion mode. The FET measured in Figure 6.11(a) has a threshold voltage of ≈ -2.5 V and an on-off ratio of 10^5. The transconductance of the device is 4.38×10^{-8} S, and the subthreshold swing is 191 mV/decade. The FET measured in Figure 6.11(b) has a threshold voltage of ≈ -6.5 V and an on-off ratio of 10^5. The transconductance is 6.44×10^{-8} S, and the subthreshold swing is 376 mV/decade. The device characteristics of the FETs presented in Figures 6.10 and 6.11 are summarised in Table 6.2. They are listed as FET 1, (a), and (b), respectively.

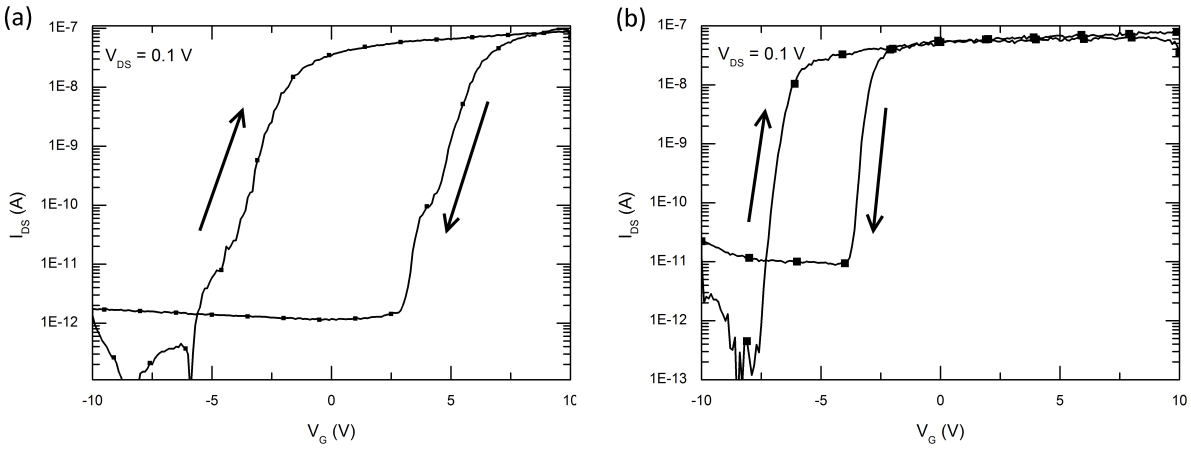

Figure 6.11: Further transfer characteristics of PEI-mediated hierarchical nanowires synthesised using 3 mM of PEI(2000). Both devices are driven at V_{DS} = 0.1 V.

Table 6.2: Summary of the device characteristics of 3mM PEI(2000) hierarchical nanowire FETs

FET	V_{th}	$I_{on/off}$	g_m (S) (max.)	Subthreshold swing (mV/dec.) (min.)
1	2	10^5	3.7×10^{-8}	547
(a)	-2.5	10^5	4.38×10^{-8}	191
(b)	-6.5	10^4	6.44×10^{-8}	376

6.3.2 PEI(1300) devices

All of the secondary-nanowire FETs fabricated using PEI(1300) also show well-defined field dependence and device characteristics, similar to those grown with PEI(2000). In total, 4 separate devices are measured here. Figure 6.12 shows the transfer characteristics of four FETs bridged by secondary nanowires grown using 4 mM of PEI(1300). All of the FETs clearly respond to applied gate voltages and have clear on and off regimes. The devices are driven at a constant drain-source voltage of 1 V. As before, all of the devices here exhibit n-type behaviour. The two devices shown in 6.12(a) and 6.12(d)

operate in enhancement mode, with threshold voltages of 4 V and 5 V respectively, and with on-off ratios of 10^4 and 10^3. The other two devices (shown in 6.12(b) and 6.12(c)) operate in enhancement mode, with threshold voltages of -4 V and -7.5 V, respectively. Both of these devices have an on-off ratio of 10^4.

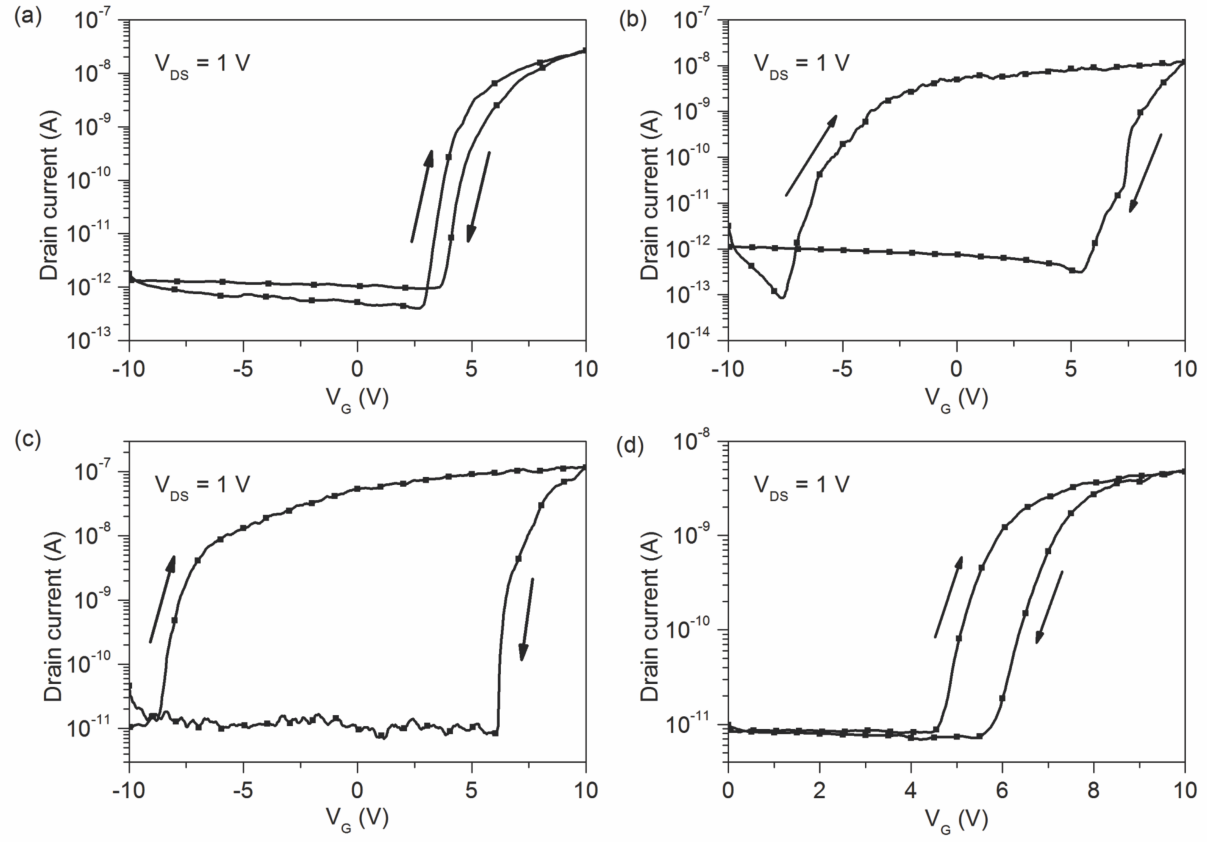

Figure 6.12: Transfer characteristics of hierarchical nanowire FETs synthesised using 4 mM of PEI(1300). The devices are measured at V_{DS} = 1 V.

The device characteristics for the FETs displayed in Figure 6.12, including their transconductance and subthreshold swing values, are summarised in Table 6.3. The transconductances of the devices are comparable to those fabricated using PEI(2000), and are on the order of 10^{-8} - 10^{-9} S. The subthreshold swings are also comparable, although the FET shown in Figure 6.12(c) has a slightly higher subthreshold swing than other FETs, which is on the order of 1V/decade.

Table 6.3: Summary of the device characteristics of 4 mM PEI(1300) hierarchical nanowire FETs

FET	V_{th}	$I_{on/off}$	g_m (max.) (S)	Subthreshold swing (mV/dec.) (min.)
(a)	4	10^4	3.37×10^{-9}	561
(b)	-4	10^4	1.3×10^{-8}	719
(c)	-7.5	10^4	5.7×10^{-8}	1083
(d)	5	10^3	9.55×10^{-9}	336

6.3.3 PEI(800) devices

Figure 6.13 shows the transfer characteristics of three FETs bridged by secondary nanowires grown using 8 mM of PEI(800). As before, all of the devices show n-type behaviour and well-defined on and off regimes. All of the devices are driven at a constant drain-source voltage of 1 V. The FET in Figure 6.13(a) operates in enhancement mode, with a threshold voltage of 1 V and an on-off ratio of 10^4. In contrast, the two FETs shown in Figure 6.13(b) and (c) operate in depletion mode, with threshold voltages of -2.5 V and -5 V respectively. Both have on-off ratios of $\approx 10^3$. The devices which operate in depletion mode have a significantly increased hysteresis compared to those operating in enhancement mode, as is the case for the PEI(1300) FETs displayed in Figure 6.12.

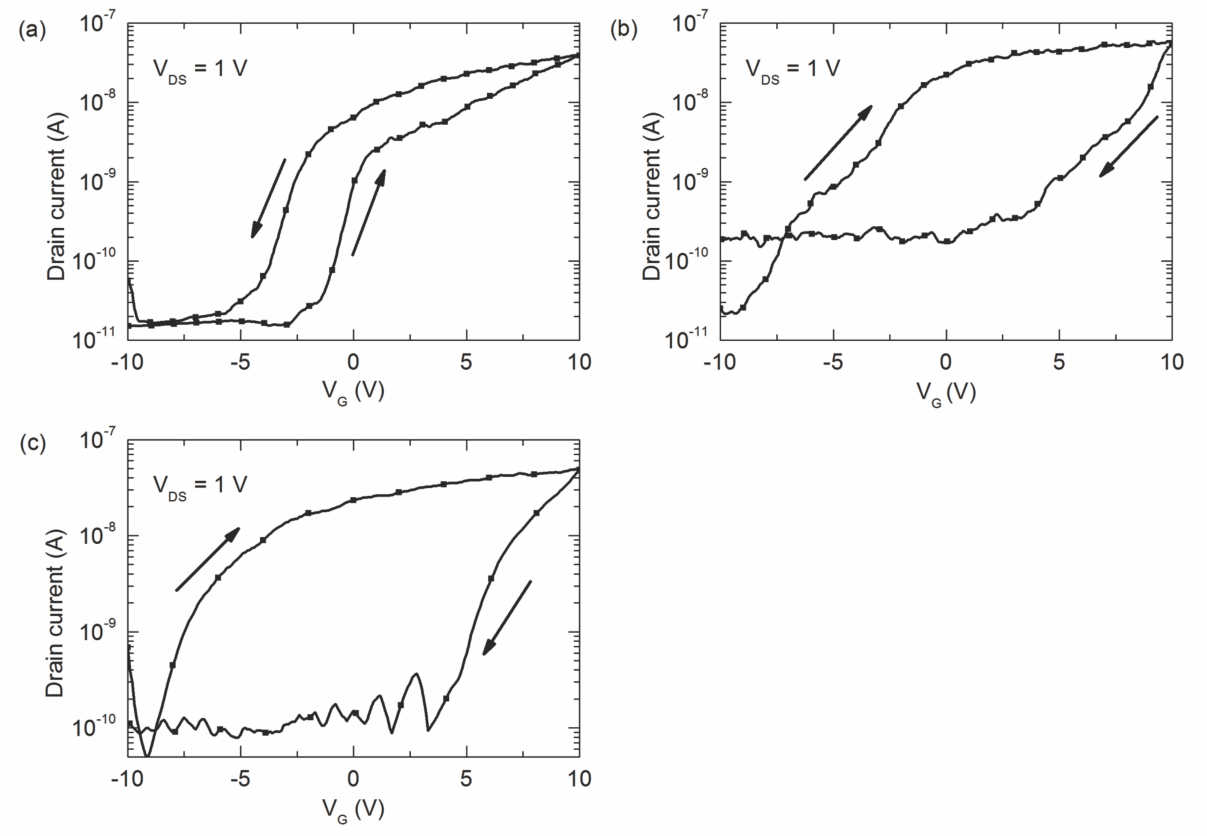

Figure 6.13: Transfer characteristics of hierarchical nanowire FETs synthesised using 8 mM of PEI(800). The devices are measured at V_{DS} = 1 V.

The device characteristics of the FETs shown in Figure 6.13 are summarised in Table 6.4. The minimum subthreshold swing values of these devices is significantly larger than all of the FETs fabricated with PEI(2000), and almost all of the FETs fabricated with PEI(1300) (bar FET (c), detailed in Table 6.3.) This is attributed to the increased number of nanowire-nanowire junctions present in the PEI(800) samples, which has a detrimental effect on the switching ability of the FET. These samples are represented

by the SEM images depicted in Figure 6.6.

Table 6.4: Summary of the device characteristics of 8 mM PEI(800) hierarchical nanowire FETs

FET	V_{th}	$I_{on/off}$	g_m (max.) (S)	Subthreshold Swing (mV/dec.) (min.)
a	1	10^4	1.1×10^{-8}	1149
b	-2.5	10^3	5.57×10^{-8}	2061
c	-5	10^3	2.76×10^{-8}	1219

6.3.4 Discussion

All of the hierarchical nanowire FETs that have been measured show obvious field dependence, and are responsive to applied gate voltages without any high-temperature annealing or post-processing. This is in stark contrast to the majority of reported ZnO nanowire FETs [113, 114, 118, 54, 11] (which are discussed in detail in Chapter 3), and hierarchical nanowire FETs which are fabricated using intersecting primary nanowires. Furthermore, some of the FETs presented here operate in enhancement mode, meaning they are depleted at zero gate voltage and must be turned on by populating the nanowires with charge carriers. In comparison, field-independent ZnO nanowires are typically highly conductive at zero gate voltage, and cannot be depleted even with very strong negative gate biases [113, 118].

As the secondary nanowires presented here have a lower electron concentration in their as-grown state than usual, there must either be fewer intrinsic electron donors to begin with, or the intrinsic electron donors are compensated for by electron acceptors. Because the nanowires have a high surface to volume ratio, it is possible to capture electrons from the bulk through surface traps. It is well-known that O- and OH- groups from the atmosphere preferentially adsorb on ZnO nanowire surfaces, depleting the nanowire by compensating intrinsic electron donors [176, 177, 178]. There is some variation in the densities of the depleting surface states between nanowires, which can even occur between nanowires retrieved from the same growth batch [179]. This variation can affect the charge carrier density of the nanowires, which may be responsible for the variation of device characteristics between the nanowire FETs fabricated here. As discussed in Section 3.5 of the thesis, surface states also strongly affect the hysteresis of nanowire FETs [180, 181], which may be responsible for the device hysteresis and variation thereof.

6.4 Persistent photoconductivity measurements

It has been well documented that the surface states which deplete ZnO nanowires can be desorbed using UV radiation, releasing trapped electrons back into the nanowire bulk [182, 183, 184, 185]. Although there is still some contention over the exact mechanism [183], it is generally accepted that photogenerated holes from electron-hole pairs recombine with surface-trapped electrons, which then causes the surface species to desorb [178, 182, 185, 96]. Thus, if a nanowire is exposed to UV radiation while being kept under vacuum, desorped surface species are pumped away before they can readsorp, giving rise to a persistent nanowire photoconductivity. The significance of the surface traps can then be determined by the magnitude of the persistent

photoconductivity.

To properly gauge the impact of the nanowires' adsorbed surface states, a hierarchical nanowire FET which operates in enhancement mode (i.e. with a positive threshold voltage) was selected for persistent photoconductivity measurements. As the FET is depleted at zero gate voltage, it is assumed that the channel is fully depleted due to the surface states. The FET measured was fabricated using 4 mM of PEI(1300).

The FET was connected to a printed circuit board using copper wire and silver paste, and consequently measured inside of a cryostat. This cryostat was used solely as a vacuum chamber, and all measurements were taken at room temperature. The cryostat is fitted with a CaF_2 window, which allows for illumination of the sample with UV light. UV light was provided by 395 nm LEDs at an intensity of 8.8 mW cm^{-2}. The intensity of this UV source was measured before and after each exposure to ensure that there was no fluctuation in power. The pressure of the chamber was measured during pumping, and decreased from an initial pressure of 5.56×10^{-4} mbar to 1.2×10^{-4} mbar over a 35 hour period. All electrical measurements were acquired using the standard Agilent 4156C parameter analyser used elsewhere in this thesis.

Before the cryostat was pumped down and the FET illuminated with UV, transfer characteristics of the FET in atmosphere were recorded as a control. The transfer characteristics are displayed in Figure 6.14. The FET shows well-defined on-off switching in atmosphere, with a threshold voltage of $\approx$2 V. The rise in the drain-source current (shown in black) with negative gate voltages is explained by the leakage current (plotted in red), likely introduced by noise and unintentional conduction pathways in the cryostat system. The absolute value of the leakage current has been plotted so that it can be shown on a logarithmic scale. The FET is driven with a V_{DS} value of 5 V, which is significantly higher than the other FETs shown in this chapter.

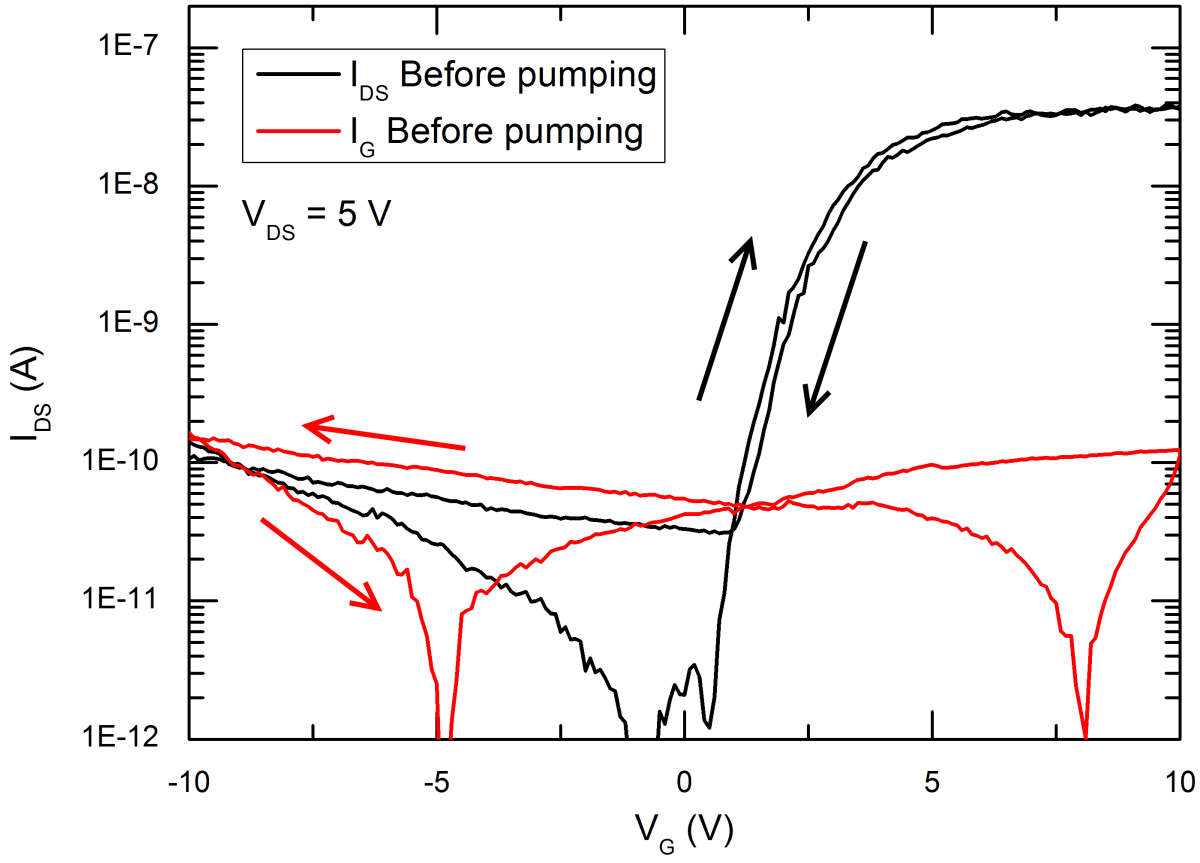

Figure 6.14: Transfer characteristics of the PEI(1300) hierarchical FET prior to evacuating the cryostat. The device is driven at V_{DS} = 5 V.

Further transfer characteristics of the same FET were taken in vacuum while the cryostat was actively pumped, but prior to UV exposure. The transfer characteristics of the FET before (black) and during (red) pumping are displayed in Figure 6.15. The measurement taken before pumping is the same transfer characteristics shown in Figure 6.14. The transfer characteristics of the FET are largely unchanged during the pumping process, with an identical threshold voltage of ≈2 V. However, the hysteresis of the device has increased as the gate voltage is swept in both directions. As noted before, nanowire surface states play a large role in determining the hysteresis of nanowire FETs [180, 181], which may change when the chamber is evacuated. The increased hysteresis of the device may be caused by these changes to the surface states.

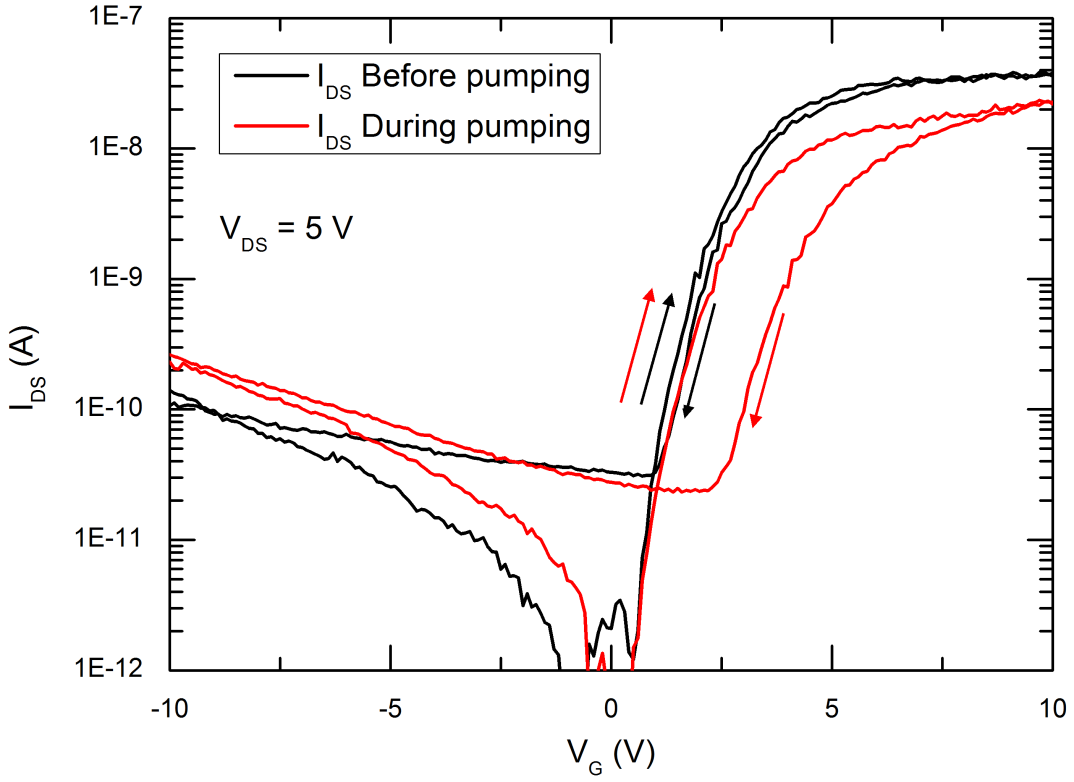

Figure 6.15: Transfer curves before (black) and during (red) pumping of the cryostat. The FET is driven at V_{DS} = 5 V.

After the FET transfer curves were recorded before and during pumping, photoconductivity measurements were performed by illuminating the sample with the 395 nm UV source. Figure 6.16 shows the persistent photoconductivity of the FET as it is exposed to UV radiation under vacuum. The FET is driven at a drain-source voltage of 1 V with no applied gate voltage, and shows an initial dark current of 10^{-12} A.

After the UV source is switched on, the drain current rapidly increases by 5 orders of magnitude. Although the wavelength of UV used (395 nm) falls outside of the bandgap of bulk ZnO, we clearly see a photoresponse corresponding to electron-hole pair production and surface species desorption, which agrees with other reports using similar wavelengths of light [186, 187].

The photoconductivity is very persistent while the vacuum is maintained, remaining stable 24 hours after the UV source is switched off. Similar to other ZnO nanowire persistent photoconductivity experiments in vacuum [182], there is no immediate drop in the current after switching off the UV light. This suggests that the photocarrier contribution to the photocurrent is minor. The contribution of the photocarriers to the photocurrent is very difficult to determine due to the indeterminate path length of the FET, but a similar order-of-magnitude calculation reported in the literature suggests that it may be as low as $\approx 10^{-4}$ nA [182]. The lack of a sharp decrease in photoconductivity when turning off the UV illumination also corroborates with other persistent photoconductivity experiments in vacuum, which are even performed using UV that falls within the bandgap of bulk ZnO [182]. After venting to atmosphere, the drain current decreases by almost two orders of magnitude over ten hours. Although the FET does not return to its initial dark current over this timescale, other nanowires in vacuum have shown similarly long decay times previously [182].

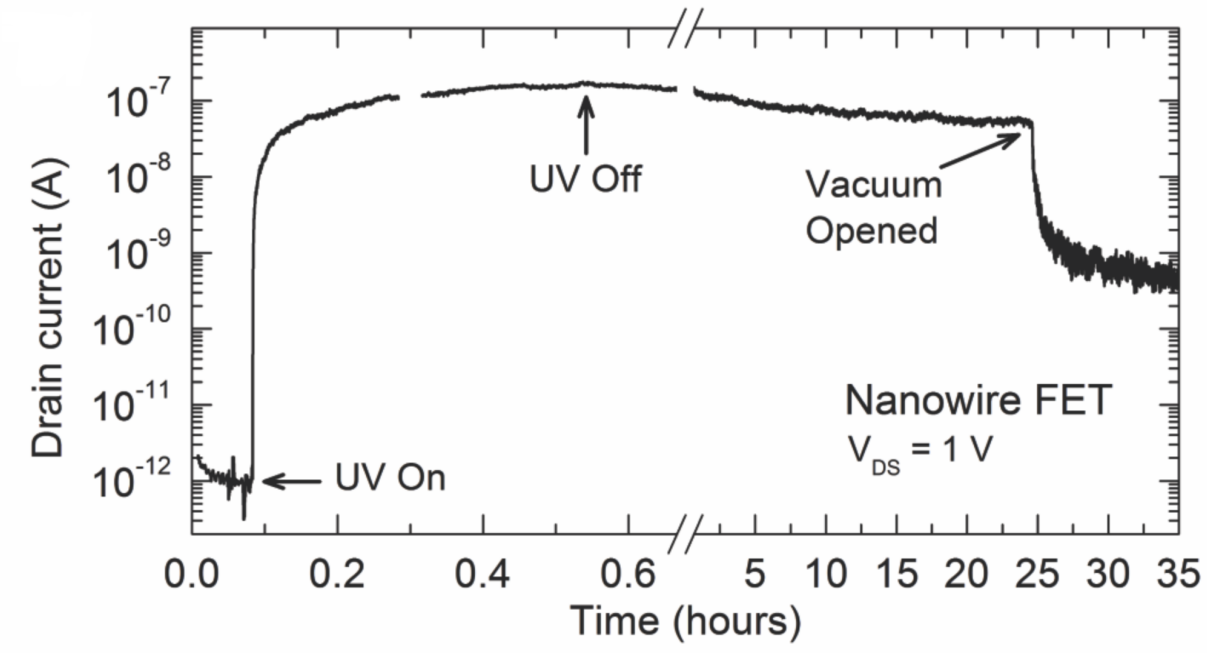

Figure 6.16: The persistent photoconductivity of the PEI(1300) hierarchical nanowire FET before, during, and after UV exposure.

6.4.1 Transfer characteristics during persistent photoconductivity

The persistent photoconductivity shows that the nanowire electron concentration rapidly increases by orders of magnitude as the depleting surface states are removed from the nanowire surface. The depleting surface states therefore act as a competing defect mechanism to the electron donors still present in the bulk of the nanowire. To determine how the depleting surface states affect the field dependence of the FET, the cryostat was re-pumped after venting and the FET was re-exposed to the UV source. The transfer characteristics of the FET were then measured while the FET was in the persistent photoconductivity state (i.e. after the UV source had been switched off, but before the cryostat was vented.)

Figure 6.17 shows the transfer curves of the FET both prior to pumping (black) and during persistent photoconductivity (red). Removing the depleting surface states has an enormous effect on the behaviour of the device. As the secondary nanowires have been stripped of the depleting surface states, there is no competing mechanism to account for the intrinsic electron donors. As such, the FET is now filled with charge carriers at zero gate voltage, causing the device to switch from operating in enhancement mode to depletion mode. The threshold voltage of the device has changed from $\approx$2 V (prior to UV exposure) to $\approx$-13 V (during persistent photoconductivity.) While the FET is measured during persistent photoconductivity, the on-current increases by almost two orders of magnitude, and the hysteresis also increases significantly.

As discussed in the overview of hysteresis and passivation in ZnO nanowires (Section 3.5), surface states at the nanowire/atmosphere interface and the nanowire/substrate interface can influence the hysteresis of the FET. The persistent photoconductivity measurements show an increase in hysteresis, despite the fact that absorped charge traps are being expunged from the nanowire surface. This may suggest that the nanowire/substrate interface states act in opposition to the surface charge traps, and the balance is tipped with their removal. Another possibility is that the UV light releases trapped charges on the SiO_2 surface, which are now mobile. In any case, it is likely that the surface states have an impact on the hysteresis, although it is very difficult to determine exactly what causes the increase under persistent photoconductivity conditions.

Despite the fact that the threshold voltage has significantly shifted in the negative direction, the hierarchical nanowire FET still shows clear field dependence. Furthermore, the threshold voltage of $\approx$-13 V is not particularly low when compared to other hydrothermal nanowire FETs in the literature (summarised in Table 3.1 in Chapter 3), even when they have been annealed and have comparable diameters to the hierar-

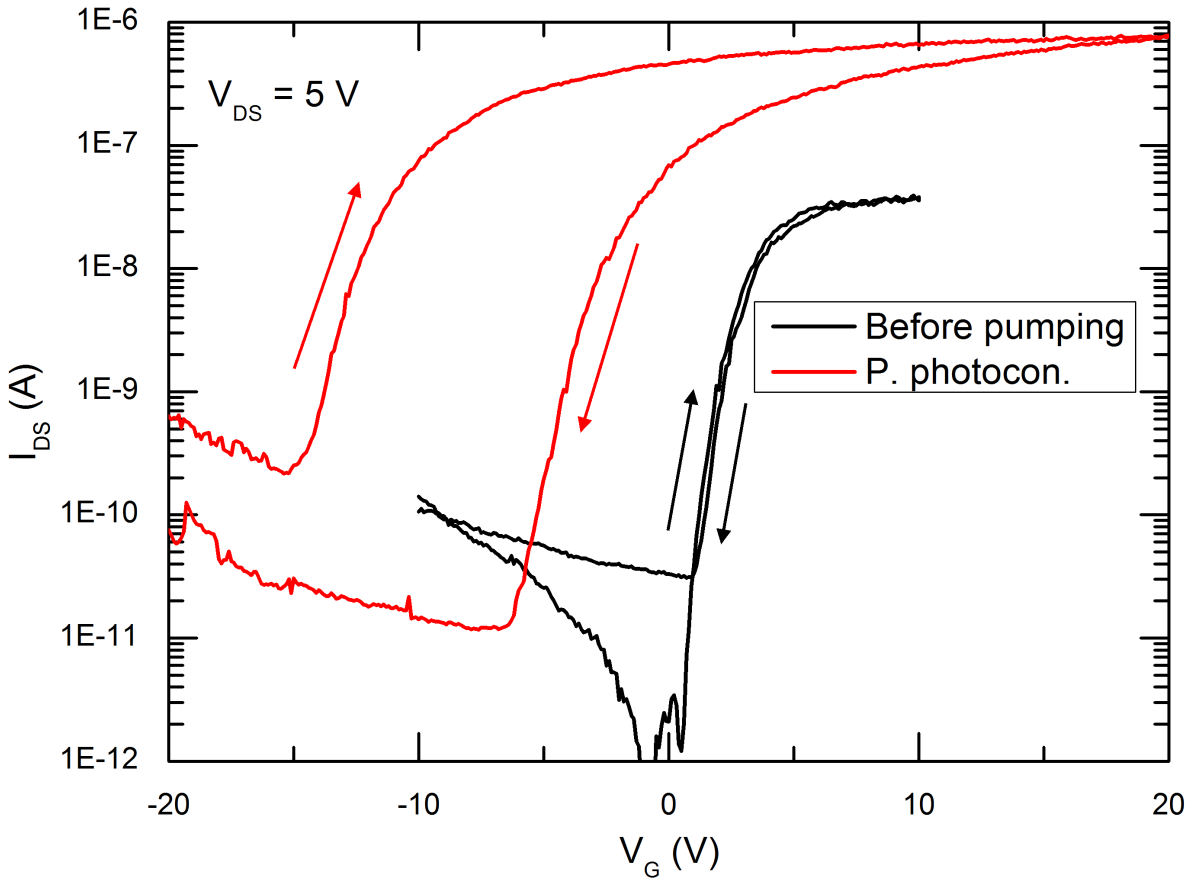

Figure 6.17: Transfer characteristics of the hierarchical nanowire FET taken before pumping (black) and during persistent photoconductivity (red).

chical nanowires [113, 118]. This suggests that while the surface states play a role in determining the threshold voltage of the device, they may not determine the field dependency of the nanowires.

6.4.2 Persistent photoconductivity of primary nanowire FETs

FETs which are bridged with the primary nanowire portion of the hierarchical nanowires show no field dependence, as demonstrated in Figure 6.10. To gauge the impact of the depleting surface states on these devices, a primary nanowire bridged device was connected to the cryostat and persistent photoconductivity measurements were performed. Figure 6.18 shows the persistent photoconductivity of the primary nanowire FET. The FET exhibits a stable dark current before the UV is switched on, after which the drain current rapidly increases by an order of magnitude. This photoconductivity is largely persistent after the UV source is turned off, although a small decrease is observed over several hours with further small decreases once the vacuum is opened. While both the primary and secondary nanowire FETs show a persistent response to UV illumination, the marked difference in their magnitude suggests that depleting surface states play a much larger role in determining the charge carrier concentration of the nanowires.

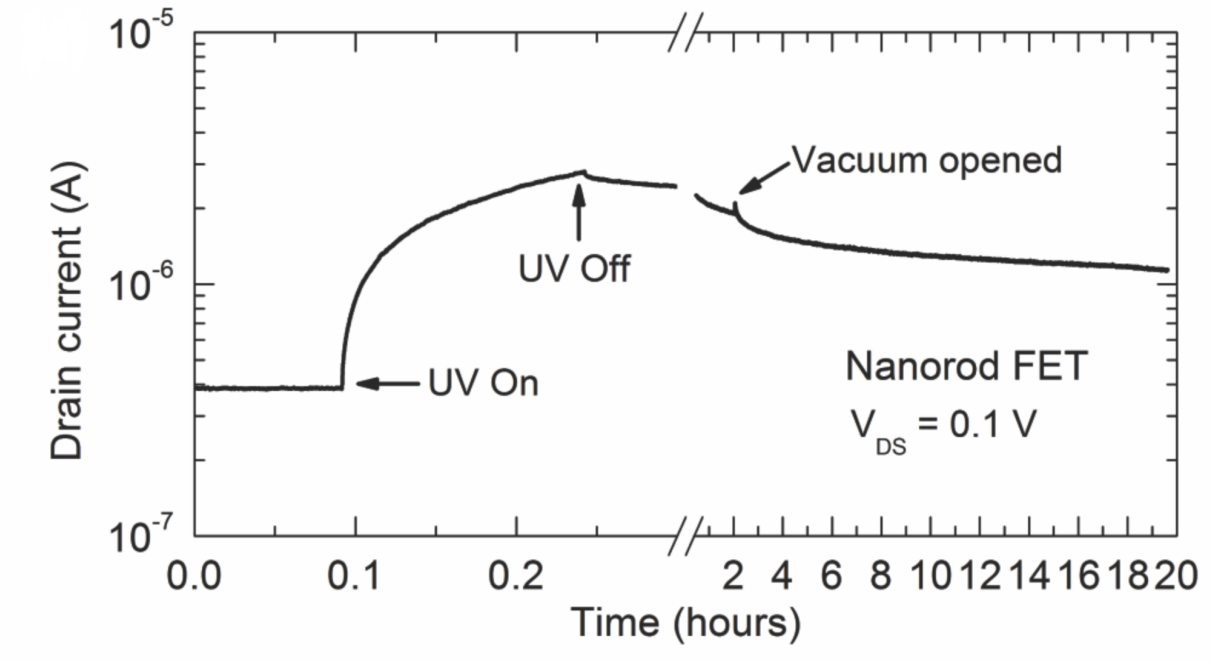

Figure 6.18: Persistent photoconductivity measurements of a primary nanowire FET. The device is driven at V_{DS} = 0.1 V.

6.5 Conclusion

In conclusion, a PEI-mediated hydrothermal growth is shown to reliably fabricate lateral hierarchical nanowires using 3 different molecular weights of PEI. These hierarchical nanowires consist of large primary nanowires, which abruptly terminate in significantly thinner, longer secondary nanowires. Both of the primary and secondary nanowires are monocrystalline, and share an epitaxial common c-axis at their interface. The growth substrates are designed to also function as device substrates, which allow for direct measurements of the primary and secondary nanowires as FETs. FETs which are bridged by the secondary nanowire portion of the hierarchical nanowires show clear field dependence, despite being measured immediately after growth without any annealing or post-growth processing. In contrast, FETs bridged with the as-grown primary nanowires show no field dependence, which is consistent with other reports of ZnO nanowire FETs in the literature.

The secondary nanowire FETs show good device performance, with on-off ratios of 10^3 to 10^5 and threshold voltages between -7.5 V to 5 V. Persistent photoconductivity measurements show that the secondary nanowire surfaces are covered in depleting surface states, which play a strong role in determining the threshold voltage of the FETs. These depleting surface states act as a competing defect mechanism to intrinsic electron donors, which also plays a role in determining the field dependence of the nanowires.

Chapter 7

Modular growth of lateral hierarchical ZnO nanowire FETs

7.1 Introduction

One of the main struggles of creating ZnO nanowire field-effect transistors is to synthesise nanowires which exhibit field dependence [11]. In Chapter 6, hierarchical nanowires which showed clear field dependence were successfully synthesised. These hierarchical nanowires did not require any post-growth annealing or other processing, which is significantly different from most ZnO nanowires [11]. The mechanisms behind the growth of hierarchical ZnO nanowires (discussed in Chapters 6 and 5) are attributed to an initial growth phase driven by regular interactions of hydrothermal precursors, which is then followed by a distinctly different second growth phase mediated exclusively through PEI-Zn^{2+} complexes. These complexes decay through a Mannich reaction, releasing Zn^{2+} ions back into solution [75]. These two growth phases take place during a single hydrothermal growth, which allows for the rapid fabrication of field-dependent ZnO nanowire FETs.

Instead of relying on a PEI-mediated growth process over a single hydrothermal growth, it would be ideal to separate the two distinct growth phases into two modular hydrothermal growths, neither of which necessarily rely on PEI. The modular synthesis of hierarchical nanowires is achieved in this chapter, with the first growth responsible for the growth of primary nanowires, and the second growth responsible for the growth of secondary nanowires. These hydrothermal growths initially contain PEI, although the optimum growth recipes for maximum hierarchical nanowire yield neglect PEI entirely. The primary modular hydrothermal growth is preheated for 20 or 60 minutes, and lasts for 6 hours. The second modular growth is preheated for 3 hours, and takes place over 19 hours. These optimised recipes yield hierarchical

nanowires 50% of the time.

Electrical measurements of the twice-grown hierarchical nanowires show that they are relatively field-independent when measured as-is, unlike the PEI-mediated hierarchical nanowires grown in Chapter 6. Field dependence is achieved by measuring in a liquid environment using de-ionised H_2O as a liquid gate dielectric, in conjunction with a reference electrode or a back gate electrode. Liquid-gated hierarchical nanowire FETs show good device characteristics when used in conjunction with a reference electrode, with threshold voltages as low as 0.45 V and subthreshold swings as low as 82 mV/decade. A liquid back-gated FET also shows reliable field dependence, with an on-off ratio as high as 10^5, and a threshold voltage of 8 V. The implementation of a liquid gate may allow the FETs to be used as sensors for biological applications.

7.2 Hierarchical nanowire synthesis

7.2.1 Theory and motivation

In Chapter 5, vertical hierarchical ZnO nanowires were grown by including 4 mM of PEI(1300) in the hydrothermal growth solution. These nanowires were composed of a 'primary' nanowire which nucleated directly from the substrate, and a comparatively finer 'secondary' nanowire, which nucleated from the terminating end of the primary nanowire. The proposed hierarchical nanowire growth mechanism involved two distinct growth phases. The first growth phase was responsible for synthesising the primary nanowires, and was driven by direct and indirect crystallisation of ZnO from Zn^{2+} ions. In turn, the secondary nanowires were synthesised during the second growth phase, which was driven exclusively by the crystallisation of Zn^{2+} ions supplied in the growth solution by a PEI-mediated Mannich reaction [75]. Likewise, PEI-mediated lateral hierarchical ZnO nanowires were grown in Chapter 6, and were also attributed to a combination of primary and secondary growth phases, with the second growth phase driven by the crystallisation of PEI-mediated Zn^{2+} ions.

In both instances, the vertical and lateral hierarchical ZnO nanowires are grown over the course of a single hydrothermal growth, with complex interactions between the PEI and regular precursors causing the two distinct growth phases. Although coupling the two growth phases in a single hydrothermal growth has some advantages, it would also be useful to separate the two growth phases into two distinct hydrothermal growths. This would enable a greater level of control over each respective growth phase, thereby offering more control over the growth of the primary and secondary

nanowires. Furthermore, if the two growth phases could be separated, PEI could possibly be omitted entirely, which could possibly lead to a more facile and predictable hierarchical nanowire synthesis route.

The synthesis of lateral hierarchical nanowires through two separate hydrothermal growths is shown schematically in Figure 7.1. Lateral growth substrates (shown in Figure 7.1(a)) first undergo a hydrothermal growth resulting in primary nanowires which extend from the exposed ZnO sidewall, as shown in Figure 7.1(b). The samples then undergo a second hydrothermal growth, causing secondary nanowires to hierarchically nucleate from the tips of the primary nanowires, as in Figure 7.1(c). In order to achieve a significant difference in diameter between the primary and secondary nanowires, the second hydrothermal growth must use a drastically reduced precursor concentration [64, 97, 188, 48]. This occurs naturally for hierarchical nanowires grown using PEI in a single hydrothermal growth, as the PEI-mediated Zn^{2+} ion source driving the second growth phase occurs only after the bulk of the original precursors have been exhausted. If the initial hydrothermal growth is simply repeated twice, the growth solution is effectively refreshed, which is a well-established technique to grow longer nanowires while maintaining or increasing their diameter [10, 69, 189].

7.2.2 Experimental details

To initially test the viability of a two-growth approach to synthesizing lateral hierarchical nanowires, growth substrates were fabricated by patterning SiO_2 (100 nm)/p^+-Si substrates with ZnO/Ti (80/50 nm) electrodes. Each substrate had 8 electrodes, with electrode gaps ranging from 10 μm to 80 μm in 10 μm increments. Primary nanowires were hydrothermally grown from these substrates in a hydrothermal growth solution containing 25 mM of $Zn(NO_3)_2$/HMT, along with 3 mM of PEI (M_W = 2000 g/mol). The hydrothermal growth solution was preheated for 20 minutes at 95 °C before the patterned growth substrates were placed into the growth solution. The patterned growth substrates were kept in the growth solution for 19 hours before being removed, and were consequently rinsed with de-ionised water and dried with N_2 at room temperature.

After the first hydrothermal growth was completed, the secondary hydrothermal growth solution was prepared using 2.5 mM of $Zn(NO_3)_2$/HMT and 0.3 mM of PEI (M_W = 2000 g/mol). The concentration of these precursors is 10% of the concentration used in the primary nanowire growth. The second hydrothermal growth solution was preheated for 3 hours at 95 °C before the primary nanowires were introduced. After 19 hours, the now twice-grown substrates were removed from the second

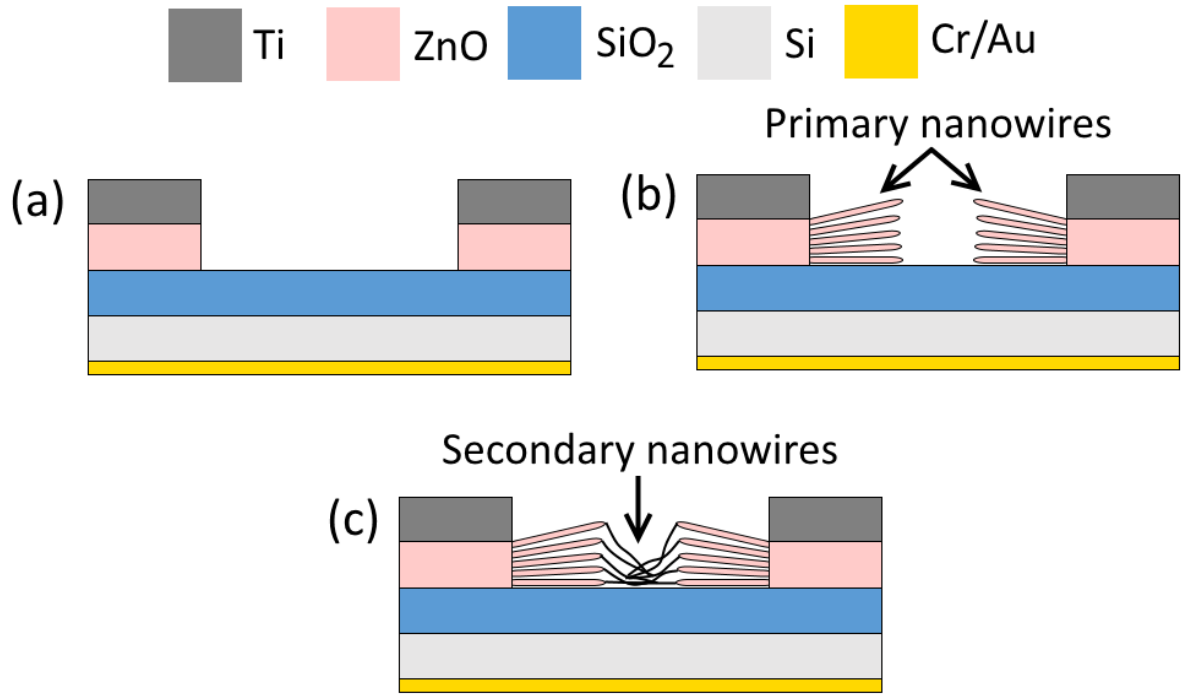

Figure 7.1: (a) The growth substrates used in the fabrication of twice-grown hierarchical nanowires. ZnO seed layers sit atop an SiO_2/Si ensemble, and are in turn capped with Ti. This only leaves the sidewall of the ZnO seed layer exposed. ZnO nanowires nucleate and grow from the exposed ZnO sidewall during the first hydrothermal growth (b). A second hydrothermal growth follows, resulting in the growth of secondary nanowires from the primary nanowires, as shown in (c).

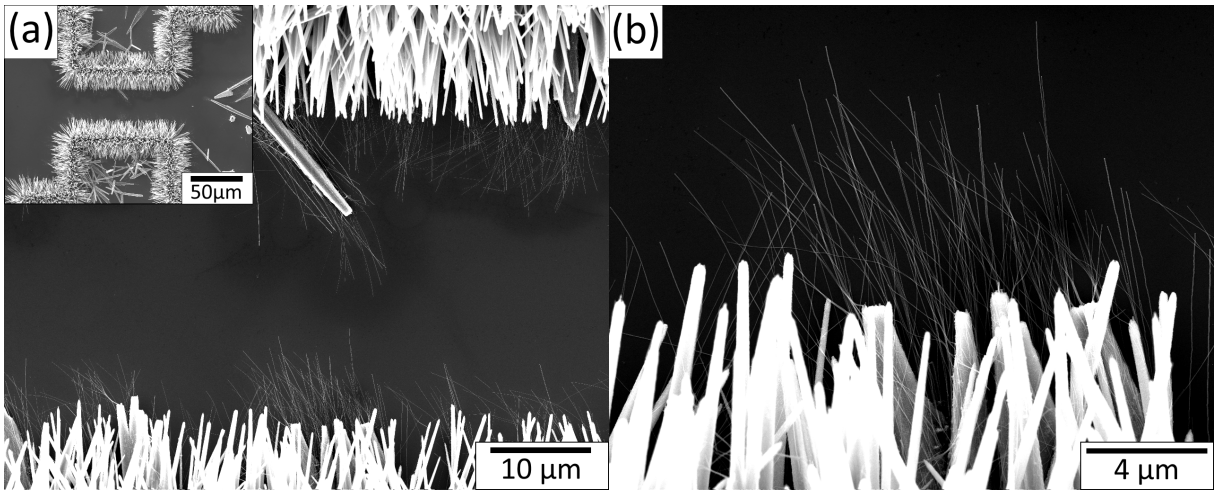

Figure 7.2: (a) A top-down view of an interelectrode channel showing hierarchical nanowires growing from the ZnO seed layer. Large primary nanowires, synthesised during the first hydrothermal growth, grow from the sidewall of the ZnO seed layer. These primary nanowires terminate in much thinner secondary nanowires, which are synthesised during the second hydrothermal growth. The inset to the figure shows a broader picture of the two electrodes. (b) A closer view of the primary/secondary nanowires. The secondary nanowires lie flush with the SiO_2 substrate.

growth solution, rinsed with de-ionised water, and dried with N_2 at room temperature.

The fabrication process of the substrates is described in detail in Chapter 4, while the hydrothermal growth and roles of the various precursors are discussed at length in Chapter 2.

7.2.3 Initial results

Figure 7.2 shows an SEM image of one of the twice-grown samples from a top-down perspective. Large primary nanowires, synthesised during the primary growth, nucleate laterally in a 180° arc from the ZnO sidewalls, as shown in the inset to Figure 7.2(a). It is believed that partially etching the ZnO layer under the Ti capping layer can restrict this effect for optimised devices, but this has not performed on these samples. These primary nanowires have lengths of 15 to 20 μm and diameters of 0.5 - 1 μm. Secondary nanowires, 20 - 50 nm in diameter and up to 10 μm in length, hierarchically nucleate from the tips and surfaces of the primary nanowires. A portion of these secondary nanowires lie flush along the dielectric of the substrate, clearly shown in Figure 7.2(b), capable of bridging pairs of electrodes.

Figure 7.3 shows the sample from a cross-sectional perspective. The cross-section of a single channel is shown in Figure 7.3(a). At this scale, the two arcs of primary

nanowires growing from the ZnO sidewalls (indicated by arrows) are clearly visible, while the ZnO/Ti seed layer is too thin to be clearly discerned. A close-up of a single primary growth arc is shown in Figure 7.3(b), showing the 180° arc the primary nanowires make. Figure 7.3(c) shows the centre of the arc, where the primary nanowires have nucleated from. The primary nanowires share a common ZnO agglomerate that has grown from the seed layer during the primary growth. Secondary nanowires can be seen hanging down from the primary nanowires. A close-up of the seed layer and common ZnO agglomerate is shown in Figure 7.3(d). Nucleation of ZnO at the sidewall during the primary growth has forced the ZnO seed layer to partially delaminate and curl in on itself, which allows the primary nanowires to grow in an arc rather than confined strictly to the surface of the substrate.

Hierarchical nanowires were isolated from growth substrate and placed on carbon grids to investigate their crystal structure. Transmission electron microscopy (TEM) measurements were carried out by Dr. Jerome Majimel and Uli Castanet. Figure 7.4 shows TEM images of the twice-grown hierarchical nanowires. The primary nanowires, shown in Figure 7.4(a) and (b), are coated in an agglomerate of ZnO nanoparticles from the second hydrothermal growth. These nanoparticles have different crystal orientations in relation to the primary nanowires, as evidenced by the high-resolution image shown in Figure 7.4(b). These nanoparticles give the primary nanowires a feathery texture, rather than the smooth texture of a single crystal that would be expected from a primary-only nanowire growth. The interface between a primary and secondary nanowire is shown in Figure 7.4(c). The secondary nanowire consists of the same ZnO nanoparticles that coat the primary nanowires. These nanoparticles have self-assembled and orientated into a nanowire structure. The individual crystal orientations of the nanoparticles are shown in Figure 7.4(d). From these measurements, it is clear that the secondary nanowires are polycrystalline, rather than single crystals, and also have a similar texture to the primary nanowires.

7.3 Optimisation for reproducibility and device fabrication

The initial results in the previous section clearly demonstrate the feasibility of growing hierarchical nanowires through two separate hydrothermal growths. This is in contrast to the hierarchical nanowires synthesised in Chapters 5 and 6, where the primary and secondary growth phases occur over the course of a single hydrothermal growth. In these instances, the primary nanowire growth is driven by a multitude of Zn^{2+} ion complexes directly and indirectly crystallising, while the second growth phase is driven exclusively through the gradual release of PEI-chelated Zn^{2+} ions via a

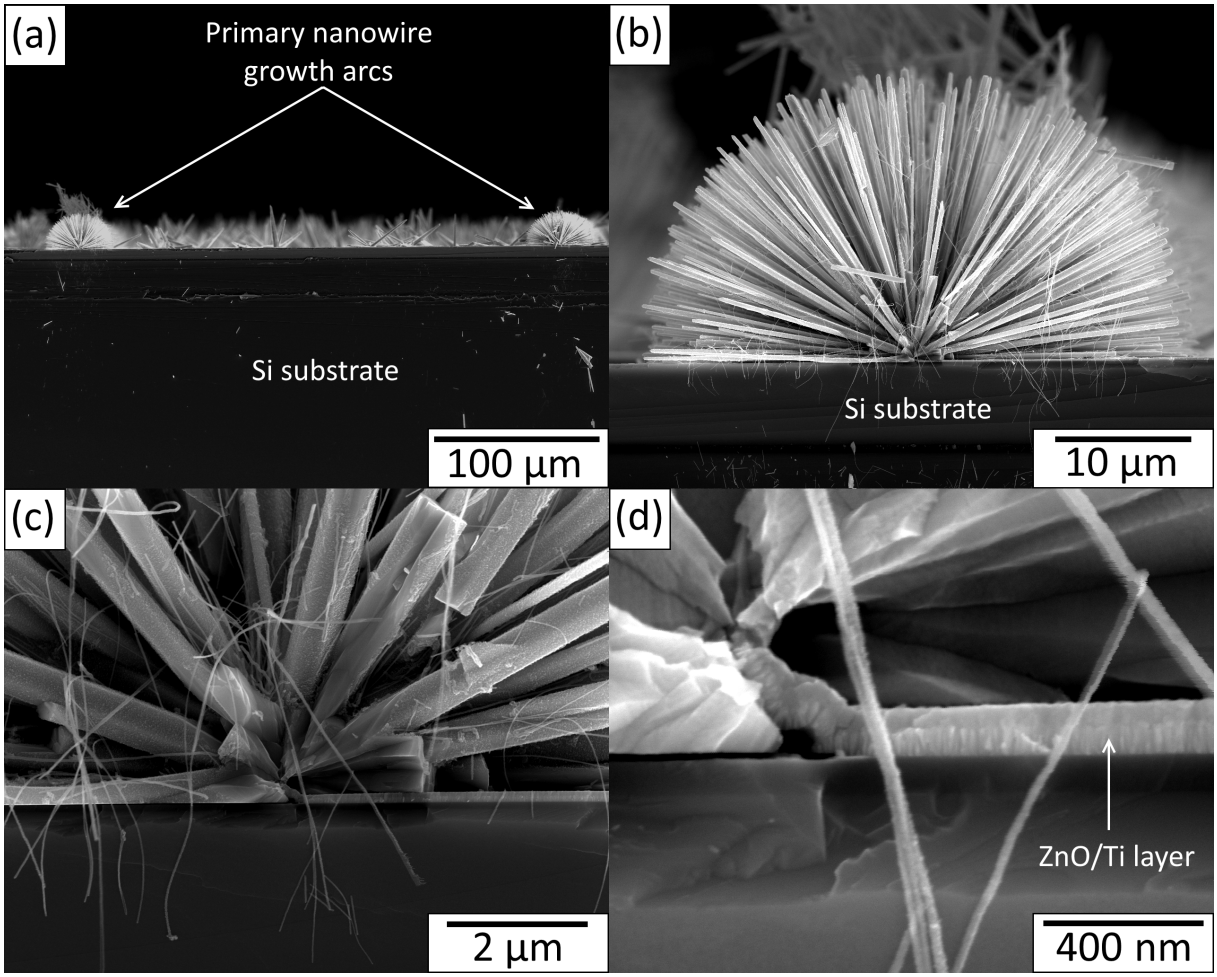

Figure 7.3: (a) A cross-section of a ZnO electrode after undergoing two consecutive hydrothermal growths. The primary nanowires are indicated by arrows. (b) A closer view of a single edge of the ZnO seed layer. The primary nanowires clearly grow in a 180° arc. (c) A higher magnification image of the centre of the primary growth arc. The primary nanowires all collectively share an agglomeration of ZnO as their nucleation point, which has grown over the course of the primary growth. (d) A high-magnification image of the interface between the common ZnO agglomerate and the seed layer. The seed layer has partially delaminated during the primary growth, exposing the underside of the layer to the hydrothermal growth solution.

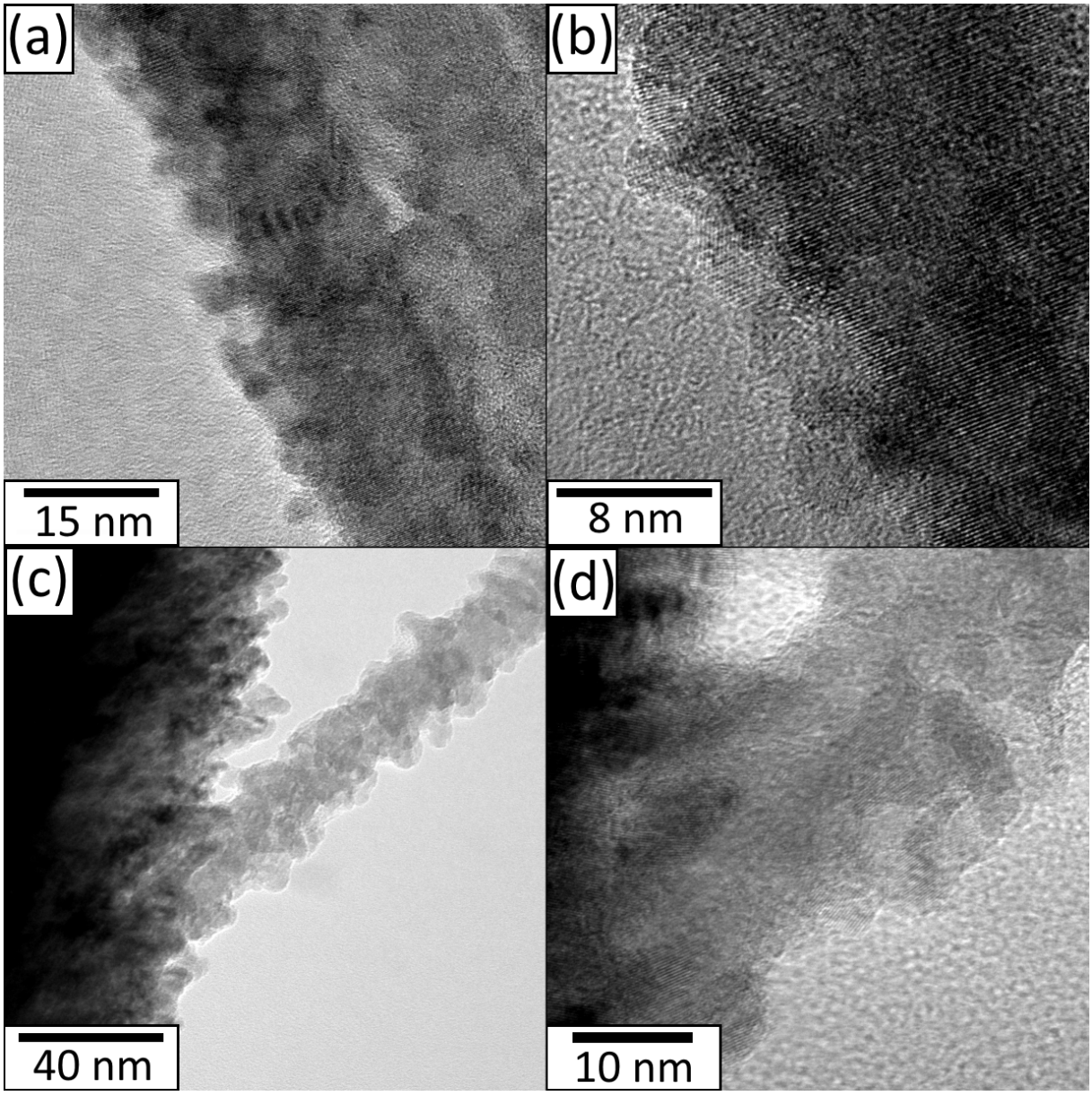

Figure 7.4: (a),(b) Transmission electron microscopy images of primary nanowires, showing nanoparticle accumulation on the surface. (c),(d) The primary/secondary nanowire interface.

Mannich reaction [75]. However, while the primary and secondary growth phases are assigned to separate hydrothermal growths in Section 7.2, PEI was included in both of these hydrothermal growths. This naturally raises the question of whether PEI is necessary in either or both of the hydrothermal growths for the reproducible synthesis of secondary nanowires. As the two hydrothermal growths are distinct and separate, we can elucidate the role of PEI by including or excluding it in each respective growth, and noting whether there is any effect on the reproducibility or morphology of the secondary nanowires.

Similarly, the separation of the primary and secondary growth phases allows us to vary the parameters of each hydrothermal growth individually, and investigate the effect on the reproducibility of the hierarchical nanowire synthesis. In this section, the preheat time of the primary growth is systematically varied, along with the inclusion of PEI in both the first and second hydrothermal growth. This ultimately allows for the reliable synthesis of hierarchical nanowires and the fabrication of electronic devices.

7.3.1 Hydrothermal growth details

Primary hydrothermal growths were prepared using 25 mM of HMT/$Zn(NO_3)_2$ as basic precursors, as in Section 7.2. To test the influence of PEI on the primary growth, 3 mM of PEI(M_W = 2000 g/mol) was included with the standard precursors for those grown with PEI, and was omitted for those grown without PEI. The primary hydrothermal growth bottles were preheated for 0 minutes, 20 minutes, or 60 minutes, both with and without PEI. Four growth substrates (identical to those described in Section 7.2) were placed into each of these primary hydrothermal growth bottles after their respective preheat, and were removed after 6 hours. This comparatively short growth time was chosen to decrease the likelihood of unintentionally bridging pairs of electrodes with primary nanowires by reducing their overall length. The short growth time also ensures that secondary nanowires don't grow through a PEI-mediated second growth phase during the primary growth, as in Chapters 5 and 6. Three identical bottles of each preheated hydrothermal growth (with and without PEI) were prepared to test for the overall reproducibility of the hierarchical nanowire synthesis.

After the primary hydrothermal growth was completed, the growth substrates were removed and rinsed with DI water. Secondary hydrothermal growth solutions were prepared using 2.5 mM of HMT/$Zn(NO_3)_2$, both with and without 0.3 mM of PEI(M_W = 2000 g/mol). These secondary hydrothermal growth bottles were all preheated for 3 hours. Each individual growth substrate from a given primary growth was placed into its own secondary growth bottle. As each primary growth

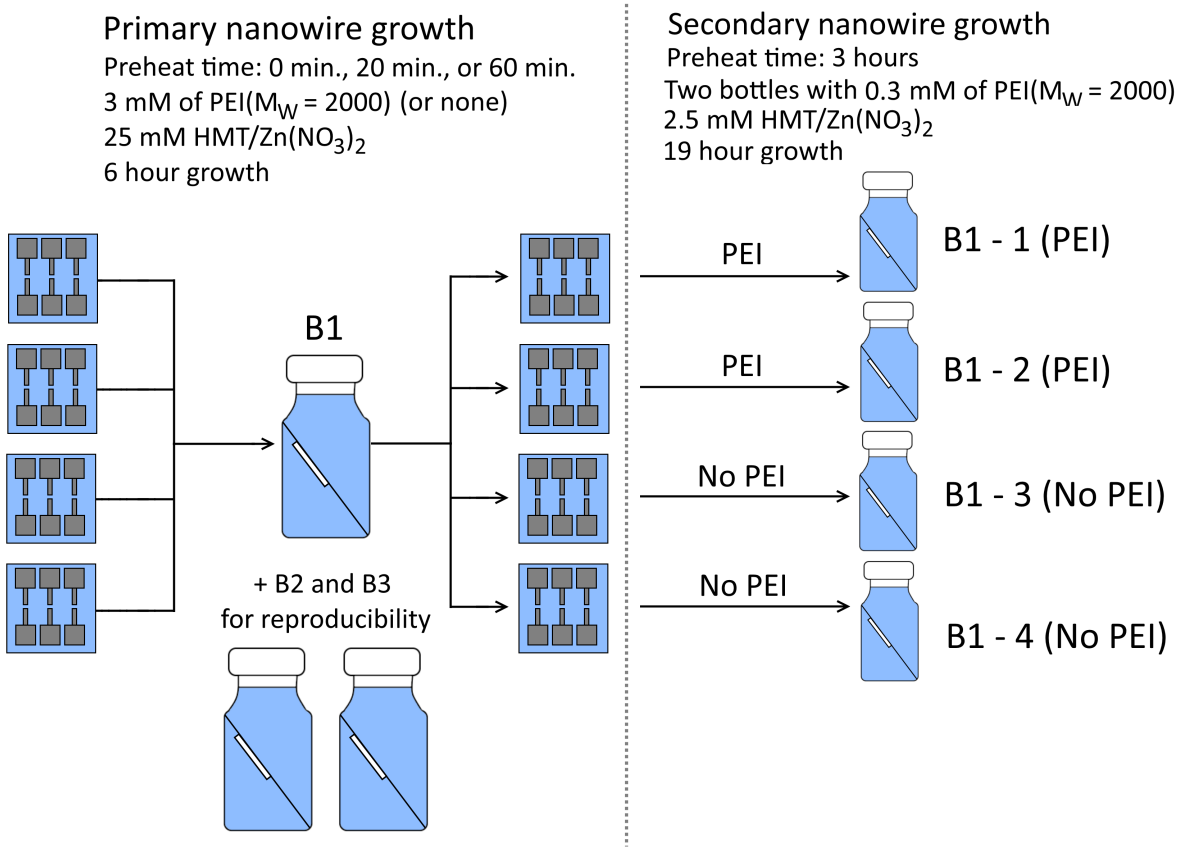

Figure 7.5: The growth flow of a particular fixed set of variables for the primary growth. Four substrates are included in a single primary growth bottle, which are then individually placed into secondary growth bottles.

bottle contained four separate growth substrates, four secondary growth bottles were prepared for each primary growth bottle. Two of these secondary growth bottles contained PEI along with the standard precursors, while the other two secondary growth bottles omitted PEI. This allowed for comparisons of growths both with and without PEI in the primary growth, and with and without PEI in the secondary growth. The individual second-grown substrates are removed from the hydrothermal growth solution after 19 hours, rinsed in DI, and dried with N_2 at room temperature. The process flow of the primary and secondary growth is shown in Figure 7.5 for clarity.

7.3.2 Effect of preheat on the primary growth

As the primary hydrothermal growth solution heats up after being placed in the waterbath, the dissolved precursors are thermodynamically driven to interact with one another. This causes the Zn^{2+} ions to form complexes, leading to the direct and indirect crystallisation of ZnO, as described in Chapter 2. Supersaturated ZnO within the solution can homogeneously precipitate out of solution, or heterogeneously

nucleate at energetically favourable sites [190, 58, 40]. While the hydrothermal growth solution is preheating in the absence of a growth substrate, heterogeneous nucleation can only occur on the glass walls of the growth bottle. This ensures that the majority of ZnO nucleation during the preheat phases is homogeneous, with ZnO directly precipitating out of solution, with the rate of homogeneous precipitation declining over time as the precursors are exhausted.

In comparison, when the hydrothermal growth takes place with growth substrates present in the solution, ZnO can heterogeneously nucleate onto energetically favourite sites on the substrate. These sites are typically along the exposed ZnO sidewall of the patterned ZnO seed layers, but ZnO can also unintentionally nucleate directly on the surface of Ti capping layer or the SiO_2 dielectric. The likelihood of nucleation and growth of ZnO on the SiO_2 surface is related to the concentration of precursors in the growth solution This means that the longer the growth solution has been preheated for, and the more Zn^{2+} ions have been complexed or precipitated out of solution, the less overall ZnO nucleation there is on the substrate surface. Conversely, if the hydrothermal growth solution has been preheated for an inadequate amount of time, or hasn't been preheated at all, there is often a correspondingly high amount of ZnO precipitation on the SiO_2 surface.

Figure 7.6 shows optical images of primary nanowires grown after a 0 minute, 20 minute, and 60 minute preheat, all grown without PEI over 6 hours. The comparative difference in the amount of surface-nucleated ZnO (or 'debris') is clearly obvious, with a significantly larger amount of debris present on the substrate grown without a preheat. The amount of debris present on the 20 minute preheated substrate is substantially less, and in turn there is less on the substrate preheated for 60 minutes. The sample grown after a 60 minute preheat has the least amount of debris present on the SiO_2 surface, although is not totally devoid from it.

Debris are ordinarily undesirable when fabricating lateral ZnO nanowire devices as there is no way to control where they nucleate. This means they can nucleate and grow in and around inter-electrode gaps, potentially forming unintentional conduction pathways between transistor sources and drains. These conduction pathways can extend over long distances if the debris have nucleated at a sufficiently high density, which can even cause electrical shorts between source electrodes and the back gate of the transistor. These back gate shorts are presented in Section 7.4. In addition to potentially fouling the channels between source, drain, and gate electrodes, debris on the SiO_2 surface pose a unique problem for the twice-grown hierarchical nanowires presented in this chapter. When primary-grown substrates are placed in the second growth, secondary nanowires can preferentially nucleate from the ZnO nanocrystals

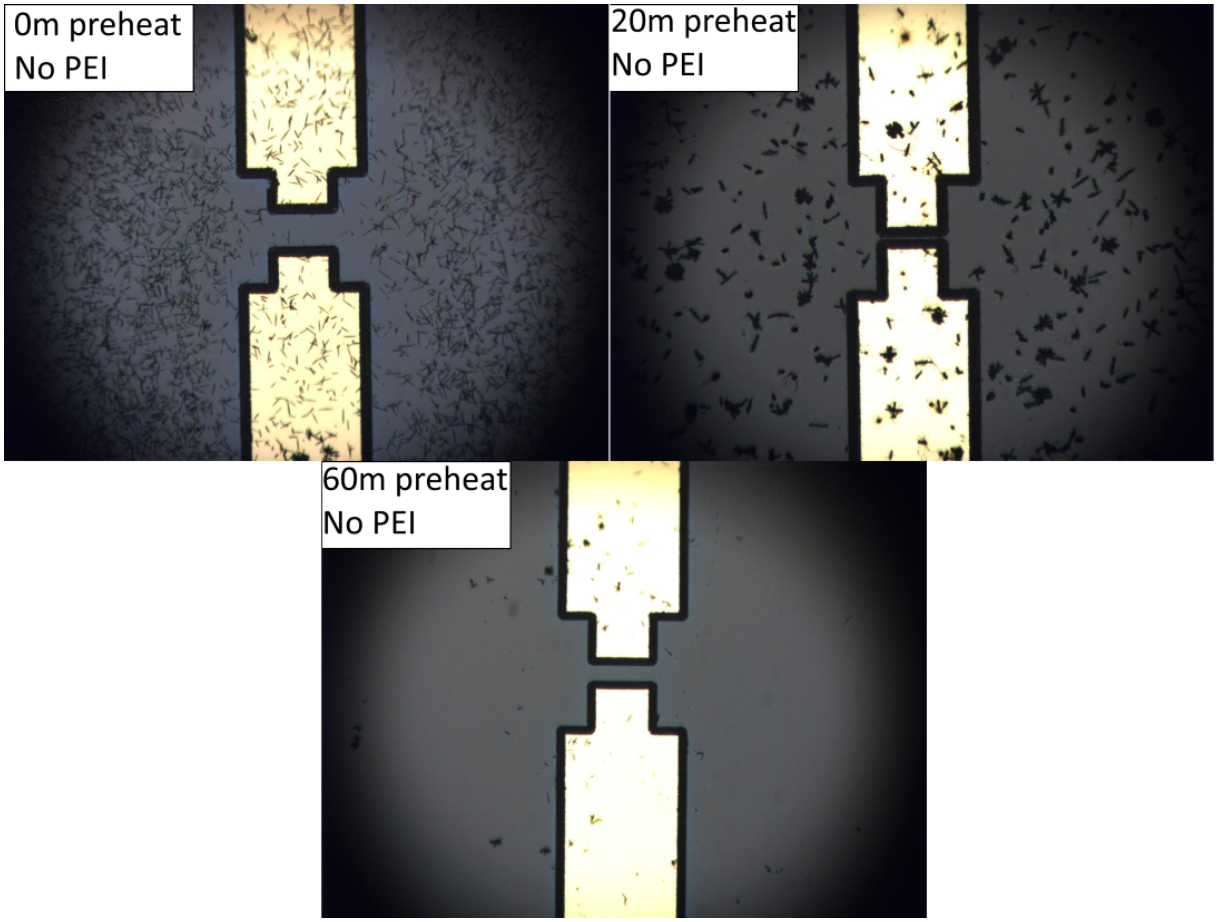

Figure 7.6: Optical images showing the relationship between the preheat of the primary growth and the density of surface-nucleated debris. The left-most sample is grown without a preheat, the middle sample is grown with a 20 minute preheat, and the right-most sample is grown with a 60 minute preheat. PEI was omitted for all of the growths.

on the SiO_2 surface, rather than from the primary nanowires themselves. As such, the surface-nucleated debris can compete with the primary nanowires for secondary nanowire growth, which can reduce the overall yield of hierarchical nanowires. These yields are presented in the next subsection.

7.3.3 Results and discussion

Systematically varying the preheat time of the primary growth, along with the inclusion/exclusion of PEI in the primary and secondary growths, can lead to drastic differences between the primary/secondary nanowires. In terms of reproducible hierarchical nanowire synthesis, the results of a given primary/secondary growth combination fall into one of three categories:

- **No secondary nanowire growth** - No secondary nanowire growth from any of the nanowires/nanostructures grown during the primary growth
- **Secondary nanowire growth from debris** - Secondary nanowire growth exclusively from ZnO nano/microcrystals which have nucleated on the SiO_2 surface of the substrate during the primary growth. Primary nanowires remain unchanged.
- **Hierarchical nanowire growth** - Successful nucleation and growth of secondary nanowires from the primary nanowires, as in Section 7.2. Secondary nanowires may also have nucleated and grown from ZnO nano/microcrystals which have nucleated on the substrate surface during the primary growth

Hierarchical nanowires are ultimately synthesised with the intention of bridging source/drain electrodes, thereby fabricating electronic devices. To this end, any growth that results in either no secondary nanowires or secondary nanowires confined to debris is considered a failure, while hierarchical nanowire growth is considered a success.

The results of the varied growths are shown in Table 7.1. Samples which showed no secondary growth are left blank and coloured red. Samples which showed secondary nanowire growth exclusively on surface-nucleated debris are labelled 'Debris' and coloured yellow. Finally, samples which showed successful hierarchical growth are labelled 'Hier. NWs' and coloured green. The top row of the table indicates the preheat time of the primary growth, and whether or not PEI is included in the growth. The left-most column indexes the individual growth substrates. As described in Section 7.3.1, three separate primary growth bottles were prepared for each set of primary growth variables (namely the preheat time and the inclusion/exclusion of PEI.) The Bx label refers to which of these three bottles the individual substrate was first grown

in. This allows us to compare twice-grown substrates which were in the same primary growth bottle, or were grown in different bottles using ostensibly identical recipes. Each primary growth bottle contained four samples, which were then individually regrown in separate growth bottles during the second hydrothermal growth. The second number in the left-most column labels uniquely identifies these substrates. The label also indicates whether PEI was included in the second hydrothermal growth, and is omitted for those which did not. The overall success rate of hierarchical nanowire synthesis by primary growth is shown in the bottom row of the table. This success rate only considers hierarchical nanowire growth (i.e. secondary growth from the primary nanowires), and disregards secondary nanowire growth from surface-nucleated debris.

Table 7.1: Yield results from secondary nanowire growths. Primary growths are indexed by column while secondary growths are indexed by row. Entries left blank failed to grow any secondary nanowires. 'Debris' refers to secondary nanowire growth exclusively from surface-nucleated debris. 'Hier. NWs.' refers to successful secondary nanowire growth from the primary nanowires.

	0 min. (PEI)	0 min. (No PEI)	20 min. (PEI)	20 min. (No PEI)	60 min. (PEI)	60 min. (No PEI)
B1 - 1 (PEI)	Hier. NWs	Debris	Debris	Hier. NWs	Hier. NWs	Debris
B1 - 2 (PEI)	Hier. NWs		Hier. NWs	Debris	Hier. NWs	Debris
B1 - 3		Debris		Hier. NWs	Hier. NWs	Hier. NWs
B1 - 4				Hier. NWs		Hier. NWs
B2 - 1 (PEI)	Hier. NWs	Debris	Debris	Debris	Debris	Debris
B2 - 2 (PEI)	Hier. NWs		Debris	Debris	Hier. NWs	Debris
B2 - 3		Debris	Debris	Hier. NWs		Hier. NWs
B2 - 4				Hier. NWs		Hier. NWs
B3 - 1 (PEI)	Debris	Debris	Debris	Debris	Debris	Hier. NWs
B3 - 2 (PEI)		Debris	Hier. NWs	Debris	Debris	Debris
B3 - 3						
B3 - 4		Hier. NWs	Debris	Hier. NWs		Hier. NWs
Success rate	33%	8.3%	16.6%	50%	33%	50%

There is a wide variety of overall success rates of hierarchical nanowire growth for the different combinations of primary and secondary growth conditions. The smallest yield of hierarchical nanowires occurs when the primary growth isn't preheated and PEI is omitted, with only one sample (B3- 4) successfully growing hierarchical nanowires. Six of the other substrates show secondary nanowire growth exclusively from surface-nucleated debris. This competition between the debris and primary

nanowires for secondary nanowire nucleation seriously affects the overall yield of hierarchical nanowires, suggesting that preheated primary growths without PEI are unsuited for device fabrication.

When PEI is included in the unpreheated primary growth, the overall yield of hierarchical nanowires increases to 33%, with secondary nanowire growth exclusively from debris restricted to a single sample. Although the overall yield of secondary nanowires from either primary nanowires or debris is lower, with a total of 7 samples showing no secondary nanowire growth from either, the rate of successful secondary nanowire growth from the primary nanowires is improved. These results suggest that the presence of PEI in the primary growth increases the preferentiality of secondary nanowire nucleation from the primary nanowires.

Both 20 minute preheated and 60 minute preheated primary growths without PEI have the equal highest rate of hierarchical nanowire fabrication, with overall yields of 50%. Each primary growth recipe yields 6 samples with hierarchical nanowires and 5 samples with secondary nanowires from debris, leaving only one sample with no secondary nanowire synthesis. In both cases, 5 of the 6 hierarchical nanowire samples are fabricated without PEI in the second growth, with 1 sample grown using a PEI-mediated second growth. This clearly demonstrates that PEI isn't necessary for hierarchical nanowire synthesis when two separate hydrothermal growths are used.

When PEI is included with the 20 minute preheated primary growth, the frequency of samples showing any secondary nanowire synthesis decreases. The yield of successful hierarchical nanowires is drastically decreased from 50% to 16.6%, while the rate of secondary nanowire nucleation exclusively on the surface debris slightly increases from 41.6% to 50%. Four samples show no secondary nanowire growth when PEI is included with the growth solution, compared to only a single sample when PEI is omitted from the growth solution. Secondary nanowire synthesis is also reduced overall when PEI is included in the 60 minute preheated primary growth. The reduction of successful hierarchical nanowire synthesis is not as drastic, decreasing from 50% to 33.3%. However, secondary nucleation from surface debris decreases from 41.6% to 25%. Similarly, the number of samples showing no secondary nanowire growth increases to 5 samples when PEI is included in the primary growth, compared to only a single sample when PEI is omitted from the primary growth. These comparisons clearly indicate that at least as far as hierarchical nanowire synthesis is concerned, omitting PEI from the primary growth leads to increased yields and better reproducibility.

It is also interesting to note the correlation between the success rate of hierarchical nanowires and the inclusion/exclusion of PEI in both the primary and secondary growths. When PEI is included in only the primary or only the secondary growth, the yield of secondary nanowires drastically drops. However, the yield improves when PEI is included in *both* the primary and secondary growths. Of the 23 hierarchical nanowire samples grown in the preheat/PEI experiments, only 3 are grown with mismatched PEI inclusion in the primary/secondary growth. This may suggest a different nucleation and growth mechanism between primary/secondary nanowires grown with and without PEI.

Figure 7.7 shows SEM images of a hierarchical nanowire device fabricated using the optimised recipe of a 20 minute preheated primary growth, with the PEI omitted from the primary and secondary growths. The primary nanowires are noticeably shorter than the initial devices fabricated previously in Section 7.2 due to the shorter primary growth time of 6 hours, versus 19 hours. Dense networks of secondary nanowires lie in the channel gaps, bridging the source/drain electrode pairs. This allows us to perform electrical measurements on the secondary nanowires and to utilise them as field-effect transistors.

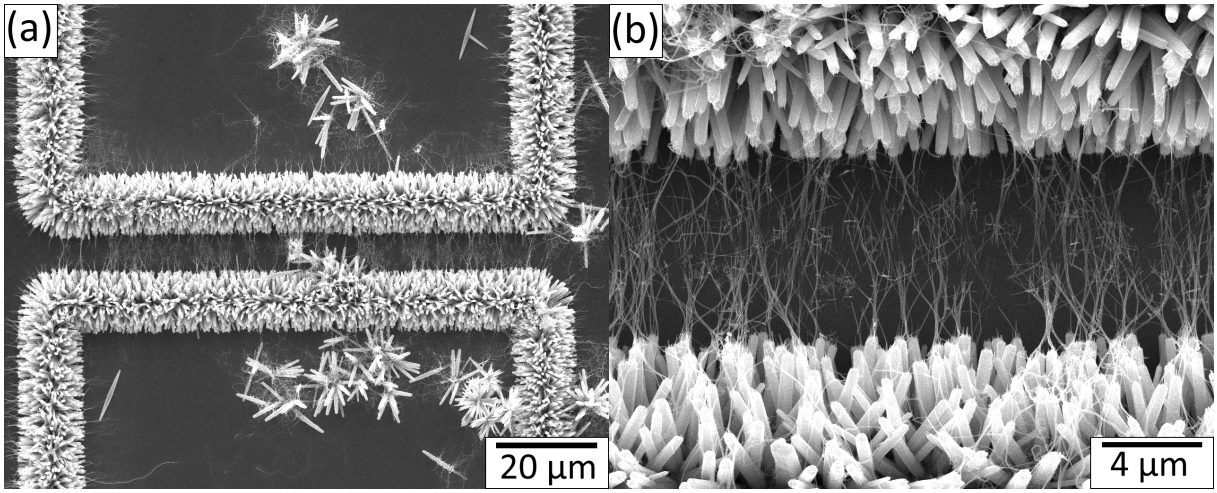

Figure 7.7: (a) A pair of electrodes bridged by hierarchical nanowires fabricated using a primary growth preheated for 20 minutes. PEI was omitted from both the primary and secondary growths. (b) A close-up of the device channel. A high density of secondary nanowires bridge the channel gap, allowing us to perform electrical measurements.

7.4 Electrical measurements

The architecture of the growth substrates used to grow hierarchical nanowires allows for electrical measurements of pairs of electrodes bridged by secondary nanowires. Each electrode consists of a thin film of ZnO capped with Ti. If the channel of the electrodes is bridged, voltage can be applied across the Ti capping layers, passing current through the bridging nanowires. The SiO_2 (100 nm)/p-Si substrate can then be used as a dielectric and back gate respectively, allowing the pair of electrodes to be used as a source and drain pair. The hierarchical nanowire substrates therefore double as device substrates. All electrical measurements presented in this section are performed using a Rucker and Kolls probe station, coupled with an Agilent 4156C parameter analyser. The experimental details of the electrical measurement set-up are described in detail in Chapter 4.

7.4.1 Unpreheated primary growths and leakage through debris

In addition to affecting the successful yields of hierarchical nanowires, the preheat of the primary growth has a strong effect on the density of debris which nucleate on the SiO_2 surface of the substrate (as discussed in Section 7.3.2.) The presence of surface debris can drastically affect the device performance by unintentionally establishing conduction paths between source/drain electrodes. In extreme cases, conduction paths can be introduced between source/gate electrodes by debris forming a continuous pathway across the SiO_2 substrate, which reach to the very edge and make contact to the back electrode. While unintentionally bridged source/drain pairs are relatively easy to observe using optical or electron microscopy, leaks between the source and gate electrodes are typically only revealed when the device is electrically measured.

As shown in Figure 7.6, samples grown with a primary growth preheated for 20 minutes or 60 minutes show debris on the substrate surface, although the overall density of the debris is too low to establish a conduction path between source electrodes and the transistor backgate electrode. However, this is not the case for samples grown using unpreheated primary growths. Figure 7.8 shows the transfer characteristics (I_{DS}-V_{DS} measurements) of the 30 μm channel of sample 0m (PEI) - B2 -2 (PEI), indexed by the convention established in Table 7.1. The device is driven at V_{DS} = 0.1 V, while the gate is swept from V_G = -10 V to 10 V. The device shows a strong leakage current (I_G) of 1.4 $\times 10^{-7}$ A at V_G = +/- 10 V due to the surface-nucleated debris. This excessively high leakage current precludes this sample from being used as an FET, even if source and drain electrodes are bridged by hierarchical nanowires.

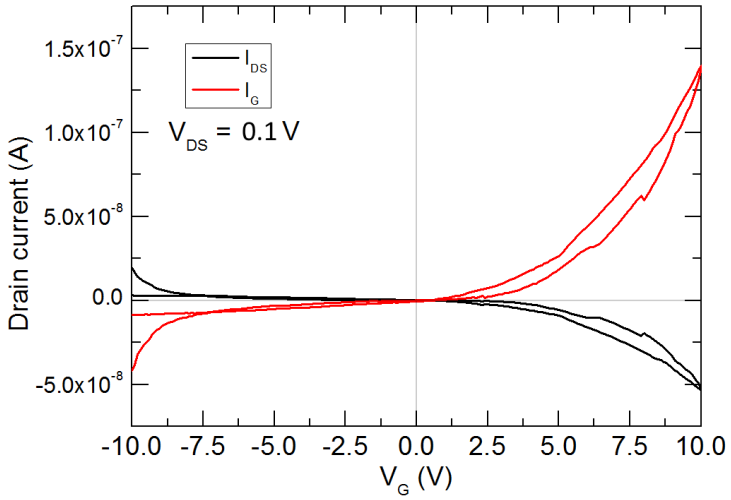

Figure 7.8: Transfer characteristics of a sample grown with an unpreheated primary growth, with PEI included in both the primary and secondary growths. The FET is driven at V_{DS} = 0.1 V. This particular device measured is the 30 μm channel of B2 - 2. The very high leakage current is caused by the high density of debris which has nucleated on the SiO_2 surface.

7.4.2 Hierarchical nanowire device measurements

Hierarchical nanowires grown with a 20 minute or 60 minute preheated primary growth don't suffer from the surface-nucleated debris to the same extent as those grown with unpreheated primary growths. This allows for output characteristic measurements (I_{DS} - V_{DS}) and transfer characteristic measurements (I_{DS}-V_G) without unintentionally measuring debris which bridge the source/drain or source/gate electrodes.

All of the hierarchical nanowire FETs fabricated in Chapter 6 showed consistent field dependence, without the need for post-growth annealing or processing. In contrast, only some twice-grown hierarchical nanowire FETs in this chapter show consistent and reliable field dependency. One of these devices is shown in Figure 7.9. This device is grown using a 20 minute preheated primary growth, without any PEI in the primary or secondary growths. The transistor is driven at V_{DS} = 1 V. This FET shows obvious field dependency, with an on-off ratio of 10^4, a threshold voltage of $\approx$0 V, a transconductance of 0.75 nS, and a subthreshold swing of 0.56 V/decade. The leakage current in this device is negligible, remaining below 10^{-10} A. These device characteristics are comparable to the hierarchical nanowire FETs fabricated in a single growth in Chapter 6, although the magnitude of the on-currents differ by 2 orders of magnitude.

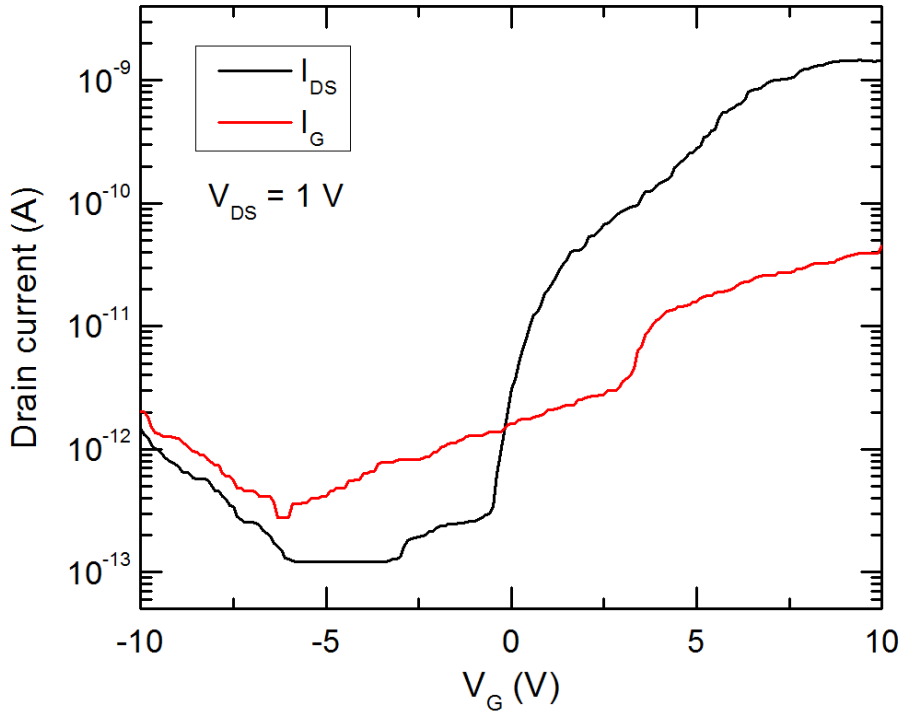

Figure 7.9: Transfer characteristics of a field-dependent FET fabricated using twice-grown hierarchical nanowires. The primary growth was preheated for 20 minutes. Neither the primary or secondary growths included PEI.

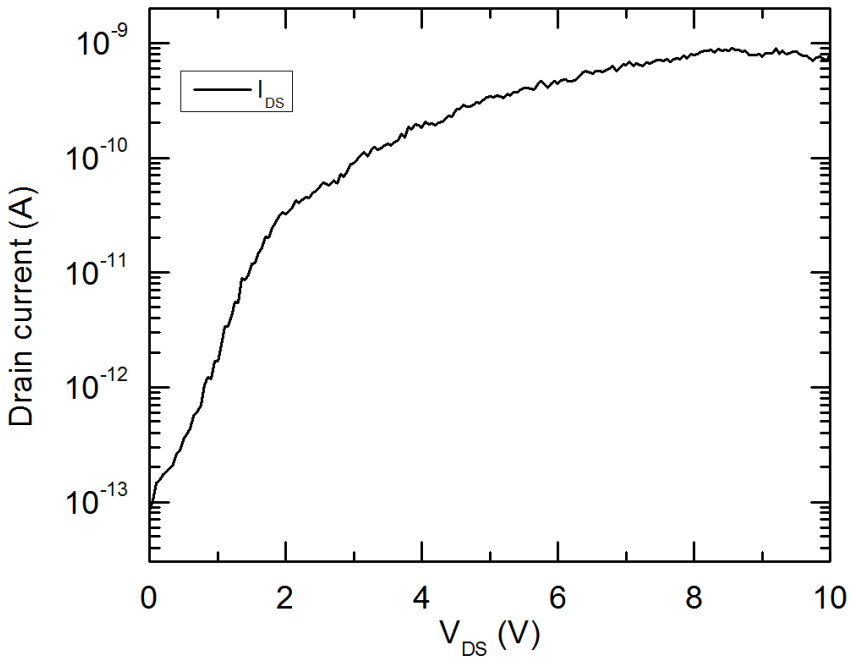

Figure 7.10: Diode measurements of a device fabricated using a 60 minute preheated primary growth. Neither the primary or secondary growths contained PEI. The measurement is taken at $V_G = 0$ V. The low current at high drain/source voltages suggest a low concentration of charge carriers.

In contrast, other devices show limited field dependence. While a lack of field dependence is typically due to excessive charge carriers caused by unintentional doping, nanowires with low charge carriers can also show a lack of field dependence. Figure 7.10 shows a diode measurement (taken at $V_G = 0$ V) of one such device. This device is fabricated using a 60 minute preheated primary growth, with PEI excluded from both the primary and secondary growths. Although the device does show conduction, the drain/source current is below 1 nA at V_{DS} = 10 V, which suggests that the hierarchical nanowires are highly resistive.

The extent of the depletion in the hierarchical nanowires significantly affects the transfer characteristics of the device, shown in Figure 7.11. The device is driven at a high voltage of $V_{DS} = 10$ V, which is necessary due to the high resistivity of the FET. Despite the high resistivity of the FET, the device shows some measure of field dependence, albeit with poorly defined on and off regimes. The FET has an on-off ratio of $\approx 10^3$, and a threshold voltage of -5 V. This suggests that the FET is operating in depletion mode, despite the high resistance of the device. The relatively low charge carrier concentration of the hierarchical nanowires is therefore unlikely to be caused by the presence of depleting surface states or other electron traps, which would necessitate a positive threshold voltage to switch the FET from off to on. Although the device shows a well-defined subthreshold regime, the drain-source current continues to rise

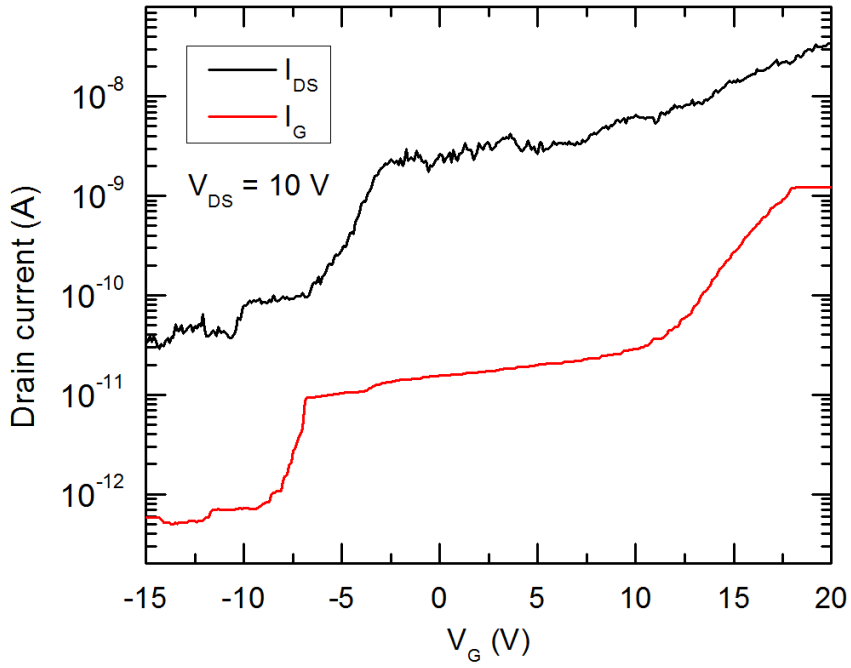

Figure 7.11: Transfer characteristics of the FET also measured in Figure 7.10. The primary growth is preheated for 60 minutes. Neither the primary or secondary growths contained PEI. The measurement is taken at $V_{DS} = 10$ V.

approximately one order of magnitude between V_G = -2.5 V to 20 V. The maximum transconductance of the device is 34 nS, and the minimum subthreshold swing is 2.14 V/decade.

Despite the above devices showing some measure of field dependence, most of the hierarchical nanowire FETs do not respond to applied gate voltages as-is. However, their field dependence can be significantly improved by utilising a liquid dielectric instead of (or in combination with) the SiO_2 layer. These measurements are described in the next subsection.

7.4.3 Liquid gating measurements

Transfer characteristics of the modular hierarchical nanowires in the previous section utilised the 100 nm thick SiO_2 layer from the substrate as the gate dielectric, although this was largely ineffective. In this section, liquid gating measurements are performed using de-ionised water as a liquid dielectric. In this configuration, the dielectric liquid and nanowires are in direct contact with each other. This covers the entire surface area of the nanowires, which allows for much more effective gating.

The gate electrode is typically directly in contact with the liquid, although the regular SiO_2/Si dielectric/gate electrode can also be used in conjunction with the

liquid dielectric. When a voltage is applied to the liquid dielectric, an electric double layer forms, which brings induced charges very close to the surface of the nanowires [191, 192, 193, 194, 195, 196]. The close proximity of the induced charge to the semiconducting nanowires causes the much more effective gating for a given gate-source voltage than would be normally achieved using the SiO_2 layer as a gate dielectric. However, extra steps must be taken to separate the source electrode from the gate electrode when using liquid gates. Despite the fact that the liquid is a highly resistive dielectric, high leakage currents can result if both the gate electrode and source electrode are in direct contact with the liquid.

Photolithography is used to insulate the source and drain electrodes from the liquid dielectric. After the hierarchical nanowires have been synthesized via the primary and secondary hydrothermal growths, the entire substrate is covered in AZ1518 photoresist. The channel area of each electrode pair is exposed to UV light using the Karl Suss MJB3 mask aligner for 60 seconds. This particularly long exposure time is used to ensure that no photoresist remains on the nanowire surface, which would insulate the nanowires from the liquid dielectric. The substrates are then developed for 40 seconds in 1:2 AZ326:DI-H_2O, rinsed in DI-H_2O, and dried with N_2 at room temperature. This photolithography step also exposes the large electrode pads to allow for contact with the probe station. Photolithography and the use of the mask aligner is explained in detail in Chapter 4.

The liquid gate architecture is shown in Figure 7.12. Deionised H_2O ($\rho \geq 18.2\mathrm{M}\Omega \cdot \mathrm{cm}$) is used as the liquid dielectric. The liquid gate electrode is an Ag/AgCl reference electrode (sourced from In Vivo Metric.) The source/drain electrodes and primary nanowires are encapsulated by the AZ1518 photoresist layer, ensuring that only the secondary nanowires are in contact with the liquid dielectric. Gating is achieved by either applying a voltage between the reference electrode and the source electrode, or between the back gate electrode and the source electrode.

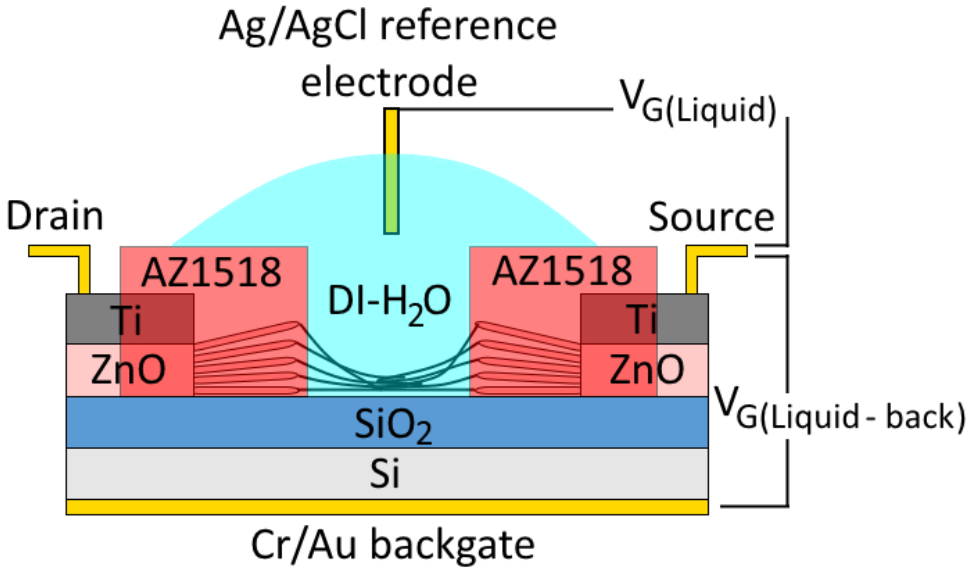

Figure 7.12: A schematic of a liquid gated hierarchical nanowire FET. The hierarchical nanowires lie in the channel between the source and drain electrodes, and are in contact with de-ionised water. The source and drain electrodes are insulated from the water by AZ1518 photoresist.

Hierarchical nanowire FETs which were otherwise unresponsive to applied fields can show marked field dependence when the liquid gate is used. Figure 7.13 shows the output characteristics of a device fabricated using a 20 minute preheated primary growth, with PEI omitted from both the primary and secondary growths. The device is clearly conductive, but shows only a minimal difference in current when V_{DS} is sweeped at V_G = -10 V and +10 V using the SiO_2/back gate. This suggests that the device is largely field-independent.

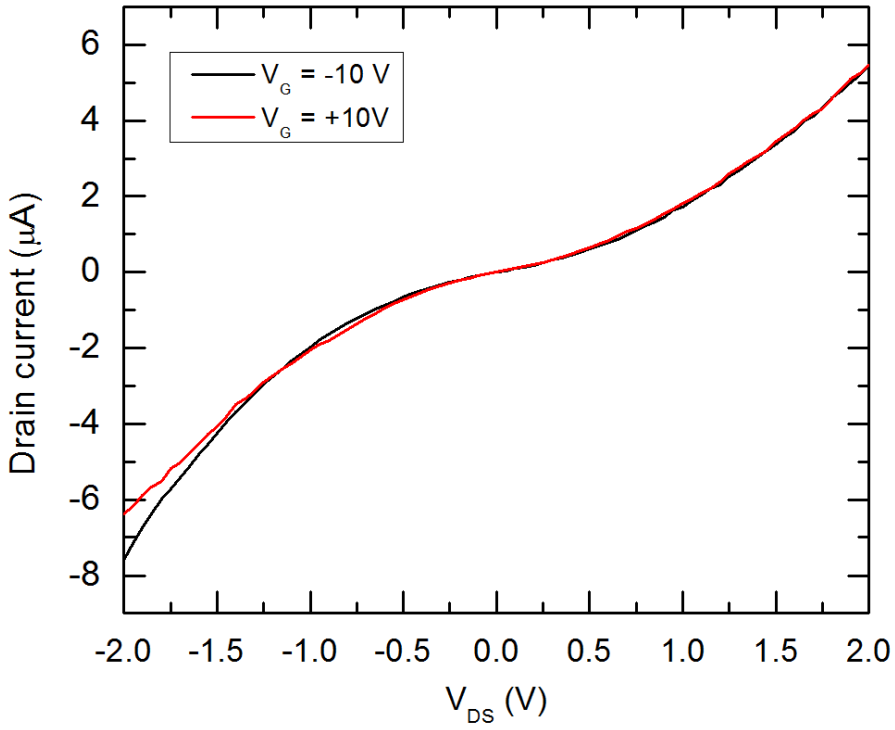

Figure 7.13: Output characteristics of a hierarchical nanowire FET taken at V_G = -10 V and 10 V. The device is fabricated using a 20 minute preheated primary growth without PEI. The output shows minimal change between the two gate voltages, suggesting the device is field independent.

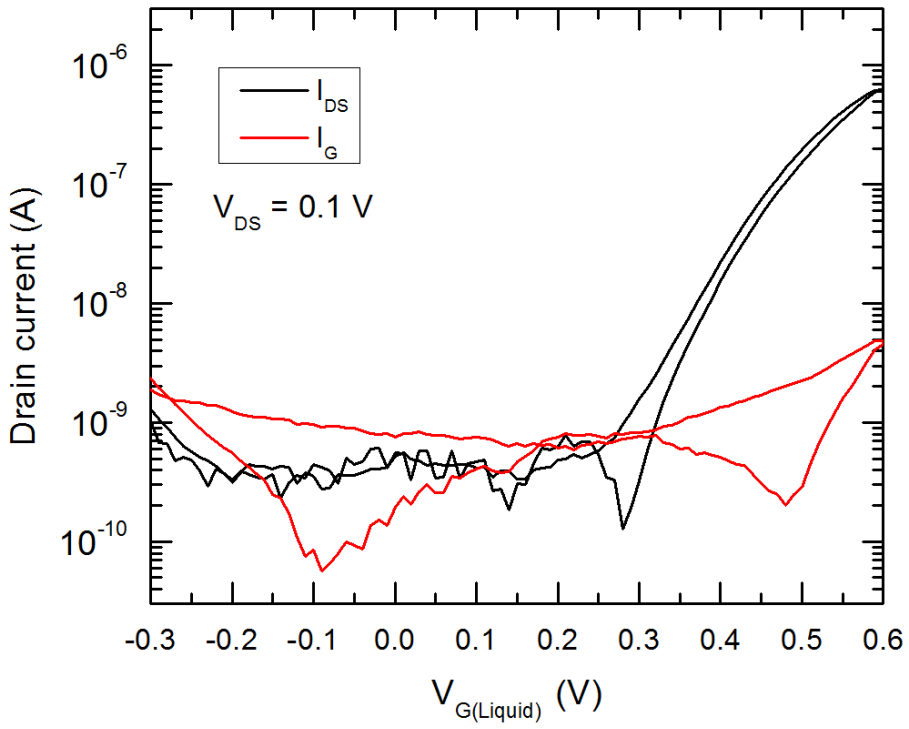

Figure 7.14: Transfer characteristics of the hierarchical nanowire FET measured in Figure 7.13. These transfer characteristics employ a liquid gate in conjunction with a reference electrode, instead of the typical SiO_2/backgate combination. Clear field dependence is achieved when the sample is measured using a liquid gate.

In contrast, the FET shows significant field dependence when a liquid gate is used. Figure 7.14 shows the transfer characteristics of the device using a liquid gate/reference electrode combination. The device is driven at V_{DS} = 0.1 V. The FET shows clear switching, with a threshold voltage of ≈0.45 V, an on-off ratio of 10^3, a transconductance of 6.43 μS, and a subthreshold swing of 88 mV/decade. The effectiveness of the liquid gating is apparent in the low threshold voltage, high transconductance, and low subthreshold swing. These device characteristics are better than the SiO_2-gated hierarchical nanowire FETs presented in Chapter 6.

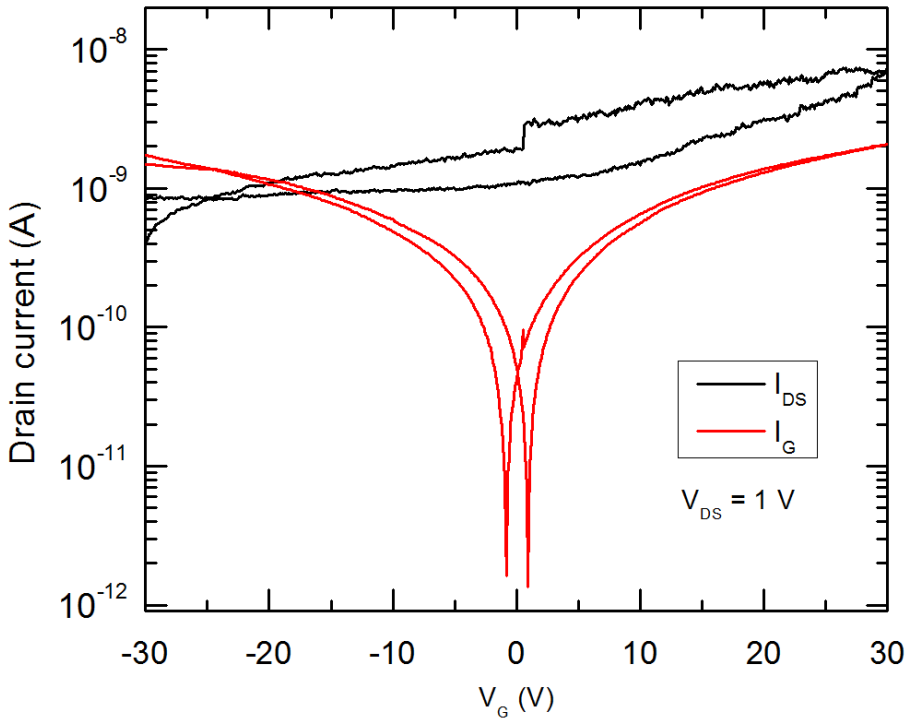

Figure 7.15: Transfer characteristics of a hierarchical nanowire FET taken at V_{DS} = 1 V using the SiO_2/backgate electrode configuration. The device is fabricated using a primary growth preheated for 20 minutes, with PEI omitted from both primary and secondary growths. The device shows very little field dependence as-is.

This behaviour is consistent across other hierarchical nanowire FETs which don't show field dependency using the traditional SiO_2/backgate configuration. Figure 7.15 shows the transfer characteristics of a device fabricated using a 20 minute preheated primary, with PEI excluded from the primary and secondary growths. The device is driven at V_{DS} = 1 V. Although the FET is subjected to relatively extreme gate voltages (+/- 30 V), the drain-source current shows only shows an order of magnitude change over the 60 volt range. This device is clearly unsuitable for FET applications as-is.

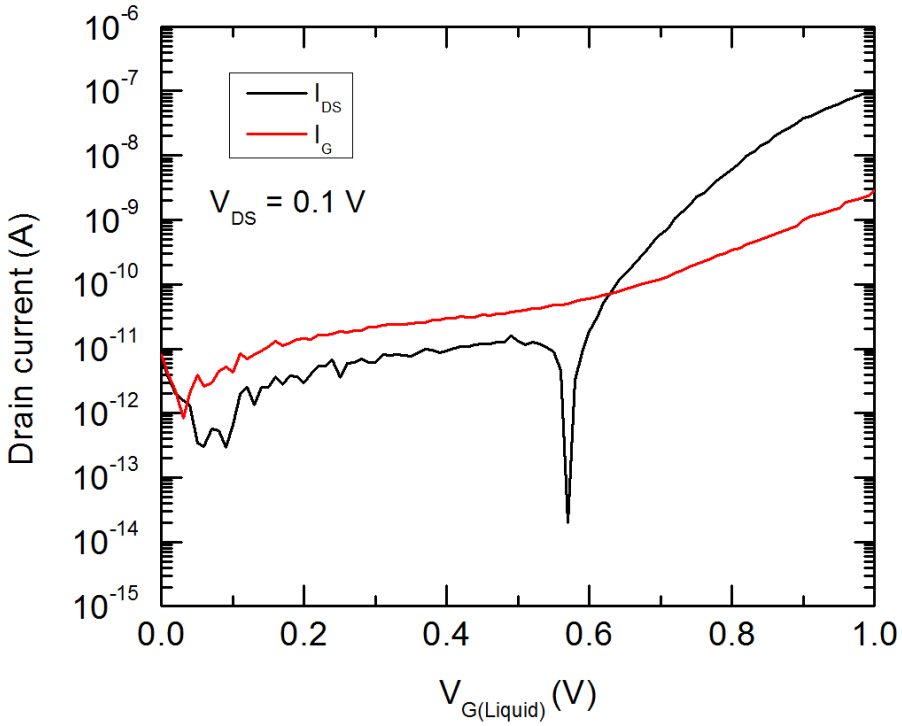

Figure 7.16: Transfer characteristics of the same hierarchical nanowire FET measured in Figure 7.15 taken using a liquid gate and a reference electrode. The FET is driven at V_{DS} = 0.1 V. Unlike the previous measurement taken with a conventional SiO_2 dry backgate, the FET shows significant field dependence.

In comparison, the device shows strong field dependence when it is liquid gated. Transfer characteristics taken using a liquid gate are shown Figure 7.16. The FET is driven at V_{DS} = 0.1 V. The device shows clear on and off regimes, with a threshold voltage of ≈0.88 V, an on-off ratio of 10^4 - 10^5, a transconductance of 0.8 μS, and a subthreshold swing of 82 mV/decade. These good device characteristics are comparable to the liquid-gated device shown in Figure 7.13, although the comparatively low transconductance is due to the lower on current of the device.

Although the liquid gate measurements in Figures 7.14 and 7.16 both use a reference electrode directly in contact with the liquid dielectric, it is possible to use the conventional SiO_2/backgate electrode with the liquid in contact with the nanowires. This is less effective than directly placing a reference electrode into the liquid droplet, as the electric field needs to propagate through the SiO_2. However, the field effect is still drastically improved in comparison to using a "dry" SiO_2/backgate combination, as the presence of the electric double layer ensures that the induced charges in the dielectric liquid are very close to the nanowires, and that the entire surface area of the nanowires is surrounded.

Figure 7.17 shows a wet backgated measurement of the FET measured in Fig-

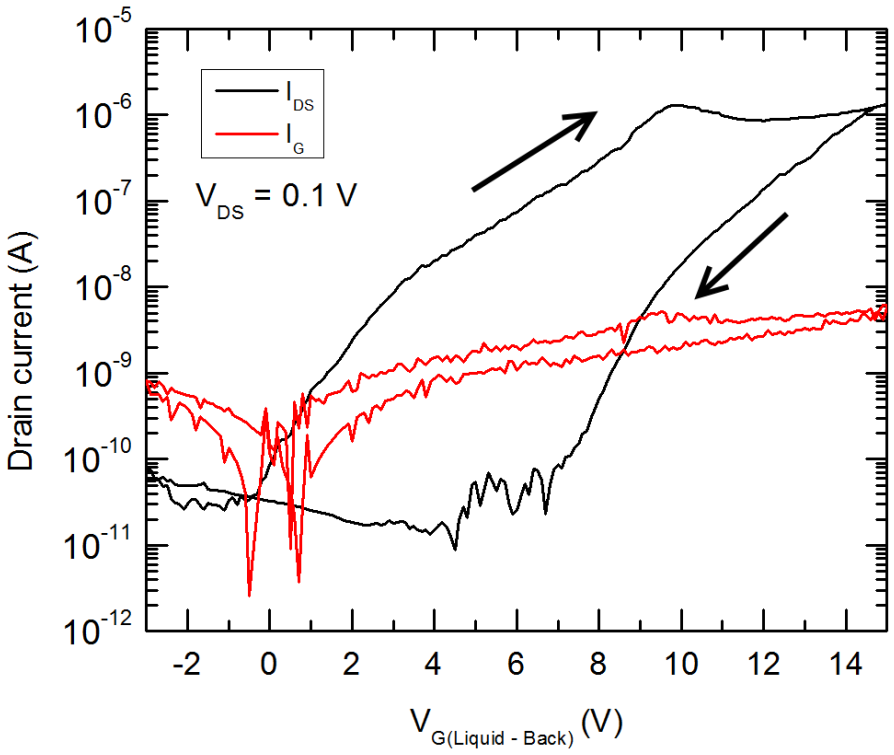

Figure 7.17: Transfer characteristics of the hierarchical nanowire FET measured in Figures 7.15 and 7.16. The transistor is driven at V_{DS} = 0.1 V. This measurement is performed with DI-H_2O on the nanowire surface, but using the regular SiO_2/substrate as the gate electrode. The SiO_2 layer consequently couples to the DI-H_2O.

ures 7.15 and 7.16. The device is driven at V_{DS} = 0.1 V. Although the liquid gate is only used as a secondary dielectric in conjunction with the SiO_2 layer, the FET shows clear field dependence, in stark contrast to the "dry" back-gated transfer characteristic shown in Figure 7.15. The FET operates at a threshold voltage of $\approx$ 8 V, with an on-off ratio of 10^5. The device has a maximum transconductance of 1.02 μS, and a minimum subthreshold swing of 1 V/decade. The difference in device characteristics between the liquid back-gated measurement and liquid top-gated measurement (i.e. when the reference electrode is in direct contact with the liquid dielectric) is to be expected, due to the relatively inefficient coupling of the SiO_2 layer and the DI-H_2O.

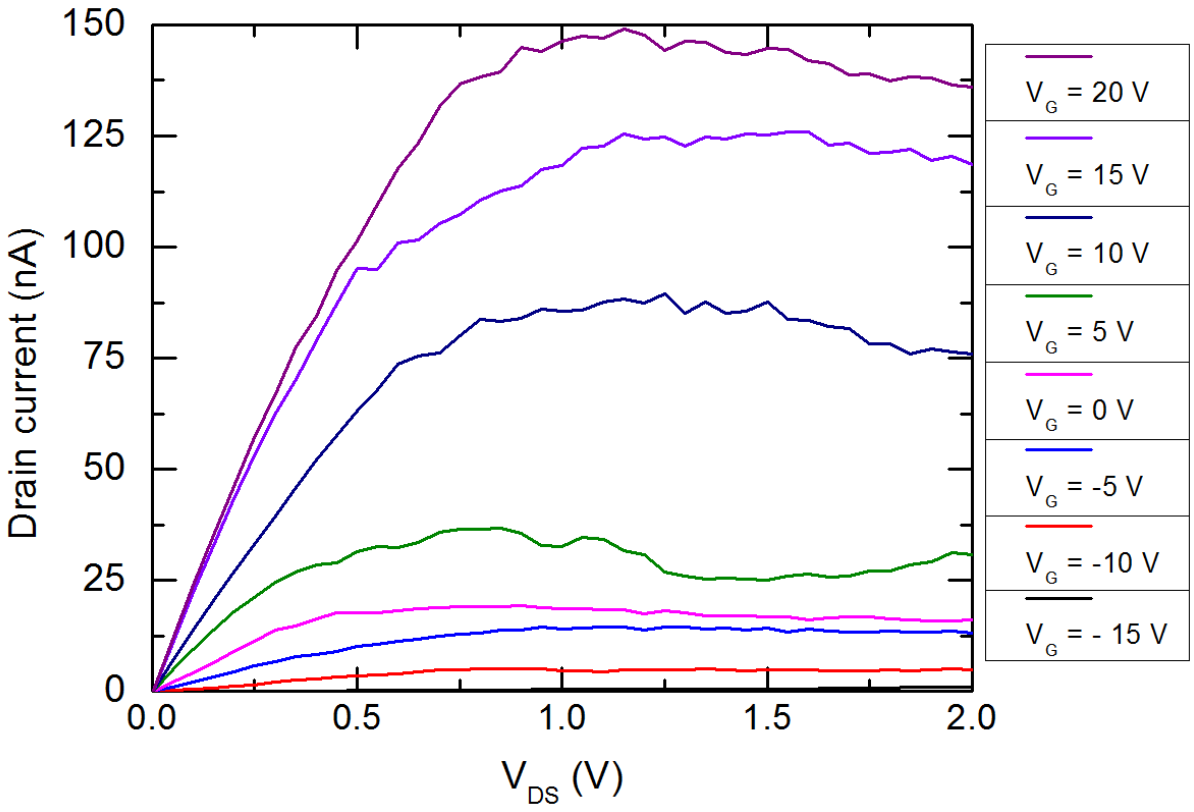

Figure 7.18: Output characteristics of the previously measured wet backgated hierarchical nanowire FET. V_{DS} is swept from 0 to 2 V. The wet backgated voltage ranges from +20 V to -15 V in 5 V steps.

The comparatively high operating voltages of the wet backgated device allow for output characteristic measurements over a wide range of gate voltages. Figure 7.18 shows the output characteristics of the wet backgated device. V_{DS} is swept from 0 to 2 V, while V_G is stepped from V_G = + 20 V to V_G = -15 V in 5 V steps. These measurements clearly show the device depleted at V_G = -15 V. Other measurements at higher gate voltages show well-defined Ohmic and saturation regimes, with the saturation voltage increasing concurrently with V_G.

7.4.4 Context within literature

Although liquid-gated carbon nanotube FETs have attracted significant attention for their potential in biosensing applications [197], there is very little evidence in the literature of liquid-gated ZnO nanowires. There is evidence of at least one liquid-gated ZnO nanowire transistor reported [112], and another device which operates in liquid environments, but not as an FET [198]. Similarly, there are at least two reports of liquid-gated transistors which are based on bulk ZnO [199, 200]. The single report which does use ZnO nanowires as liquid-gated transistors [112] is similar to the work here, in that

the devices are fabricated in pre-defined locations using ZnO seeds. However, the transistors which are fabricated require high-temperature annealing to achieve field dependence, whereas all of the modular hierarchical nanowires measured here show field dependence without the need for an anneal. This suggests that they are also compatible with fabrication on flexible device substrates, which is a great boon for biosensing devices. As such, there is a real opportunity for this work to be furthered in biosensing applications, and a gap in the literature exists which these devices could readily fill. These ideas are extrapolated on in the conclusion of this thesis.

7.5 Conclusion

In conclusion, hierarchical nanowires can be synthesised by modular growth of the primary and secondary nanowires in two separate hydrothermal growths. This significantly generalises the growth process from the PEI-mediated single growth presented in Chapter 6, and allows for control over the individual growth phases. As the secondary growth replaces the PEI-mediated gradual release of Zn^{2+} ions, PEI can be omitted from both the primary and secondary growths if required.

Yields of hierarchical nanowires were optimised by systematically adjusting the preheat of the primary nanowire growth, the inclusion of PEI in the primary growth, and the inclusion of PEI in the secondary growth. Primary growths were carried out using 25 mM of HMT/$Zn(NO_3)_2$, along with 3 mM of PEI (M_W = 2000 g/mol) for the PEI-included growths. The primary growths were either unpreheated, preheated for 20 minutes, or preheated for 60 minutes. The primary growth time was fixed at 6 hours. The secondary hydrothermal growths were carried out at 10% of the precursors of the primary growths, namely 2.5 mM of HMT/$Zn(NO_3)_2$. PEI was added at a concentration of 0.3 mM (M_W = 2000 g/mol) for the secondary growths which included PEI. The secondary growth preheat was fixed at 3 hours, and the growth time was fixed at 19 hours.

These experiments either resulted in no secondary nanowire growth, secondary nanowire growth confined to surface-nucleated debris, or secondary nanowire growth from the primary nanowires (i.e. hierarchical nanowire growth.) The optimum recipes were found to be a 20 or 60 minute preheated primary growth without PEI, followed by a secondary growth without PEI. These both had an equal overall hierarchical nanowire growth yield of 50%. The inclusion of PEI in either the primary or secondary nanowire growth significantly reduced the overall yield of hierarchical nanowires.

Electrical measurements of the twice-grown hierarchical nanowires show that

they are typically field independent when measured using a typical SiO_2/backgate, unlike the PEI-mediated hierarchical nanowires measured in Chapter 6. In contrast, the hierarchical nanowire FETs show field dependence when measured when using de-ionised H_2O as a liquid gate. These measurements can be performed using a gate electrode directly in contact with the liquid, or by using the standard back-gate to couple the DI-H_2O to the SiO_2. Using a gate electrode in direct contact with the DI-H_2O results in faster and easier switching, with subthreshold swings as low as 82 mV/decade, and threshold voltages as low as 0.45 V. In comparison, the hierarchical nanowire FET measured using a liquid gate in conjunction with the back gate electrode has a threshold voltage of 8 V, with a subthreshold swing of 1V/decade.

Chapter 8

Individually contacted ZnO nanowires

8.1 Introduction

In this chapter, large numbers of vertically-grown ZnO nanowires are individually contacted using electron beam lithography to fabricate FETs. The single-nanowire devices are fabricated in batches, and three separate batches are presented here. Each batch consisted of 3 - 4 samples (device chips), with multiple nanowires contacted on each sample. All of the single nanowire devices show non-Ohmic conduction, and are modelled using back-to-back Schottky barriers consistent with metal-semiconductor-metal devices which have not been annealed after metallisation [201]. The Schottky barrier heights of two contacts on a single nanowire are shown to be strongly correlated with one another, as are the ideality factors. It is also shown that these do not depend on the diameter of the nanowire. There is no obvious relationship between the physical characteristics of the ZnO nanowire or its growth conditions with the Schottky barrier heights/ideality factors of the contacts.

Despite the large number of devices fabricated, almost all of the FETs show no field dependence regardless of whether or not the nanowires are annealed, in contrast with the literature [113, 114, 118, 54, 11]. One single FET fabricated using a vertically-grown nanowire responds to gate voltages, with an on-off ratio of 10^4 and a threshold voltage of -7 V, a transconductance of 1.65 nS, and a minimum subthreshold swing of 937 mV/decade. The field-dependent mobility of the FET is approximately 0.106 cm^2 V^{-1} s^{-1}.

Another functioning FET is fabricated using a field-dependent secondary nanowire which is isolated from a hierarchical lateral FET, as described in Chapter 6. Damage to the SiO_2 dielectric of the device substrate sustained during the fabrication process negatively impacts the off current of the FET, which is 3 to 4 orders of magnitude

higher than than a typical lateral device. The contacted nanowire displays field dependence, with a threshold voltage of -6.2 V, an on-off ratio of 10^2, a transconductance of 30.1 nS, and a subthreshold swing of 845 mV/decade. Calculations yield a mobility of 2.964 $cm^2\ V^{-1}\ s^{-1}$.

The chapter concludes with some outstanding questions that the results have raised, which pave the way for future work in this field of research.

8.2 Motivation and background

While the ZnO nanowire field-effect transistors fabricated in Chapters 6 and 7 show consistent field dependence and device operation, the FET device channels are complicated due to the overlapping and intersecting nanowires. These nanowire-nanowire junctions and the interfaces between ZnO seed layers and Ti source/drain electrodes could negatively impact the performance of the FETs. The conduction pathway between source and drain electrodes is shown in red in Figure 8.1, with junctions between thin films, primary nanowires, and secondary nanowires highlighted by red circles. A further issue with the device geometry used in Chapters 6 and 7 is the indeterminate channel length of the FET. Accurately knowing the length of the FET channel is necessary to measure certain device parameters, such as the field dependent mobility [103, 104, 105, 54, 106, 107]. Although the gap between the source/drain electrodes is well defined, the length of the secondary nanowires which bridge the gap can be difficult to determine, as they often bridge the electrodes in very large numbers and at a variety of angles.

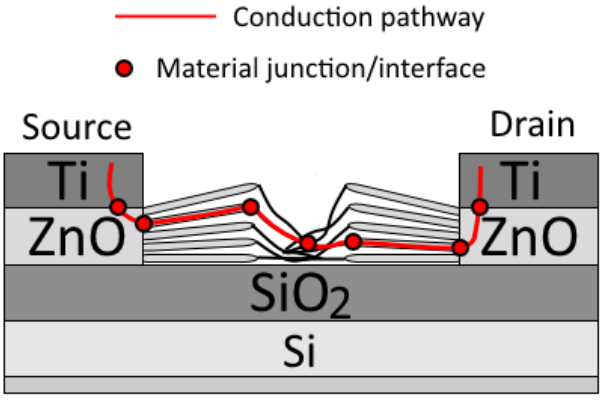

Figure 8.1: A schematic showing the conduction pathway (red) between the source and drain for a lateral hierarchical FET. Junctions in the pathway are highlighted by red circles.

As such, there is a clear motivation to contact individual ZnO nanowires using electron beam lithography (EBL). Restricting the channel to a single ZnO nanowire allows

for accurate measurements of the device channel and nanowire radius, which allows us to calculate device parameters such as mobilities and current densities. Decoupling the channel material from complicated bilayer electrodes also allows for cleaner interpretations of electrical measurements and the characteristics of ZnO nanowires as an electronic material.

8.2.1 Nanowire-metal contacts and Schottky barrier modelling

Unlike the multiple-nanowire FETs fabricated in Chapters 6 and 7, single-nanowire FETs are directly in contact with the source and drain metal electrodes. The metal-semiconductor contact can influence the electrical behaviour of the FET [202], which can be broadly described as Ohmic or non-Ohmic, and can vary significantly from device to device due to impurities and surface states [202]. Although individually contacted nanowires are ostensibly a simple system, the exact cause for non-Ohmic conduction is difficult to conclusively determine. Ohmic contacts to ZnO nanowires are desirable, and have been previously achieved using Ti as a contact metal [203, 204, 205, 206, 207], often in conjunction with a high-temperature anneal. However, ZnO nanowires have also been reported to form non-Ohmic contacts with Ti [208, 209, 210, 211, 212, 213, 214, 215].

Non-Ohmic Ti contact to ZnO nanowires has not been studied in much depth, and most publications which report non-Ohmic conduction do not speculate much on possible causes behind the phenomenon. However, there are isolated reports which investigate the issue. Lin et al. [216] have fabricated both Ohmic and non-Ohmic Ti contacts on individual ZnO nanowires, and relate the quality of the metal to the electrical behaviour. Pure and high-quality Ti allows for Ohmic conduction, while contacts deposited under poorer conditions show non-Ohmic behaviour, which is attributed to nanocrystalline TiO_x granules in either the bulk of the contact or in the vicinity of the nanowire [216]. In addition to problems with the metal contacts, non-Ohmic behaviour has also been attributed to variation in the surface energy of the ZnO nanowire. Furthermore, because the surface energy of the nanowire is affected by the its radius, tapered or inconsistently-shaped nanowires have shown variable electrical behaviour when contacted with Ti. Bercu et al. [217] showed that Ti contacts to large ends of ZnO nanowires were Ohmic, while contacts to narrow ends were Schottky contacts, which was attributed to differences in the nanowire surface energy due to the difference in radius. It is possible that poor-quality metal contacts or the surface states/energy of the ZnO nanowires contributes to the non-Ohmic conduction reported in this chapter, or possibly a combination of the two factors.

The complexity of non-Ohmic contacts therefore makes comprehensive modelling of the ZnO nanowires difficult. One model which has been used successfully in the past to model non-Ohmic conduction treats both metal/semiconductor interfaces as Schottky diodes [218, 219, 220, 221, 222, 223, 224]. When metal comes into contact with a semiconductor, a Schottky barrier typically forms at the interface [202]. As a ZnO nanowire is contacted by metal at both ends, it forms a metal-semiconductor-metal (MSM) system with two Schottky barriers. For *n*-type semiconductors, the Schottky barrier height (SBH) is given as the difference between the conduction band edge of the semiconductor and the Fermi level of the metal, depicted in Figure 8.2. The height of this Schottky barrier can be approximated to a first order by considering the difference in the work function of the metal and the electron affinity of the semiconductor. However, the actuality of the situation is more complicated, and Schottky barrier heights can vary dramatically even when ostensibly using identical metals and semiconductors due to interface states between the materials [202]. Another figure of merit is the ideality factor, which qualitatively describes how rigorously the Schottky barrier adheres to the Shockley diode equation [202].

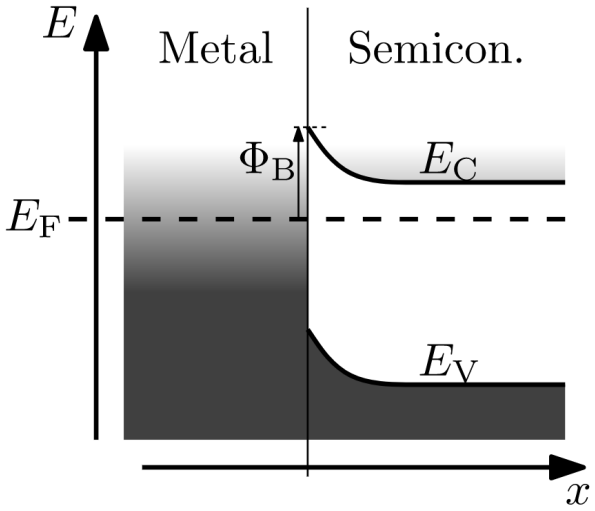

Figure 8.2: A figure showing the Schottky barrier ϕ_B which forms at the metal/semiconductor interface due to the mismatch of the Fermi level of the metal and the conduction band edge of the *n*-type semiconductor. Figure adapted from [225].

While there are several ways of modelling back-to-back Schottky diodes, several of these rely on temperature-dependent measurements. In this chapter, we make use of the current density model first developed by Chiquito et al. [218], and later used/adapted by others [219, 220, 221, 222, 223, 224]. Diode measurements of nanowire devices are taken with no gate voltage applied, and the cross-sectional area of the nanowire is then ascertained using SEM. When a source-drain voltage is applied, one of the Schottky diodes is forward-biased, while the other is reverse-biased. The

current densities of the individual Schottky diodes are considered using a thermionic emission model [218], and the net current density through the nanowire is given as the sum of the current densities through each individual Schottky diode. For modelling purposes, the series resistance of the nanowire is assumed to be negligible, and barrier lowering from mirror images is neglected. Using these assumptions, the current density of the nanowire can then be expressed as [218]:

$$J = \frac{J_1 J_2 \sinh(\frac{qV}{2k_B T})}{(J_1 \exp(\frac{qV}{2n_1 k_B T}) + J_2 \exp(\frac{-qV}{2n_2 k_B T}))} \tag{8.1}$$

where k_B is Boltzmann's constant, q is the elementary charge, V is the drain-source potential, T is the temperature, and n_1 and n_2 are the ideality factors of the first and second Schottky contacts, respectively. J_1 and J_2 are defined as:

$$J_{1,2} = A^{**} T^2 \exp(-\frac{\phi_{1,2}}{k_B T}) \tag{8.2}$$

Where A^{**} is the Richardson constant. In the calculations used throughout this chapter, the temperature is taken to be 300 K, and the Richardson constant is taken to be 32 A cm^{-2} K^{-2} [93].

Current densities were fitted using a custom non-linear curve fit build using OriginLab's Origin 8.5 Fitting Function Builder. The ideality factors and Schottky barrier heights were constrained to be above 0, and fits were achieved using a least squares approach. However, the ideality factor isn't restricted to any particular range. As the ideality factor describes how carriers recombine in thermionic diodes [202], a least-squares approach can in theory produce results which mathematically model the observed results, but do not accurately reflect the Schottky diode. It is important to keep this in mind when considering these results.

8.2.2 Batchwise fabrication of devices

The EBL work was carried out in collaboration with Assoc. Prof. Martin Allen through the MacDiarmid Institute at the University of Canterbury (UC), and Assoc. Prof. Adam Micolich at the University of New South Wales (UNSW). Single nanowire devices were fabricated in batches. The recipes used to grow the ZnO nanowires differed between these batches of devices, as well as EBL techniques, device substrate designs, and the corresponding results. As such, this chapter is separated into sections where each batch is analysed individually. The overall single nanowire yields are considered and the electrical measurements of the devices are presented.

Single nanowires are contacted via EBL on device substrates, which are referred to in this chapter as "samples". Each sample has multiple single-nanowire devices, which are referred to as writefields. The samples are grouped together batch-wise. There are three batches of samples in total which are presented in this chapter. They are:

1. UNSW1 - Batch of samples fabricated at the University of New South Wales
2. UC1 - First batch of samples fabricated at the University of Canterbury
3. UC2 - Second batch of samples fabricated at the University of Canterbury

Samples within each batch are given a number, SN, and individual writefields on each sample are indexed as WFN. The batch number, sample number, and writefield are used to refer to specific single nanowire devices. For example, UC1 - S3 - WF4 refers to the fourth writefield of the third sample from the UC1 batch. The total number of writefields per sample differs between batches, as different device substrate designs were used for each batch. These are detailed in each relevant section, along with the particular ZnO nanowires used.

8.3 UNSW1

8.3.1 Single nanowire device fabrication and yields

UNSW1 consisted of 3 samples in total, referred to as UNSW1 - S1, S2, and S3. All three samples were fabricated using identical nanowires. The contacted nanowires were first hydrothermally synthesised using 25 mM HMT/$Zn(NO_3)_2$ and with 1.5 mM of PEI($\mathrm{M_W} = 2000$ g/mol) on a dedicated growth substrate, as per Chapter 5. The hydrothermal growth solution was preheated at 95°C for 20 minutes, and the growth lasted 19 hours. The vertical nanowires were then transferred to the samples using

the dry tex-wipe method described in Appendix A. All of the contacted nanowires originated from a single nanowire growth substrate, to ensure they were directly comparable. The nanowires were used as-is after transfer, with no annealing step. The UNSW1 samples are summarised in Table 8.1.

Table 8.1: The nanowires and anneals used in the fabrication of the UNSW1 batch of samples

	PEI Concentration (M_W = 2000g/mol)	Growth substrate	Anneal
UNSW1 - S1	1.5 mM	Vertical	None
UNSW1 - S2	1.5 mM	Vertical	None
UNSW1 - S3	1.5 mM	Vertical	None

The device substrates used in all the UNSW1 samples are very similar to those described in Appendix A, although differ slightly. The device substrates have 24 pairs of electrodes, corresponding to 24 write fields in total. The photolithographically defined Ti/Au electrodes are deposited onto an HfO_2(10 nm)/SiO_2(100 nm)/Si substrate, which is used as a bi-layer dielectric and back gate. The thin layer of HfO_2 has a higher dielectric constant than SiO_2, which can improve device characteristics. The EBL system used in the fabrication of UNSW1 is a Raith150-TWO, which slightly differs from the Raith150 at the University of Canterbury, described in Appendix A, however the processes are similar.

Patterned areas of the UNSW1 samples were exposed to 470 μC/cm^2, and were developed in 3:1 IPA:MIBK (2-propanol/methyl isobutyl ketone) for 60 seconds. The samples were cleaved in half before metallisation, with one half of each sample exposed to an O_2 plasma at 50W. This plasma ostensibly descummed the nanowire ends from residual PMMA, which can improve contact and the yield of fabricated devices. The other half of each sample was left untreated. Both halves of each sample were then pumped down in an evaporator and coated with a 85/15 Ti/Al layer via resistive evaporation. After metallisation, both halves of each were lifted off using an overnight acetone bath and agitation with a plastic pipette.

Figure 8.3 shows a collage of SEM images of single nanowires contacted from UNSW1 - S1, S2, and S3. The nanowires which have been broken off from the growth substrate during transfer to the device substrate, which has reduced their lengths considerably. Figure 8.3(a) to (e) show nanowires which have successfully been contacted using EBL, while Figure 8.3(f) shows a contact which is unreliable/broken due to discontinuous metal in the contact. This typically occurs from a combination of

factors, including the EBL process itself and the metallisation/liftoff.

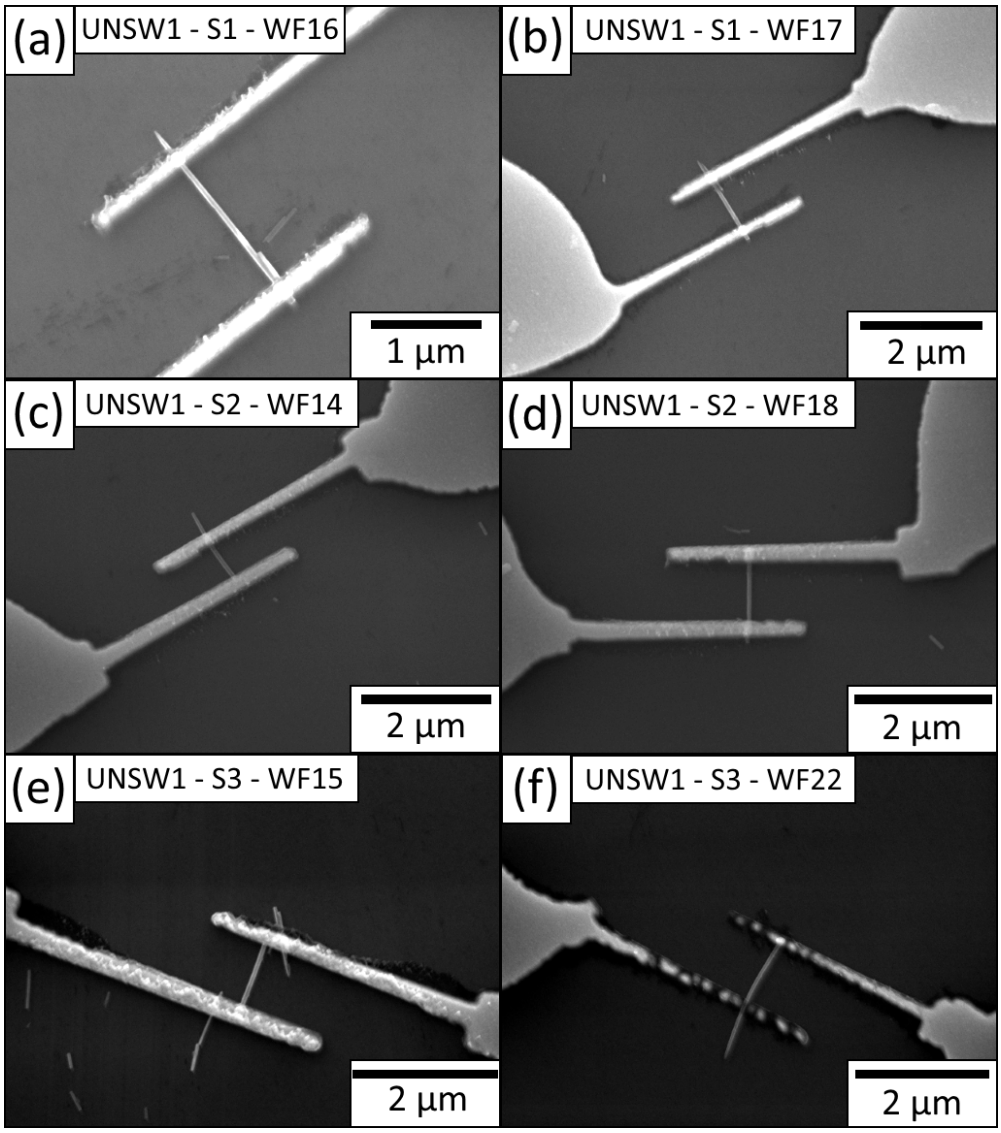

Figure 8.3: SEM images taken of different contacted nanowires from the UNSW1 S1 (a & b), S2 (c & d), and S3 (e & f). Each image is labelled with the specific writefield imaged. The quality of the contacts is good overall, although some suffer from discontinuities in the deposited metal, as in (f).

8.3.2 Electrical measurements

Contacted nanowires were electrically measured to determine whether the nanowires conducted and whether they were field dependent. Significantly, the half samples which were exposed to an O_2 plasma prior to metallisation showed no conduction, and are omitted here. This is consistent with reports in the literature correlating increased nanowire resistivity with exposure to O_2 plasma, which is caused by surface states depleting charge carriers from the nanowire [177].

All of the nanowires contacted on the halves of S1, S2, and S3 which weren't plasma treated showed conduction. However, only one device showed field dependence, which was contacted on UC1 - S1. To contrast the field-dependent device from the field-independent devices, Figure 8.4 shows a collage of diode measurements and transfer measurements from various writefields of UNSW1 - S1 which weren't exposed to O_2 plasma.

The SBH/ideality factor of the contacts for each writefield are included on the diode measurements. The Schottky barriers can vary within individual writefields, with each individual contact on a single nanowire having a different barrier height and ideality factor. This can lead to asymmetric diode behaviour such as writefields 16 and 17, shown in Figure 8.4(a) and (e) respectively. Other devices show less variation between the two contacts and symmetry about $V_{DS} = 0$ V, as in writefield 19, shown in Figure 8.4(c). In addition to variations between the two contacts on an individual nanowire, the Schottky barrier height and ideality factors of the contacts can also vary strongly between different nanowires/writefields.

Figure 8.5 shows the current density of writefields 16 and 17 fitted using the back-to-back Schottky barrier model. This model accurately reproduces the electrical behaviour of the devices, and both fits have low residual errors.

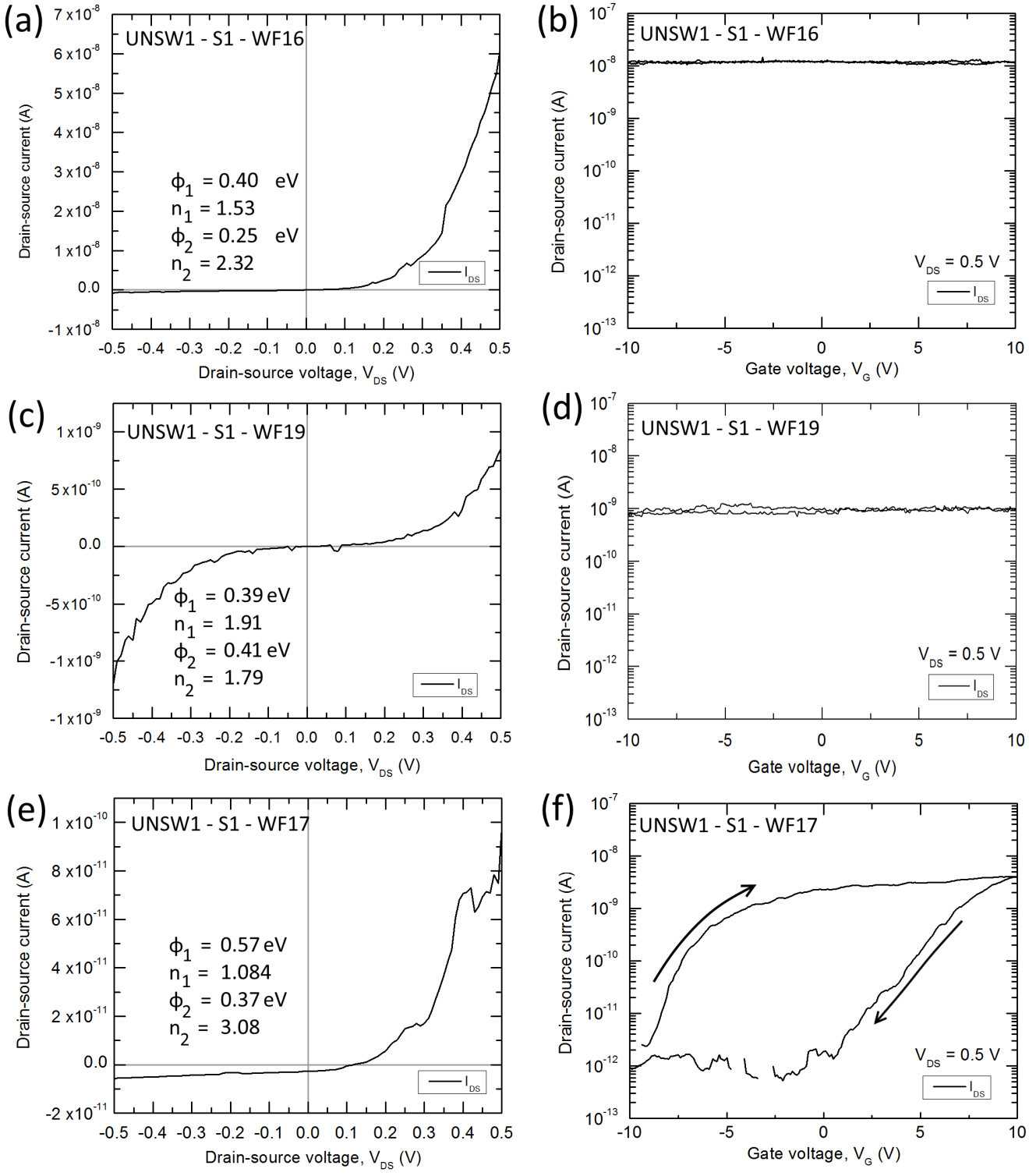

Figure 8.4: Diode and transfer measurements of three different writefields from UNSW1 S1. Diode measurements of all three writefields (a, c, and e) show that the nanowires clearly conduct. Writefields 16 and 17 (a and e, respectively) are asymmetric, which is reflected in different SBH/ideality factors for each contact. Conversely, writefield 19 (c) is symmetric, and the SBH of the two contacts differ by ≈2%. Transfer characteristics of the writefields are shown in (b, d, and f). Writefields 16 and 19 show no field dependence, while writefield 17 clearly responds to applied gate voltages.

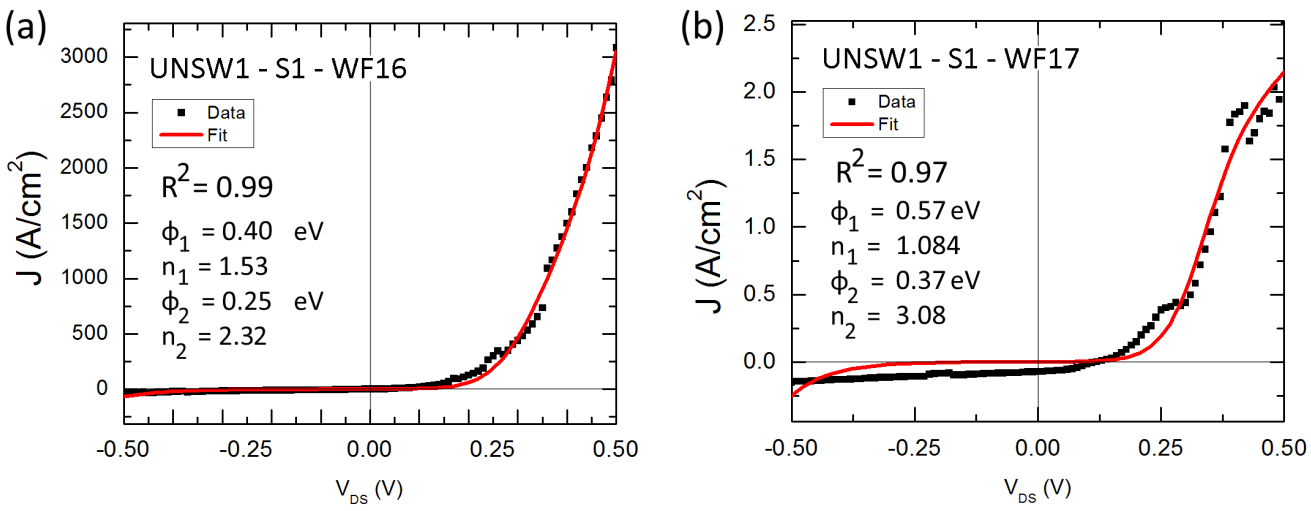

Figure 8.5: The current densities of (a) WF16 and (b) WF17 fitted using the back-to-back Schottky model (red).

Although the nanowires show conduction, only the nanowire contacted at writefield 17 shows field dependence. The transfer characteristics of writefields 16 and 19, shown in Figure 8.4(b) and (d), are more representative of the nanowires contacted on the UNSW1 samples. The drain-source currents shows no variation between V_G = -10 to 10 V. In contrast to the field-independent nanowires, WF17 of S1 shows marked field dependence. The transfer characteristics of this device are shown in Figure 8.4(f). The nanowire operates with an on-off ratio of 10^4 and a threshold voltage of -7 V. The FET has a maximum transconductance of 1.65 nS, and a minimum subthreshold swing of 937 mV/decade.

As the channel length of this device is well-defined, we can estimate the field-dependent mobility of the FET. The mobility of the device is typically defined as [103, 104, 105, 54, 106, 107]:

$$\mu = g_m \times \frac{L^2}{V_{DS} \times C_{NW}} \tag{8.3}$$

where μ is the mobility of the device, g_m is the transconductance of the device, L is the length of the nanowire, V_D is the drain-source voltage, and C_{NW} is the capacitance of the nanowire. The capacitance of a nanowire is typically approximated as the cylinder-on-infinite-plane model, given as [103, 104, 105, 54, 106, 107]:

$$C_{NW} \approx \frac{2\pi\varepsilon_0\varepsilon_r L}{\cosh^{-1}\left(\frac{r+d_{ox}}{r}\right)} \tag{8.4}$$

where ε_0 is the permittivity of free space, ε_r is the dielectric constant, r is the radius of the nanowire, and d_{ox} is the thickness of the dielectric layer. It is worth noting

that the thin HfO_2 dielectric layer deposited on top of the SiO_2 layer is fundamentally different from the infinite-plane model, which limits the accuracy of the capacitance calculation [226]. For the purposes of this calculation, the HfO_2(10nm)/SiO_2(100nm) dielectric bilayer is treated as a homogeneous 110 nm thick dielectric with an effective dielectric constant of 4.97. This is arrived at by treating the dielectric as a bilayer with an effective dielectric constant of:

$$\varepsilon_{eff} = \frac{\varepsilon_{\mathrm{SiO_2}}\varepsilon_{\mathrm{HfO_2}}}{\frac{1}{1.1}\varepsilon_{\mathrm{SiO_2}} + \frac{0.1}{1.1}\varepsilon_{\mathrm{HfO_2}}} \tag{8.5}$$

The individual relative dielectric constants are taken to be $\varepsilon_{\mathrm{SiO_2}}$ = 3.9 and $\varepsilon_{\mathrm{HfO_2}}$ = 25, respectively [227].

Taking the nanowire radius to be 38 nm, the nanowire length to be 1.1 μm, ε_0 to be $\approx 8.854 \times 10^{-12}$ F/m, the nanowire capacitance is calculated to be $\mathrm{C_{NW}}$ = 3.76 $\times$ 10^{-16} F. Using the transconductance of the device (1.65 nS), the capacitance of the nanowire, and V_{DS} = 0.5 V, the mobility of the FET is calculated to be 0.11 cm^2 V^{-1} s^{-1}. This mobility is relatively low compared to other ZnO nanowire FETs, which are typically on the order of 0.1 - 1000 cm^2 V^{-1} s^{-1} (a table reviewing the device characteristics of published hydrothermal ZnO nanowire FETs can be found in 3.1 in Chapter 3.)

It isn't necessarily surprising that the majority of measured devices from UNSW1 do not respond to applied fields, as the contacted nanowires are unannealed and are too heavily doped to show field dependence prior to high-temperature annealing [113, 114, 118, 54, 11] (this phenomenon in general is reviewed in detail in the overview of ZnO nanowire FETs in Chapter 3.) However, it is unusual that WF17 of S1 specifically responds to applied gate voltages, while other contacted nanowires on the same sample show no response. It is not clear what exactly causes this particular nanowire to exhibit field dependence and clear switching. All of the the nanowires on the device substrate have been transferred from the same growth substrate, and are all metallised during the same Ti/Al deposition, which should minimise the difference between nanowires and contacts.

However, as we have seen in Figure 8.4, ostensibly similar nanowires contacted on the same chip can have different Schottky barrier heights and ideality factors. Furthermore, variations in the field dependence may be due to differences in the nanowires themselves, or in the contacts, or in a complex interplay between the two. Possible relationships between the nanowire properties, the contact properties, and the Schottky barrier heights/ideality factors are explored in detail in Section 8.6.

8.4 UC1

8.4.1 Single nanowire device fabrication and yields

UC1 consists of three samples in total, referred to as UC1 - S1, S2, and S3. UC1 - S1 and S2 were fabricated using nanowires grown with 25 mM HMT/$Zn(NO_3)_2$ and 8 mM of PEI(M_W = 800 g/mol). These nanowires originated from a single dedicated growth substrate. The nanowire growth solution was preheated for 1 hour before the growth substrate was introduced, and the hydrothermal growth lasted 19 hours. After the hydrothermal growth was complete, the dedicated growth substrate was annealed at 650°C for 1.5 hours in a tube furnace. The annealed nanowires were then transferred to the UC1 - S1 and S2 samples using the tex-wipe method described in Appendix A.

UC1 - S3 was fabricated using secondary nanowires which were isolated from hierarchical nanowires grown via a PEI-mediated one-pot hydrothermal growth, described in Chapter 6. These hierarchical nanowires were grown on a lateral substrate using 8 mM of PEI(M_W = 800 g/mol) and 25 mM of HMT/$Zn(NO_3)_2$. These secondary nanowires were specifically chosen as they had shown good field dependence without requiring high-temperature annealing, as evidenced by the devices measured in Chapter 6. The secondary nanowires were isolated from the lateral growth substrates using the same tex-wipe method as used for the vertical growth substrates, described in Appendix A. The secondary nanowires were used as-is, without any annealing.

All three of the UC1 samples used identical device substrates with 6 pairs of electrodes, corresponding to 6 writefields per sample. The device substrates used 100 nm of SiO_2 as the backgate dielectric. Electron beam lithography was carried out using the Raith150 at the University of Canterbury, which is described in detail in Appendix A. The samples were exposed using a dosage of 100 $\mu C/cm^2$, and developed for 60 seconds in 3:1 IPA:MIBK. After development, the samples were rinsed in IPA, and were not plasma treated. All three of the samples were metallised using Ti/Au (20/90 nm) deposited via egun deposition and resistive evaporation, respectively. After metallisation, S1 and S2 were lifted off in acetone for 3 hours and 1 hour, respectively. S3 was lifted off in NMP (*N*-Methyl-2-pyrrolidone) at 85°C for 1 hour. The UC1 samples are summarised in Table 8.2

Table 8.2: Samples fabricated from the UC1 batch of samples. UC1 S1 and S2 are fabricated using vertically grown ZnO nanowires, while S3 is fabricated using secondary nanowires which have been isolated and transferred from their lateral hierarchical substrate.

	PEI Concentration (M_W = 800g/mol)	Growth substrate	Anneal
UC1 - S1	8 mM	Vertical	600°C on growth substrate
UC1 - S2	6 mM	Vertical	600°C on growth substrate
UC1 - S3	8 mM	Lateral (hierarchical)	None

Figure 8.6 shows a collage of SEM images of contacted single nanowires from UC1 - S1, S2, and S3. Some of the nanowires which were contacted on S1 have been partially or completely etched away during the liftoff process, as in Figure 8.6(c) and Figure 8.6(d). The nanowires which have been totally etched away were clearly present on the device substrate when the metal contacts were initially deposited, as the impression of the nanowires can be seen on the surface of the metal (as in Figure 8.6(c)). Other nanowires on S1 show partial etching or damage to the nanowire surface, as in Figure 8.6(a). In addition to the etching that can occur during the liftoff, all of the nanowires contacted on UC1 - S1 and S2 also show a significant degradation over time, completely disappearing from the substrate after 8 months. The nanowire etching/degradation is discussed in detail in Section 8.7.

In comparison to UC1 - S1, nanowires contacted on UC1 - S2 do not show any surface etching, as shown in Figure 8.6(e) and (f). This is due to a reduction in the liftoff time, from 3 hours in acetone to 1 hour in acetone. Although acetone has been reported to partially etch the surface of ZnO nanowires [228, 229], it is surprising to see complete etching/dissolution of the nanowires over a comparatively short timescale. Several more samples were fabricated and lifted off in acetone over long periods of time (3 to 14 hours) to confirm the phenomenon, which also showed complete etching of the nanowires (not shown here.)

Finally, secondary nanowires contacted on UC1 - S3 showed no obvious surface etching. This may be due to either a short liftoff time (1 hour) or the use of hot NMP as a liftoff solvent, or a combination of these two factors. The overall device yield is also improved by the comparative length of the secondary nanowires, as the tolerances of errors in the contact design/alignment are significantly higher than samples fabricated using shorter nanowires. As such, all of the writefields successfully contacted the nanowires, with a contact yield of 100%.

While all of the nanowires on S3 were successfully contacted, unfortunately the total yield of viable FETs on UC1 - S3 is greatly compromised by leaks through the SiO_2 dielectric, and only one FET can be successfully measured. These leaks are most likely to be small scratches or hairline fissures which have been introduced when the device substrate is cleaved from a wafer. These leaks cannot be seen by SEM, and are only apparent when the nanowires are electrically measured.

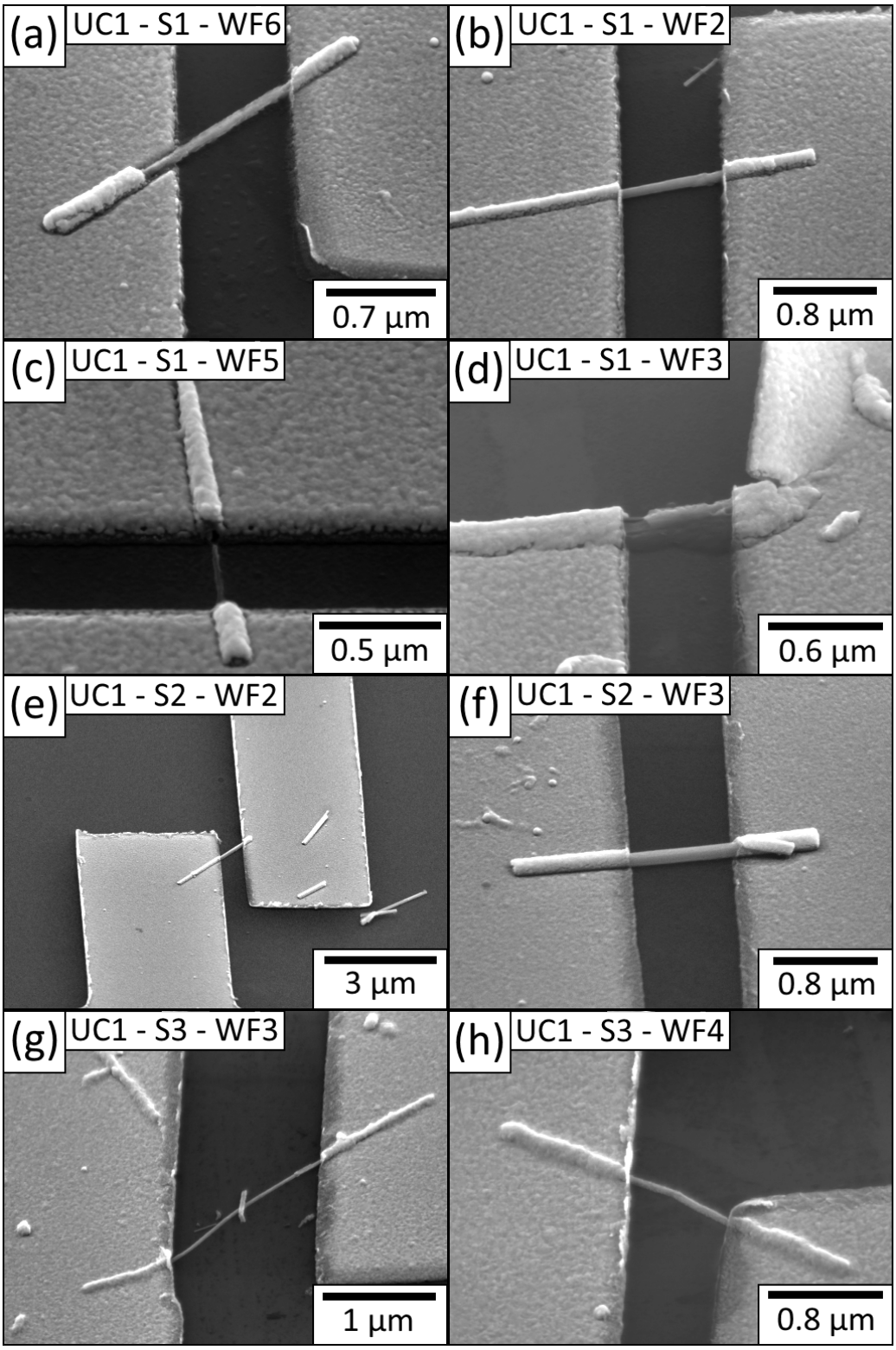

Figure 8.6: SEM images of UC1 - S1, S2, and S3. UC1 - S1 suffers from partial etching of the ZnO nanowires, shown in (a) and (b), and complete etching, as in (c) and (d). The nanowires contacted on UC1 - S2, shown in (e) and (f), are unetched due to the reduced liftoff time. Finally, (g) and (h) show contacted secondary nanowires from UC1 - S3.

8.4.2 Electrical measurements

Electrical measurements of UC1 - S1 and UC1 - S2 are shown in Figure 8.7. These measurements are taken in dark (ambient) conditions, shown in black (squares), and when exposed to UV light at 405 nm, shown in red (triangles). Exposing the nanowires to UV light photoexcites charge carriers through electron-hole pairs [96, 230, 185], which affects the electrical characteristics of the device and the SBH/ideality factor of the contacts. Diode measurements of UC1 - S1 and UC1 - S2 are shown in Figure 8.7(a - e). The devices show back-to-back Schottky barrier behaviour under both conditions. Different SBH/ideality factors between two contacts on a single nanowire lead to asymmetric measurements about V_{DS} = 0 V, as in Figure 8.7(b). These asymmetric devices represent ≈85% of the contacted nanowires from UC1 - S1 and S2.

The remaining contacted nanowires show more symmetric behaviour, such as S2- WF4 (shown Figure 8.7(e)). Although the contacted nanowires on UC1 - S1 and S2 show conduction, none of the writefields show field dependence. An example is given in Figure 8.7(f), representative of all the contacted nanowires. It is clear that the device shows no response to the applied field due to the constant I_{DS} value (≈1.5×10^{-11} A).

All of the devices show an increase in current when measured under UV illumination. The increase in current can be symmetrical, with increased drain-source current in both positive and negative V_{DS} values (as in Figure 8.7(e)), or asymmetrical, with increased current in only one direction (as in Figure 8.7(b)). These differences can be modelled as changes to the SBH/ideality factor to one or both of the contacts under UV illumination, which are shown in Figure 8.7(a - e).

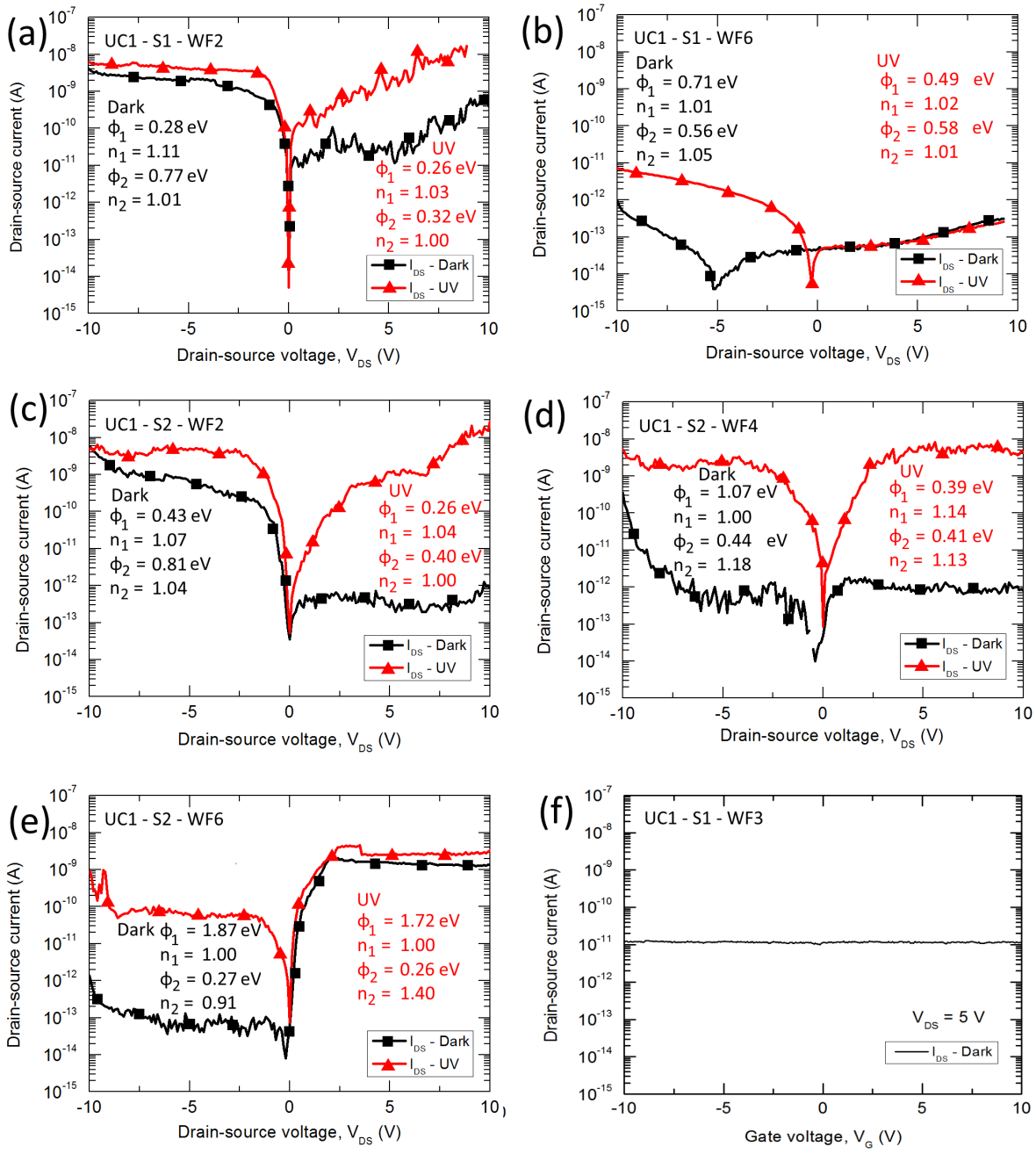

Figure 8.7: Electrical measurements of UC1 S1 (a,b) and S2 (c - d) under ambient (black, squares) and UV-illuminated (red, triangles) conditions. The fitted SBH/ideality factor of each contact is shown in the diode measurements of each device. All of the nanowires show conduction, although none show field dependence - S1 - WF3 is included in (f) as an example.

The current densities of some devices from UC1 - S1 are shown in Figure 8.8. Similar to the fits shown previously in Figure 8.5, the model accurately reproduces the current densities for diodes measured in both the dark and under UV illumination. The electrical behaviour of symmetric diodes is reproduced particularly well, although the model shows some inaccuracy with increasing asymmetry, as in Figure 8.8(d). However, the overall residual error remains small, with an R^2 value of 0.94.

There is one report on the lowering of ZnO nanowire Schottky barriers with UV light [231], which is mediated by the desorption of oxygen species on the nanowire surface through photoexcited holes. This reduces the surface depletion of the nanowire, which in turn lowers the SBH. This is identical to the mechanism which induces persistent photoconductivity in ZnO nanowires, described in detail in Chapter 6.

In this report, the UV light is at 365 nm, which falls within the bandgap of ZnO ($\approx$368 nm, or 3.37 eV [10]). In the experiments presented here, the wavelength of light used is 405 nm, which is less energetic than the ZnO band gap. Despite this discrepancy, it is likely that the same oxygen desorption mechanism is taking place in the UV-illuminated measurements of UC1 - S1 and S2. As we have shown in Chapter 6, charge carriers and persistent photoconductivity can be induced in ZnO nanowires by using 405-nm UV light, with energy less than the bandgap of ZnO. There are also reports in the literature which show charge carrier photoexcitation when using UV light which falls below the bandgap [186, 187].

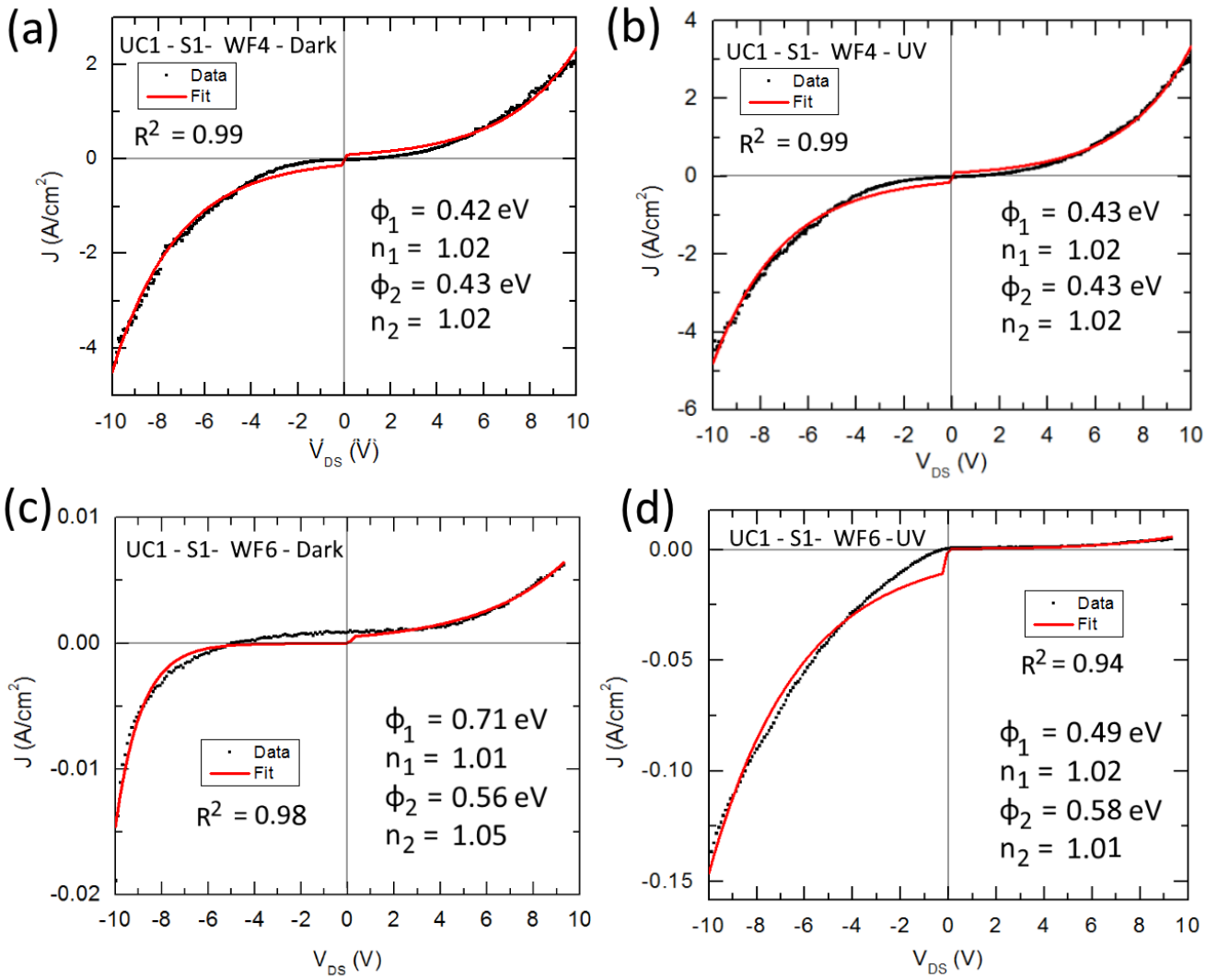

Figure 8.8: The current densities of UC1 writefields measured in dark and UV conditions, fitted using the back-to-back Schottky model (red).

In contrast to the vertical nanowires used in UC1 - S1 and S2, UC1 - S3 was fabricated using secondary nanowires which were known to be field dependent, as they were isolated from a lateral field-dependent FET fabricated in Chapter 6. However, 5 out of the 6 writefields were unusable due to leakage currents on the order of 10^{-6} A between V_G = -10 V and 10 V. These high leakage currents are caused by damage to the SiO_2 dielectric layer on the sample, introducing unintentional conduction pathways between the source/drain electrodes and the gate electrode. This damage was likely caused when the device substrate was cleaved from its larger wafer, which was inadequately protected.

Despite this damage, the nanowire contacted at writefield 3 was measurable as the leakage currents were considerably smaller. An SEM image of this nanowire is shown in Figure 8.6(g). Figure 8.9 shows the electrical measurements of UC1 - S3 - WF3. The device is measured as a diode in Figure 8.9(a) under dark and UV-illuminated conditions. The measurement is asymmetric about V_{DS} = 0 V under both dark and UV conditions due to the difference in Schottky barrier heights and ideality factors. Figure 8.9(b) shows the drain-source current (squares) of the transfer characteristics of the device, which is driven at V_{DS} = 3 V. Although the nanowire shows field dependence, the off-current of the device is relatively high (10^{-8} A), which is due to the leakage current of the device. A typical leakage current from a back-gated lateral FET fabricated in Chapter 6 is shown in Figure 8.9(c). In comparison, Figure 8.9(d) shows the leakage current of UC1 - S3 - WF3 (triangles.) The leakage current for UC1 - S3 - WF3 is $\approx$3 to 4 orders of magnitude higher than the leakage current of the lateral FET due to the damaged SiO_2 dielectric.

The FET at UC1 - S3 - WF3 operates at a threshold voltage of -6.2 V, with an on-off ratio of 10^2. The maximum transconductance is 30.1 nS, and the minimum subthreshold swing is 845 mV/decade. Taking the length of the nanowire to be 1.56 μm and the radius of the nanowire to be 17 nm, the capacitance of the nanowire is calculated to be 8.24×10^{-17} F, using the methods described in Section 8.3.2. Using the transconductance of the device along with the capacitance and length of the nanowire yields a mobility of 2.96 $cm^2\ V^{-1}\ s^{-1}$. This mobility is low yet comparable to other ZnO nanowire FETs which use hydrothermal nanowires, which are typically between 1 - 1000 $cm^2\ V^{-1}\ s^{-1}$ (a summary of different device characteristics in the literature can be found in Table 3.1 in Chapter 3.)

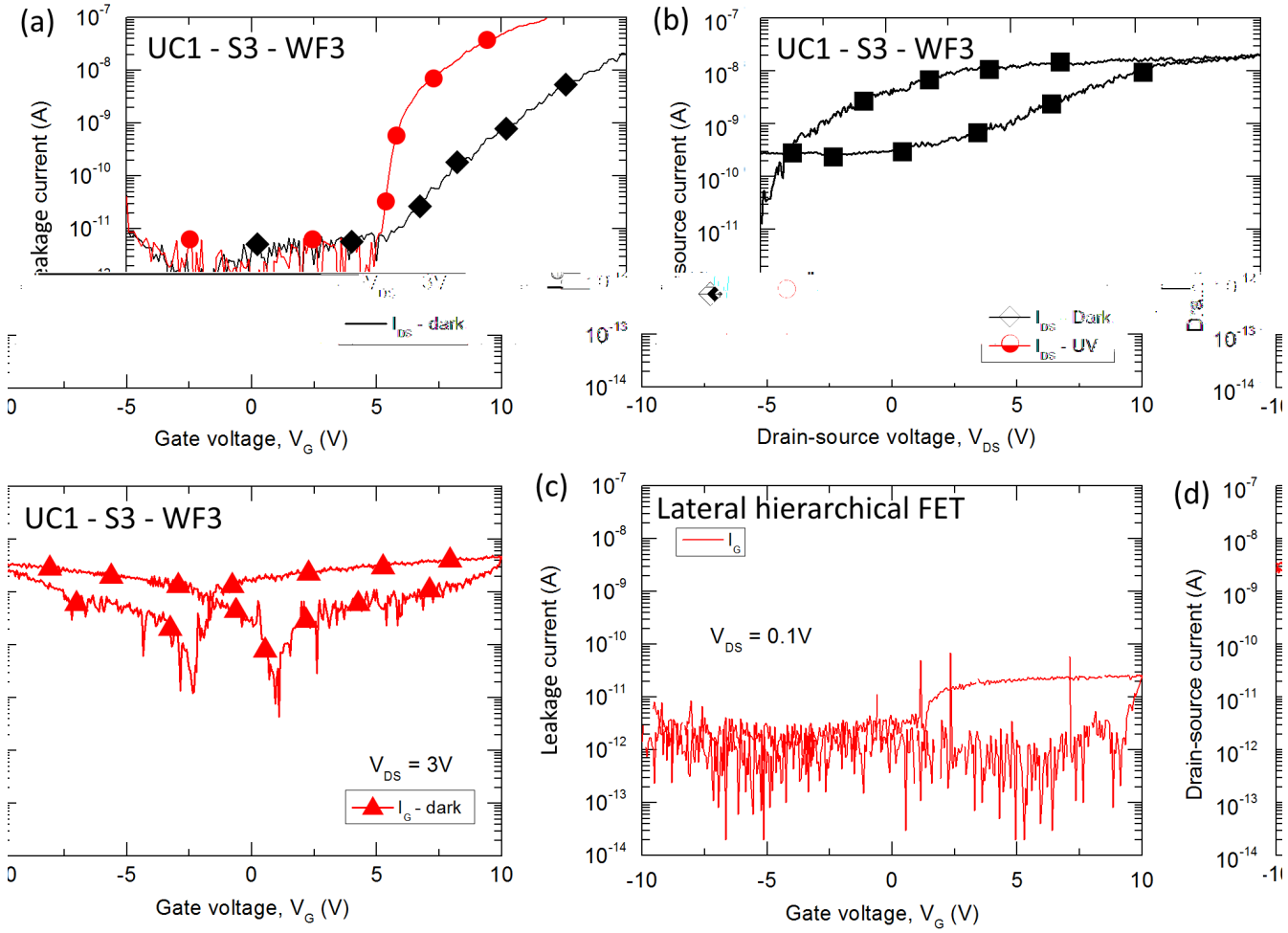

Figure 8.9: Electrical measurements of UC1 - S3 - WF3. (a) Diode measurements in dark (black, diamonds) and UV (red, circles) show an asymmetric device. (b) Drain-source current (I_{DS}) (black, squares) from the transfer measurement of the device. (c) The leakage of a typical lateral FET, where the secondary nanowire used in UC1 - S3 - WF3 is sourced from. (d) The leakage current (I_G) (red, triangles) from the transfer characteristics of UC1 - S3 - WF3.

8.5 UC2

8.5.1 Single nanowire device fabrication and yields

UC2 consists of 4 samples in total, referred to as UC2 - S1, S2, S3, and S4. These samples were fabricated using annealed and unannealed nanowires hydrothermally grown with 6 mM and 8 mM of PEI(M_W = 800 g/mol) and 25 mM HMT/$Zn(NO_3)_2$. Each nanowire growth solution was preheated for one hour at 95°C before the growth substrates were introduced. Each hydrothermal growth lasted 19 hours.

These growth recipes were chosen as nanowires grown with 8 and 6 mM of PEI(M_W = 800 g/mol) show a wide distribution of diameters below 100 nm (these results are summarised in Figure 5.14 in Chapter 5.) There was strong motivation to investigate the effects of the nanowire diameter on the nanowire field dependence, as the persistent photoconductivity measurements in Chapter 6 suggested that depleting surface states and small diameters may be responsible for field dependence. It was hoped that we could contact field-dependent nanowires which were grown vertically, summarise these results, and then contact isolated secondary nanowires *en masse*.

The device substrates used in UC2 are those described in Appendix A. Specifically, each device substrate is photolithographically patterned with 15 pairs of electrodes, corresponding to 15 writefields. The substrate itself is SiO_2 (100 nm)/Si, with a Cr/Au backgate. Samples from UC2 use a mix of unannealed and annealed nanowires. The nanowires were annealed by transferring them from the growth substrate to the device substrate as per Appendix A, and then annealing the device substrate at 450°C for 1 hour. These nanowires were consequently annealed on the device substrates rather than the growth substrates, as in the UC1 samples. All of the nanowires grown using 6 mM of PEI(M_W = 800 g/mol) were isolated from a single growth substrate. The specific nanowires used in each sample from UC2 are summarised in Table 8.3.

Table 8.3: The nanowires used in the fabrication of UC2, and their corresponding annealing treatments.

	PEI Concentration (M_W = 800g/mol)	Growth substrate	Anneal
UC2 - S1	8 mM	Vertical	None
UC2 - S2	6 mM	Vertical	450°C on growth substrate
UC2 - S3	6 mM	Vertical	None
UC2 - S4	6 mM	Vertical	450°C on growth substrate

Electron beam lithography was performed using the Raith150 at the University of Canterbury, as described in Appendix A. Electron beam dosages were kept at 100 μC/cm^2, and substrates were developed for 60 seconds in 3:1 IPA:MIBK. After development, the device substrates were exposed to an argon plasma at 50 W for 30 seconds prior to metallisation. Argon plasmas have been reported to increase the conductivity of ZnO nanowires [232, 233, 113, 118], which can improve the quality of the nanowire/contact interface. Ti/Au (20/80 nm) contacts were deposited using egun and resistive evaporation respectively, after which the substrates were lifted off in acetone over 40 minutes. This short liftoff was intentionally chosen to avoid nanowire etching as we had observed in the UC1 samples.

Figure 8.10 shows a collection of SEM images of S1 and S3. All of the nanowires appear intact and unetched, which is attributed to the short liftoff time in acetone. As was the case with samples from UNSW1 and UC1, the nanowires have snapped and partially broken during transfer from the growth substrate to the device substrate. This has significantly reduced their length, which reduces the tolerance of misalignment during the EBL process. This can lead to some nanowires being missed due to EBL misalignment. Despite this, the samples have good overall yields of contacted nanowires, with yields ranging from 75% to 100%. Furthermore, as each sample has 15 writefields, many separate nanowires can be contacted on each chip.

Although the number of successfully contacted nanowires is relatively high, the nanowires suffer material degradation over time and completely dissolve over the course of at least 8 months, as is the case for the UC1 samples. This gradual degradation occurs despite the fact that the nanowires appear initially unetched due to the short liftoff in acetone. The material degradation is discussed in detail in Section 8.7.

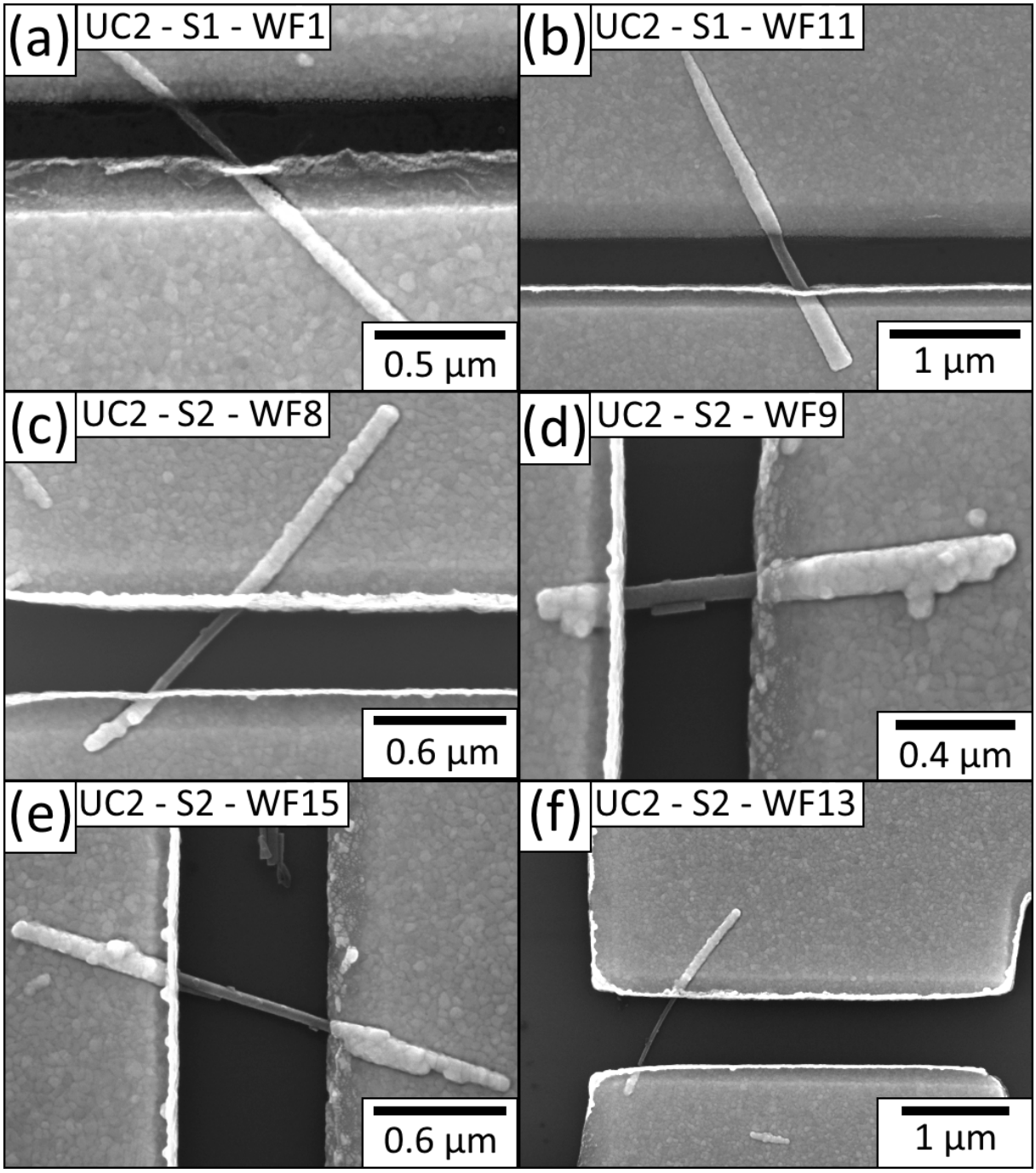

Figure 8.10: SEM measurements of UC2 - S1 and S2, which are representative of the UC2 batch of samples overall. None of the nanowires show any signs of etching after liftoff, as they are kept in acetone for only 40 minutes.

8.5.2 Electrical measurements

Electrical measurements of UC2 - S2 and S3 are shown in Figure 8.11. UC2 - S2 and S3 use nanowires which have been synthesised using the same growth conditions, but are annealed and unannealed, respectively. These measurements are taken immediately after the samples have been lifted off, under ambient conditions. All of the nanowires show back-to-back Schottky contact behaviour. Similar to the UNSW1 and UC1 samples, some of the nanowires are symmetric about V_{DS} = 0 V, such as Figure 8.11(a), while others show extreme asymmetry, such as Figure 8.11(c), depending on the SBH/ideality factor of each contact.

The unannealed nanowires contacted on UC - S3 show higher currents than the annealed nanowires contacted on UC - S2. The highest currents of the unannealed nanowires are on the order of 5×10^{-6} A, shown in Figure 8.11(e), even when the drain-source voltage is kept below 1 V. In comparison, the drain-source currents for annealed nanowires are typically on the order of 5×10^{-8} A, as in Figure 8.11(a - c).
Figure 8.12 shows the current densities of some UC2 devices which have been fitted using the back-to-back Schottky model described in Section 8.2.1. The model accurately fits strongly asymmetric devices, such as UC2 - S2 - WF11 (shown in Figure 8.12(b)). However, other devices show some deviation from their respective fits, such as S3 - WF12 (Figure 8.12(b)). This highlights some of the limitations of the model, which may be related to the assumptions made, such as a negligible nanowire resistance.

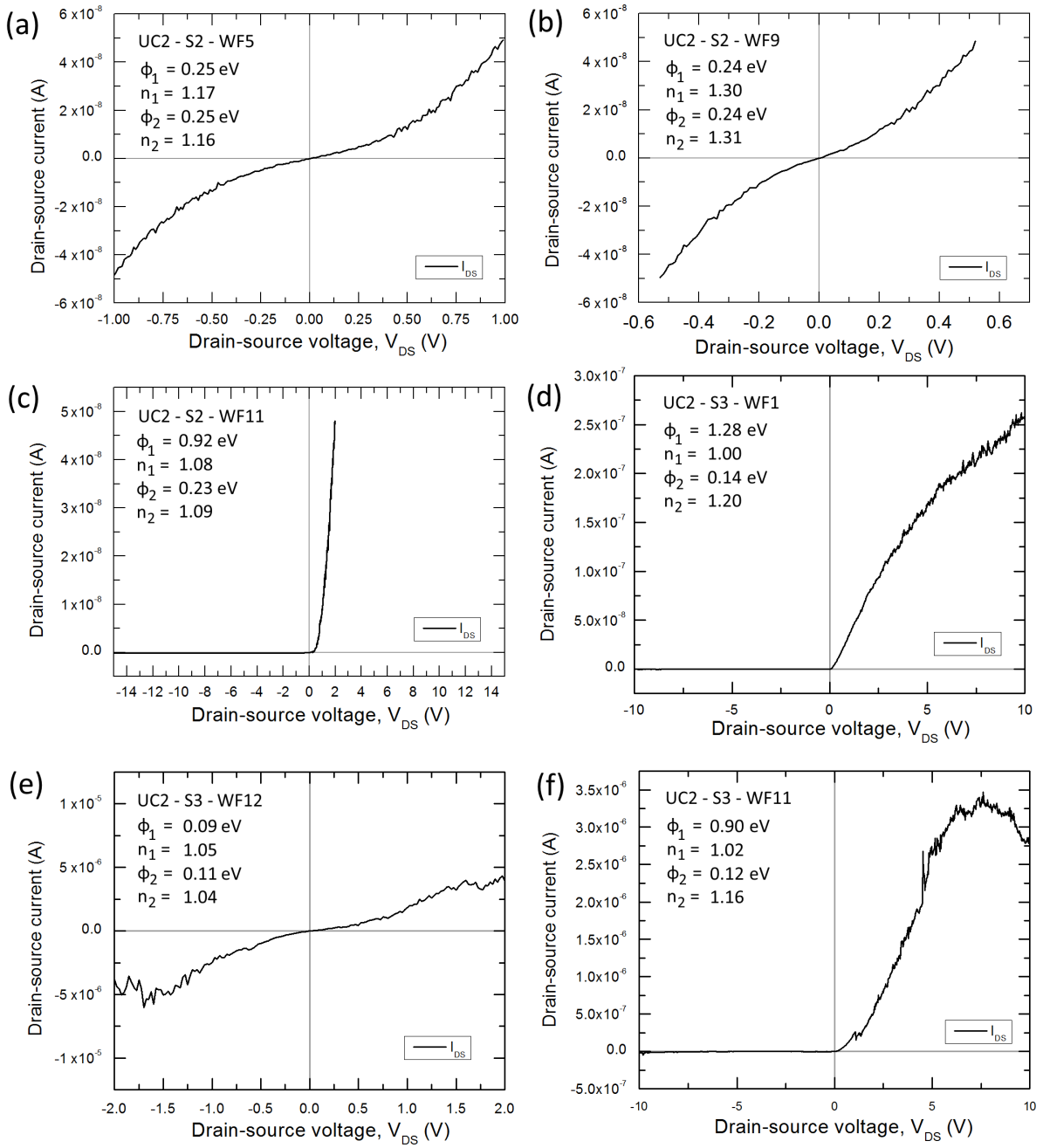

Figure 8.11: Diode measurements of UC2 - S2 (a - c) and S3, (d - f) taken immediately after liftoff, under ambient conditions. Contacted nanowires on UC2 - S2 and S3 can show symmetrical IV characteristics, (a) and (e), or asymmetric characteristics, (c) and (d). The different SBH/ideality factors of each contact are displayed on the graph. The annealed nanowires shown in (a - c) have lower currents than the unannealed nanowires, shown (d - f).

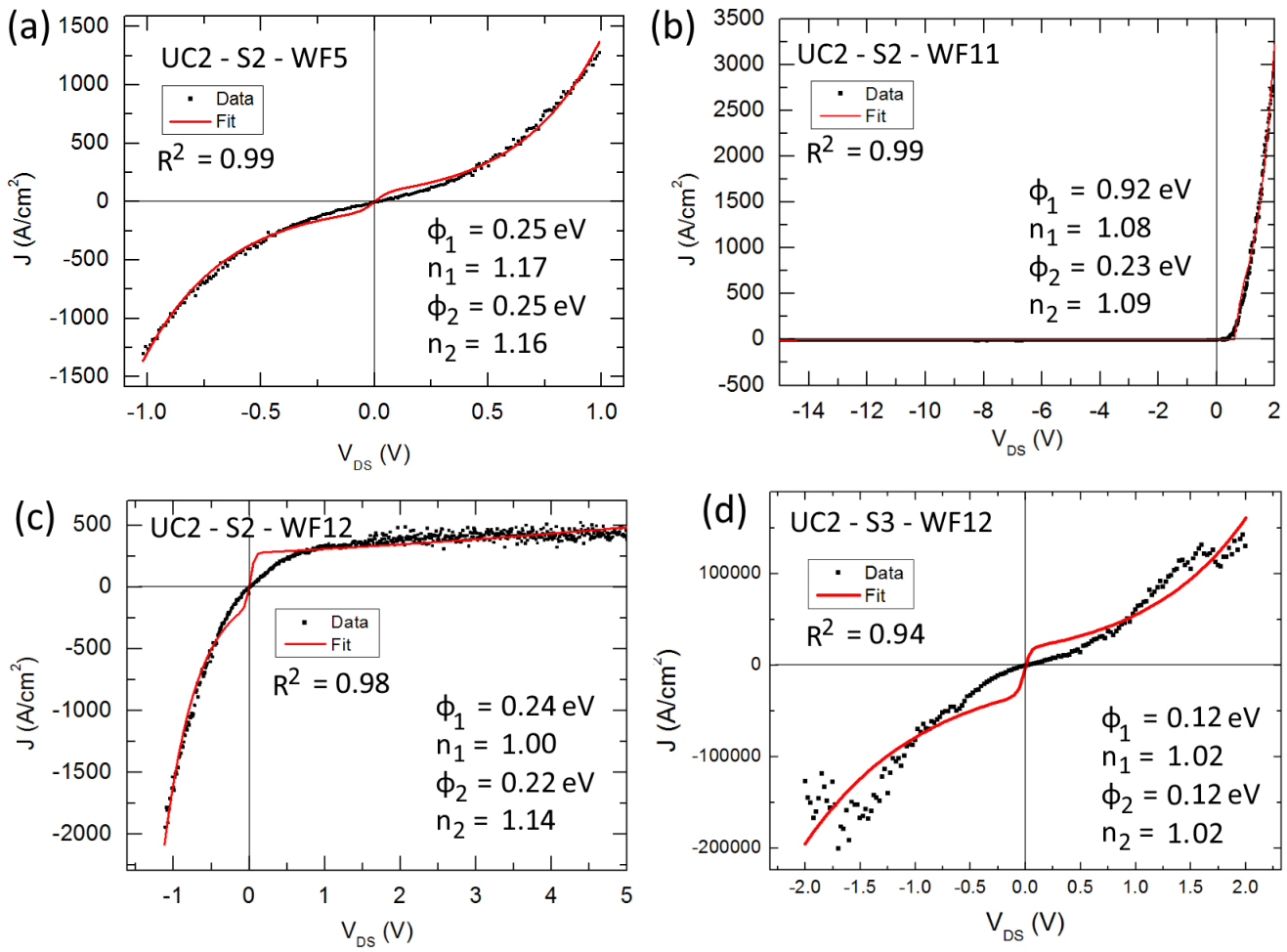

Figure 8.12: The current densities of some UC2 writefields fitted using the back-to-back Schottky model (red).

Although the nanowires show conduction immediately after liftoff, the devices are unresponsive to gate voltages and show minimum field dependence. Transfer characteristics of an annealed nanowire (UC2 - S2 - WF5) are shown in Figure 8.13. The nanowire is driven at a V_{DS} of 0.1 V. The gate voltage is lowered from V_G = 0 to V_G = -20 V in an attempt to deplete the nanowire. Although the nanowire has been annealed, the drain-source current is only reduced by an order of magnitude at best, with no well-defined subthreshold regime.

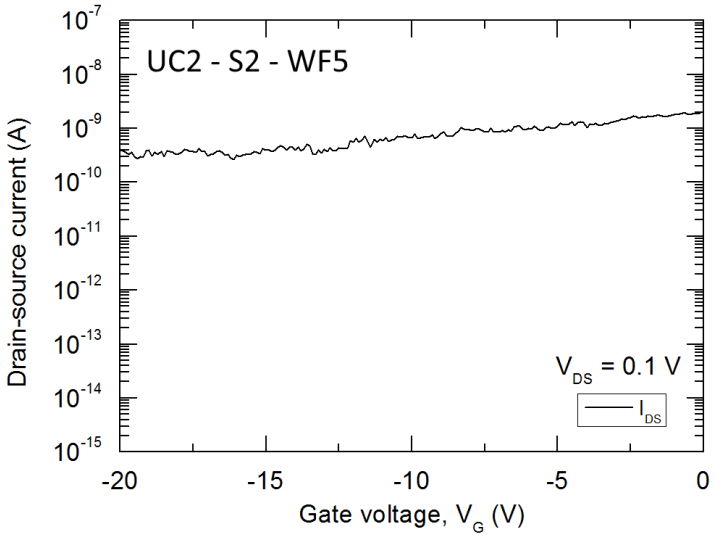

Figure 8.13: Transfer characteristics of UC2 - S2 - WF5. Despite being annealed, the nanowire shows no field dependence.

Unannealed nanowires also show a lack of field dependence. Figure 8.14 shows an attempt to deplete an unannealed nanowire at much higher gate voltages. This particular nanowire (UC2 - S1 - WF11) shows a drain current of $\approx 1 \times 10^{-8}$ A at a drain-source voltage of 0.1 V. The transfer characteristics in Figure 8.14(a) show the gate voltage progressively driven from V_G = 0 V to V_G = ≈-67 V. As the voltage is decreased, the leakage current spikes upwards at V_G = -25 V, until the dielectric layer breaks down catastrophically at V_G = -67 V. At this point the leakage current and drain-source current both drastically increase. Imaging the nanowire in SEM after the transfer measurement shows the extent of the damage, as shown in Figure 8.14(b). The nanowire itself has completely disappeared and the SiO_2 layer between the source and drain electrodes has been cratered. This clearly demonstrates the difficulty in using unannealed nanowires as FETs. The nanowire is shown prior to transfer measurements in Figure 8.10(b).

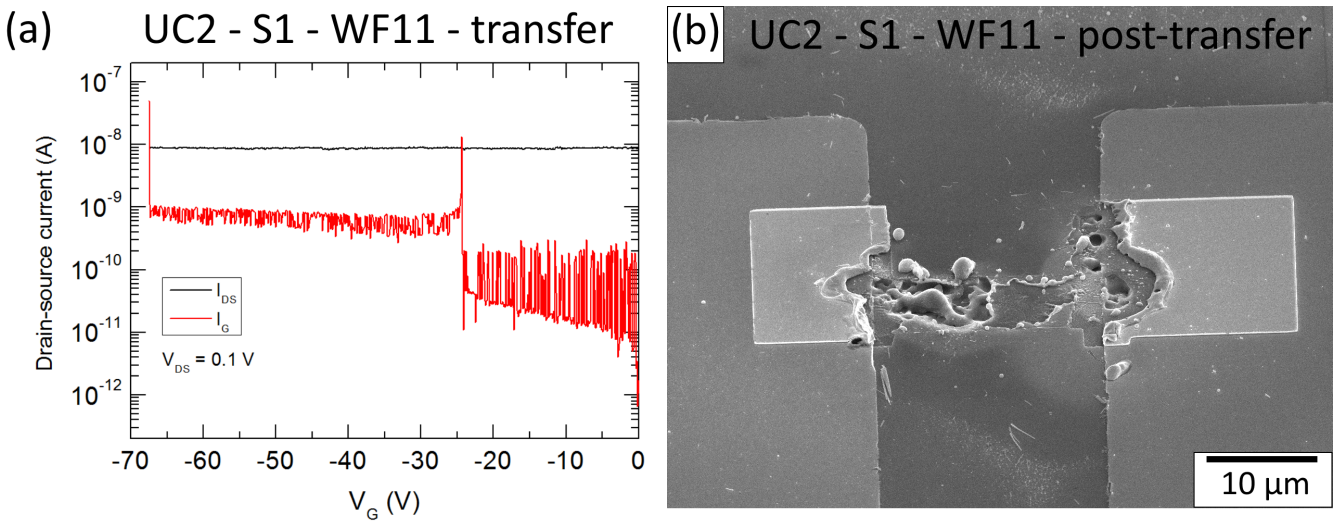

Figure 8.14: (a) Transfer characteristics of UC2 - S1 - WF11. The device is driven at a constant V_{DS} of 0.1 V, and its drain-source current is approximately 1×10^{-8} A. The gate voltage is driven to successively lower voltages in an attempt to deplete the nanowire. Eventually the SiO_2 dielectric catastrophically breaks down at ≈-67 V. (b) An SEM image of the device after the SiO_2 has completely broken down. The nanowire has been destroyed, and the SiO_2 has been damaged. An SEM image of the device prior to breakdown can be seen in Figure 8.10(b).

8.5.3 Conductivity decay and electron beam exposure

All of the contacted nanowires from UC2 - S1, S2, S3, and S4 initially show conduction immediately after lift-off. However, this conductivity rapidly decays over a 48 hour period, with Figure 8.15(a) and (b) showing diode measurements UC2 - S2 immediately after liftoff and 48 hours later. Although these nanowires all initially showed clear conduction, they behave as insulators only 2 days later. This insulating behaviour may be due to significant depletion within the nanowire channel, or extremely high Schottky barrier heights. Although this conducting-to-insulating transition is unusual, and does not have any particular precedent in the literature, it is reproducible and measurable for all of the nanowires measured in all of the samples from UC2.

After a nanowire has undergone a conductor-to-insulator transition, the conductivity of the device can be restored by exposing the nanowire to an electron beam source, such as an SEM. Figure 8.15(c) and (d) shows the same nanowires measured in (a) and (b) (respectively) after the current had decayed, and after the nanowires had been imaged in SEM. This clearly induces a drastic change in the nanowire, which has reverted from insulating to conducting. This ebeam-induced change in conductivity is temporary, and the nanowire once again transitions from a conductor to an insulator typically over 48 - 72 hours.

To ensure that the conductivity change was caused by exposure to the electron beam as opposed to some other coincidental mechanism, such as the low-pressure environment within the SEM chamber, WF8 to WF15 were selectively imaged on UC2 - S2, while the other writefields were left unimaged. As the entire sample is pumped down and subjected to the same conditions, the only difference between the imaged and unimaged nanowires is whether they are exposed to the electron beam of the SEM or not. The nanowires which were left unimaged showed no discernible sign of conduction, with the drain-source current effectively as low as the noise limit for the parameter analyser. Conversely, the nanowires which were imaged by the SEM show clear conduction, with the drain-source current several of orders of magnitude higher than the not imaged nanowires. This conclusively shows that the electron beam is responsible for inducing the temporary transition from insulating to conducting behaviour in the ZnO nanowires.

There are a very limited number of published reports in the literature which relate ZnO nanowire conductivities with exposure to electron beams [234, 235], although the increase in conductivity is relatively mild (1 to 2 orders of magnitude) when compared to the drastic transition from insulating to conducting states observed here. In both instances, the nanowires in question are contacted by back-to-back Schottky barriers.

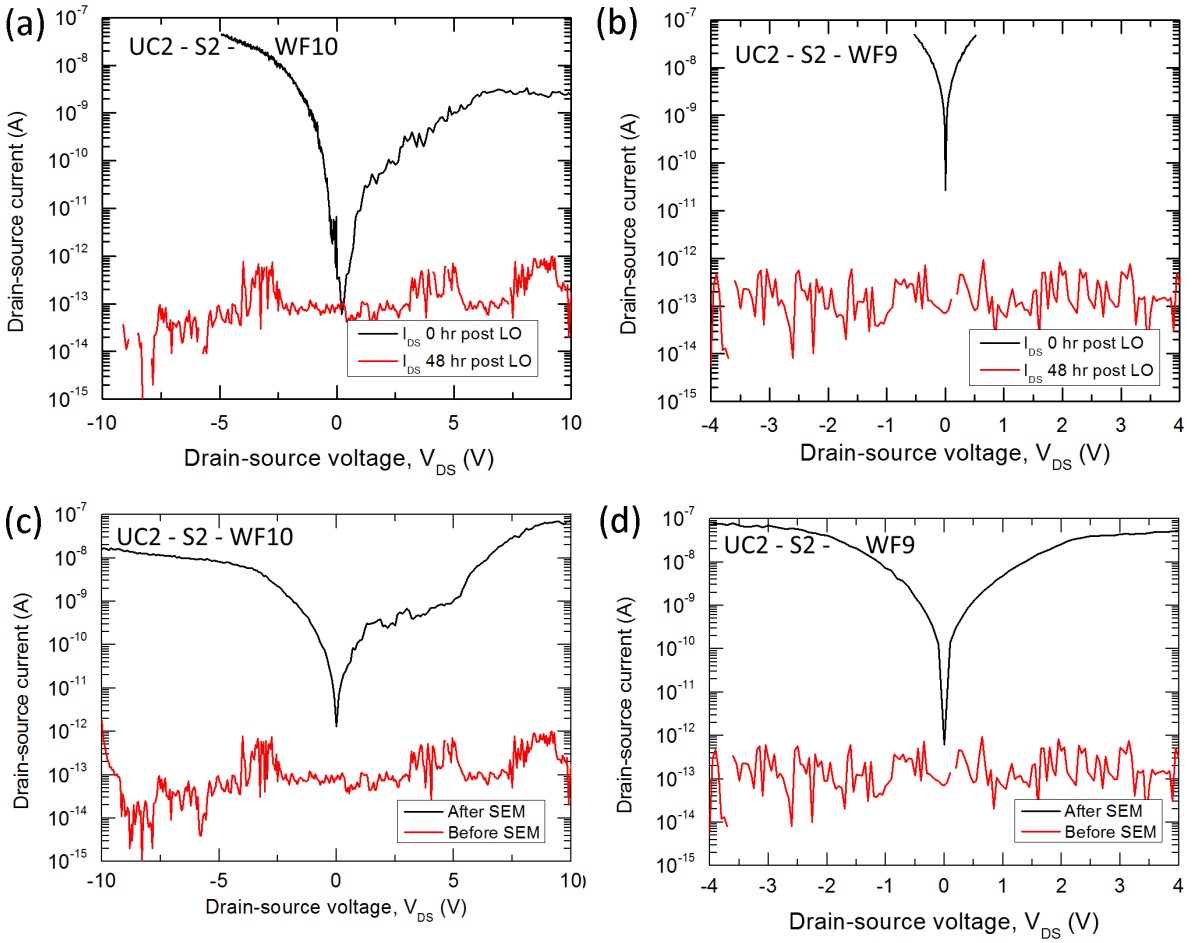

Figure 8.15: Electrical measurements of UC2 - S2 demonstrate the conducting-to-insulating transition the nanowires experience over time after liftoff, and the reversibility of this transition with electron beam exposure. S2 - WF10 and WF9 are shown in (a) and (b), respectively. Both show clear conduction when measured immediately after liftoff (black), but are effectively insulating after 48 hours (red). The short range of voltages measured in (b) is due to the device reaching a compliance of 5×10^{-8} A. WF10 and WF9 are also shown in (c) and (d). The red line shows their IV characteristics several days after liftoff, and they are clearly insulating. After being exposed to the electron beam (shown in black), their conductivity is restored.

Although no conclusive mechanism behind the conductivity increase is given, the proposed theories involve the desorption of oxygen surface states from the nanowires, similar to the influence of UV illumination on the UC1 samples reported in Section 8.4.2 and the hierarchical nanowire FETs in Chapter 6. This would also explain the initial transition from conductive to insulating behaviour we see after the nanowires are lifted off, as the nanowire surface of nanowire may be passivated by the PMMA layer used in EBL until it is removed by the acetone. In theory, this would allow us to re-apply a PMMA layer after the device has been exposed to the electron beam in SEM.

To test this theory, ZnO nanowires from UC2 - S4 were imaged in the SEM several days after being initially lifted off, to allow the nanowires to naturally transition from conducting to insulating behaviour. Once the nanowires were behaving as insulators, the sample was placed into the SEM and the contacted nanowires exposed to the electron beam. Figure 8.16(a) shows electrical measurements of UC2 - S4 - WF5 immediately after liftoff (black), and after 48 hours (red). The conduction of the nanowire has clearly decayed significantly, from an initial maximum current of 10^{-8} A to $\approx 10^{-13}$A. After being imaged in SEM (blue), the nanowire shows a drastic increase in conductivity, as shown in Figure 8.16(b), with a maximum current of $\approx 10^{-6}$ A. This post-SEM current is actually higher than when the nanowire is immediately measured after liftoff - the two measurements are directly compared in Figure 8.16(c). Although the post-SEM measurement shows lower currents within a drain-source voltage of $\approx$ +/-2.5 V, the maximum currents of post-SEM are 2 to 3 orders of magnitude higher than the post-liftoff measurements.

Once the nanowire was measured post-SEM to ensure that it was conductive, a thin layer of PMMA (on the order of hundreds of nm) was deposited on the surface using a spin coater. Figure 8.16(d) shows measurements of UC2 - S4 - WF5 immediately after the PMMA has been deposited and soft-baked onto the device substrate. Although the maximum current of the nanowire remains unchanged in the negative drain-source voltage direction, the drain-source current at a drain-source voltage of 10 V is approximately 3 orders of magnitude lower than the post-SEM measurements. These currents are still both higher than the immediate post-liftoff measurements of the device. A consequent measurement 192 hours (8 days) after the PMMA was applied (Figure 8.16(d), red) shows that the conductivity has decayed significantly from its initial PMMA-encapsulated state, but the nanowire has not undergone an insulating transition. This differs from unencapsulated nanowires which become insulating within 48 hours of liftoff.

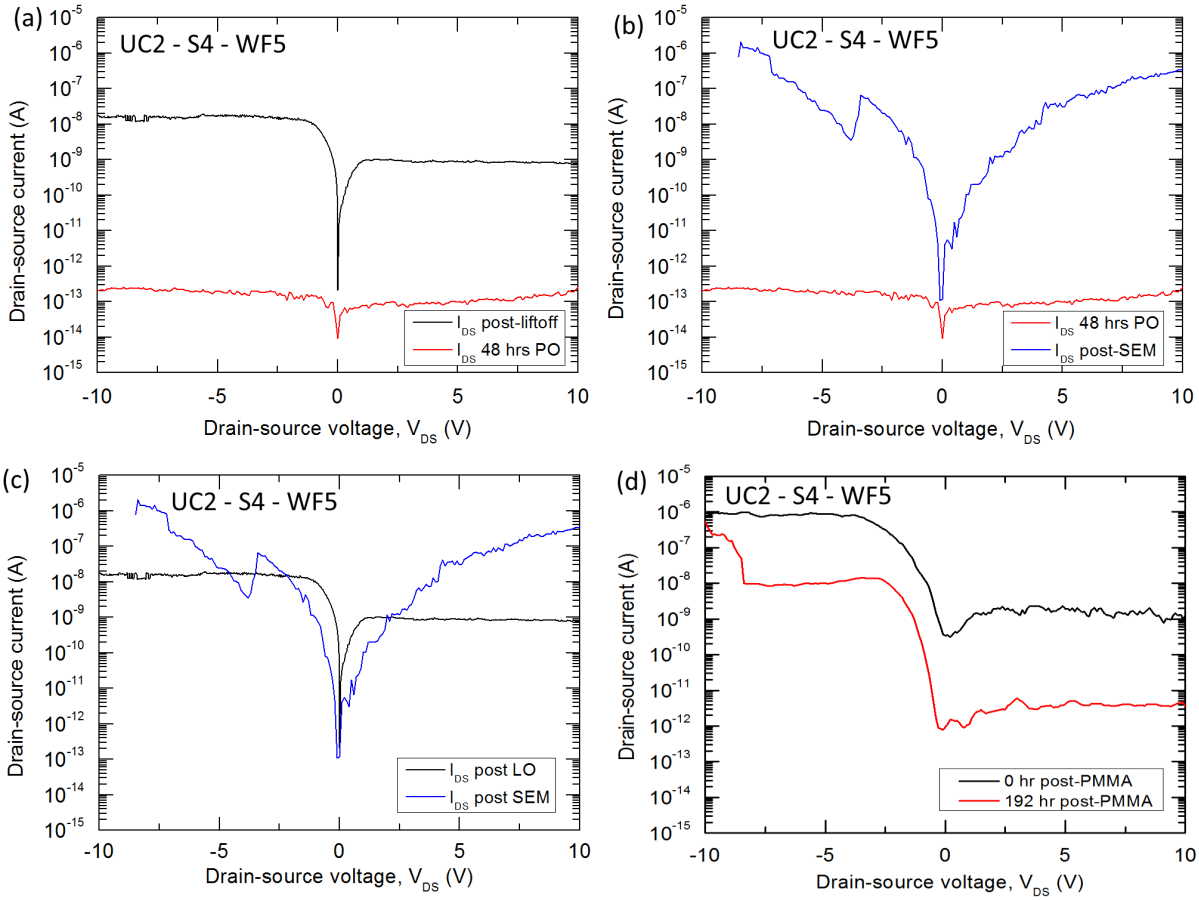

Figure 8.16: (a) Electrical measurements of UC2 - S4 - WF5 after the nanowire was initially lifted off (black) and after 48 hours (red). (b) Electrical measurements of the same device 48 hours after liftoff (red) and immediately after SEM (blue). (c) Measurements after initial liftoff contrasted with measurements immediately after SEM. (d) Electrical measurements immediately after PMMA was deposited on the device (black) and 192 hours after the PMMA was deposited (red).

This significant decay over 192 hours may due to surface species adsorping to the nanowire during the brief period of time between the nanowires being removed from the SEM and the application of PMMA. The fact that the nanowires are conductive immediately after liftoff and turn insulating over 48 hours (with currents on the order of 10^{-13} A within a source-drain voltage of +/- 10 V) suggests an interaction between the nanowires and the environment, which is almost certainly mediated through surface states. This is corroborated by the fact that the conductivity can be temporarily restored to within an order of magnitude or even increased from its original value, by subjecting the body of the nanowire to an electron beam. Furthermore, the conductivity slowly decays again once the nanowire is reintroduced into the atmosphere after SEM measurements have taken place.

8.6 Schottky barrier heights and ideality factors

*red*All of the contacted nanowires which are measured in this chapter show non-Ohmic behaviour, and have been fitted using a back-to-back Schottky barrier model. As we have seen, the Schottky barrier heights and ideality factors derived from this model can vary between two different samples fabricated using the same nanowires, two different nanowires contacted on the same sample, or even two different contacts on the same nanowire. Here, the different SBH (Schottky barrier height) values and ideality factors observed across the devices are summarised.

8.6.1 Relation between contacts on a single nanowire

Schottky barrier heights and ideality factors can be asymmetric or symmetric for a single nanowire. Symmetric devices imply that there are similarities between the two metal/semiconductor contacts on the same nanowire. Despite this, there is a wide variety of Schottky barrier heights between symmetric devices, which may suggest that some variable local to each nanowire determines the barrier height, and that this variable differs between nanowires. Figure 8.17(a) shows the SBH of contact 2 plotted against the SBH of contact 1 for Schottky barriers within 0.75 eV, restricting the dataset to the more symmetric devices. The linear intercept which runs through (0, 0) represents the symmetry line - the closer a nanowire is to this line, the more symmetrical the SBH is. Although there are a large number of symmetric devices, there is a wide variety in the barrier heights between different devices. Similarly, Figure 8.17(b) shows the ideality factor of contact 2 plotted against the ideality factor of contact 1, with devices with contact ideality factors within 0.9 - 1.2. The ideality factors of the contacts show slightly more asymmetry than the barrier heights.

8.6.2 Relation between the SBH, ideality factor, and nanowire diameter

The Schottky barrier heights and ideality factors of both contacts on symmetric devices are highly correlated with one another. Because each pair of contacts has a nanowire in common, it may be expected that there is a relationship between the physical properties of the nanowires and the SBH/ideality factors of the contacts. Furthermore, as there is a well-established relationship between the diameter of a nanowire and its conductivity [179], it would not be surprising to see a relationship between the nanowire diameter and the SBH. Figure 8.18 shows the SBH (a) and ideality factors (b) of both individual contacts plotted against the diameter of the nanowire. However, no clear relationship emerges when the barrier heights and ideality factors are plotted against the nanowire diameter. This suggests that the the SBH and ideality factor may be more

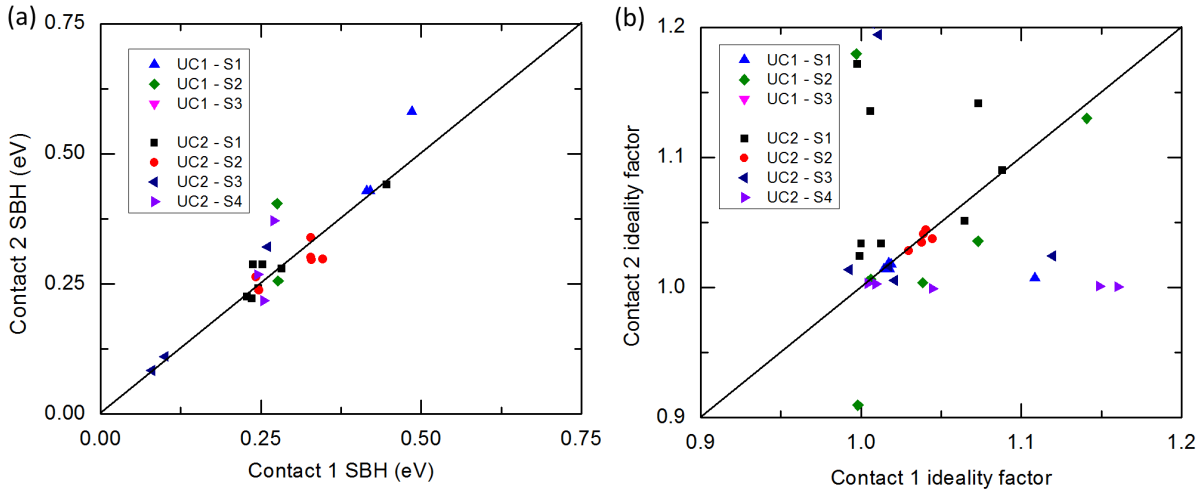

Figure 8.17: (a) The Schottky barriers of pairs of electrodes, restricted to Schottky contacts with barrier heights within 0.75 eV. The linear intercept which runs through (0, 0) represents a line of symmetry. (b)The ideality factors of pairs of electrodes, restricted to contacts with ideality factors within 0.9 - 1.2.

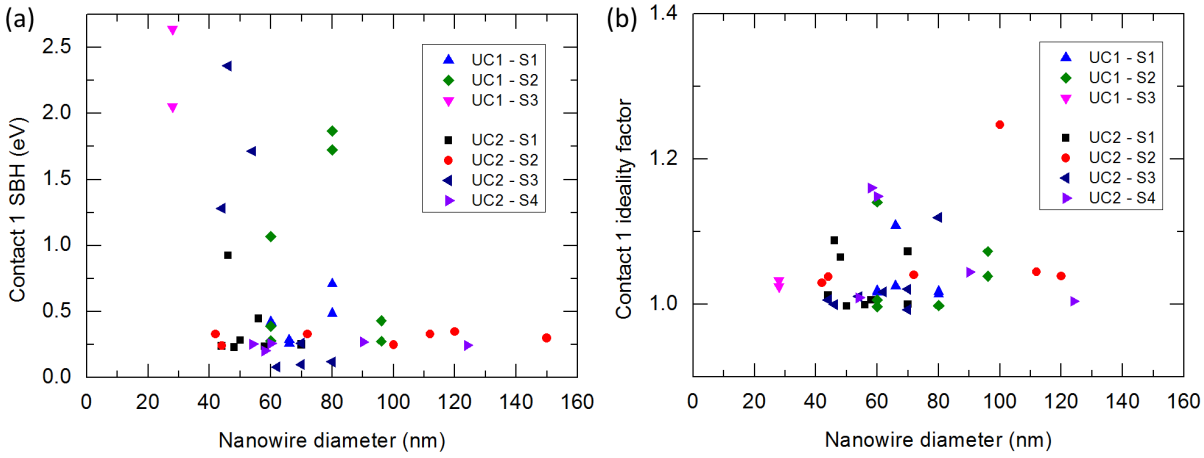

Figure 8.18: The Schottky barrier height (a) and ideality factor (b) of contact 1 and plotted against the radius of the contacted nanowire. No clear relationship emerges between the two.

or less fixed by the surface of the nanowire, or by some other variable which does not depend on the bulk or surface-to-volume ratio of the nanowire.

8.6.3 Nanowire growth conditions and Schottky contacts

The majority of the nanowires contacted here are grown using 6 mM of 8 mM of PEI(M_W = 800), referred to here as PEI(800), along with the standard precursors of 25 mM HMT/$Zn(NO_3)_2$. The growth conditions of the ZnO nanowires have an obvious impact on their diameter, as detailed in Chapter 5. These growth conditions also

may affect the electrical properties of the nanowires, which in turn could influence the Schottky contacts. Furthermore, some of the contacted nanowires have been annealed, while others have been left unannealed. Annealing certainly affects the charge carrier concentration and field dependence of ZnO nanowires, which may in turn systematically influence the Schottky contacts.

Figure 8.19 shows the SBH (a) and ideality factors (b) of both contacts on each nanowire, grouped by their hydrothermal precursors and their annealing treatments. The data has been restricted from 0 - 0.75 eV and 0.9 - 1.2, respectively. Although there is no decisive trend, there may be a tendency for annealed nanowires grown with 6 mM of PEI(800) to show lower SBHs. This trend remains even when accounting for the diameter of the nanowire, which is shown in Figure 8.19(c). The contact ideality factors of annealed nanowires grown with 6 mM of PEI(800) also show a larger degree of symmetry than the other nanowires used here, with only 3 devices deviating significantly from the symmetry line in Figure 8.19(b). These results are also consistent when accounting for nanowire diameter, as shown in Figure 8.19(d), with the bulk of the ideality factors of contact 1 having a value close to unity. These results may suggest that nanowires grown using 6 mM of PEI(800) are more suitable for nanowire devices in general, given the reproducibility of the Schottky contacts.

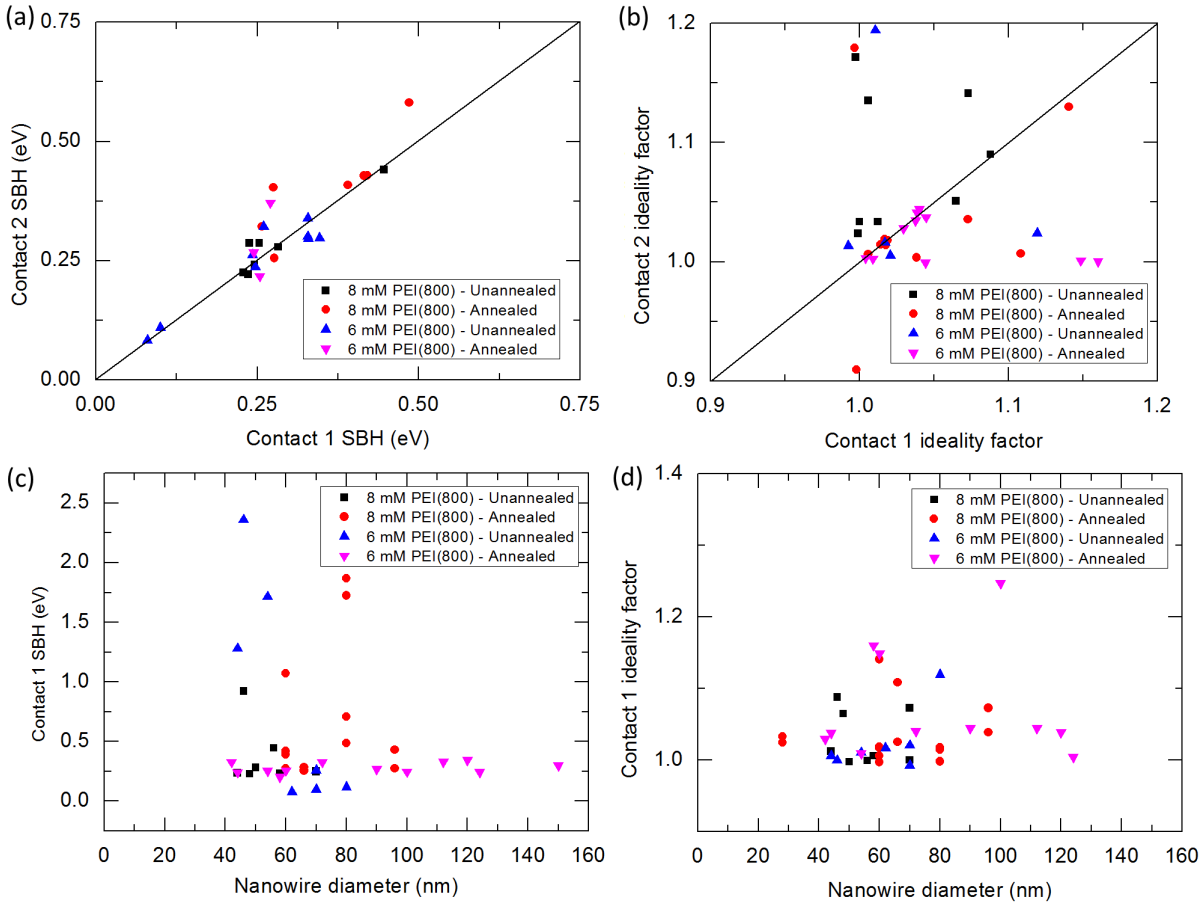

Figure 8.19: (a, b) The Schottky barrier heights and ideality factors of pairs of electrodes, grouped by the nanowire growth conditions. (c, d) The Schottky barrier heights and ideality factors of contact 1 plotted against nanowire diameter, grouped by the nanowire growth conditions.

8.7 Material degradation

Partial etching and complete dissolution of ZnO nanowires occurs when the liftoff time in acetone is 3 or more hours, as reported in Section 8.4. When the samples are imaged in SEM after liftoff, the majority of the nanowires have disappeared, and all that remains is an amorphous residue on the surface of the substrate. Figure 8.20 shows a UC1 sample which has degraded during a 14 hour liftoff in acetone. This particular sample is omitted from Section 8.4, as all of the nanowires have completely degraded and no electrical measurements can be performed.

Figure 8.20(a) shows the amorphous residue left by the etching process on the substrate. Some heavily etched nanowires remain on the substrate. The white portion of right-hand side of the image is a metal electrode on the device substrate, which appears overexposed in order to highlight the residue on the substrate surface. The residue isn't found elsewhere on the sample, and only occurs where the nanowires were prior to liftoff. Figure 8.20(b) shows a composite image of the residue, with some remaining nanowires which haven't been completely etched away. The image consists of a typical secondary electron image (bottom-left), and a backscatter image (upper-right.) Backscatter images give information about the elemental make-up of the material being imaged, as there is a relationship between the contrast of the material and its atomic number. The nanowires are clearly higher in contrast than the residue, which suggests they are composed of different elements.

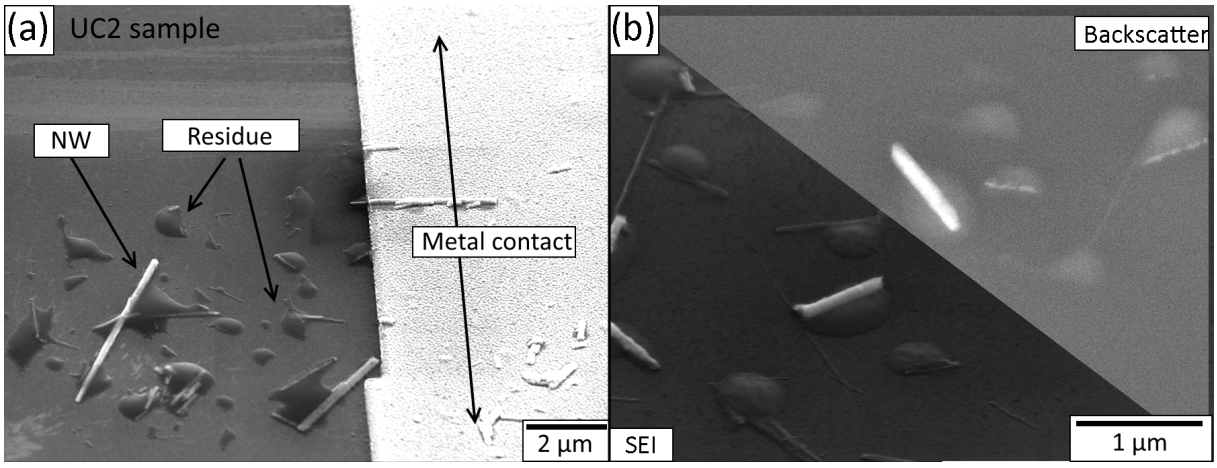

Figure 8.20: Images of nanowires on the substrate of a sample from UC1. The sample was lifted off in acetone over 14 hours, which dissolved the nanowires which had been transferred to the device substrate. The remaining nanowires are covered in a residue on which sits on the substrate surface, which is highlighted in (a). (b) shows a composite SEM image of the nanowires/residue, which is split between SEI and backscatter modes.

After this relationship between the liftoff time and damage to the nanowires was discovered, the liftoff time was reduced to 40 minutes in an effort to prevent damage to the nanowires. This was successful, as the nanowires lifted off in a shorter time showed no obvious damage. However, even the undamaged ZnO nanowires from UC1 and UC2 show complete degradation/dissolution over time when the samples are kept in regular plastic sample containers maintained in atmosphere.

Figure 8.21 shows SEM images of nanowires contacted on UC2 - S2, which were obviously intact immediately after liftoff and at the time of imaging. When they were reimaged after 8 months, it became clear that they had disappeared. Similar to Figure 8.20, all that remains is an amorphous residue on the SiO_2 surface. This behaviour is reproducible and consistent across all of the samples contacted in UC1 and UC2, although the exact timeframe over which the disappearance occurs isn't precisely known at the time of writing.

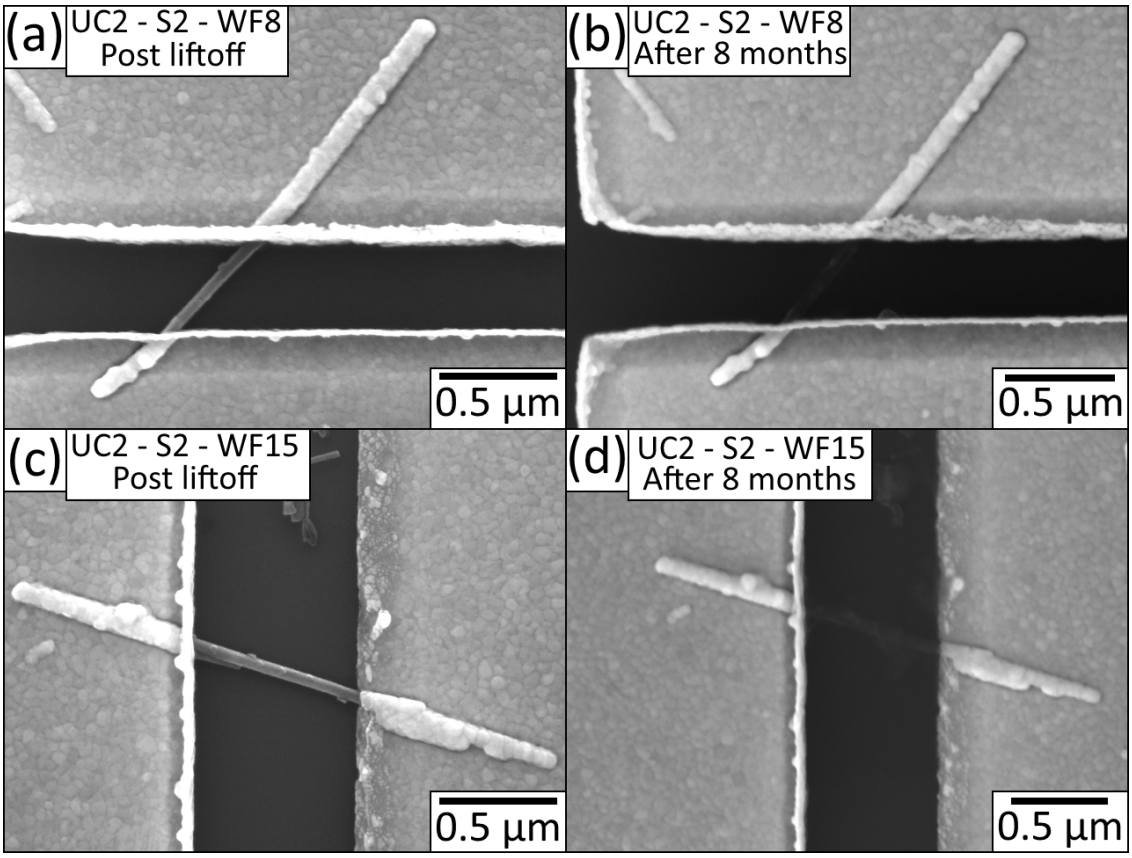

Figure 8.21: SEM images of UC2 - S2 - WF8 and WF15 initially after they were lifted off, and once they were reimaged 8 months later. The nanowires have clearly disappeared some time before the second images were taken. The post-liftoff images of WF8 and 15 are shown in (a) and (c) respectively, while the images taken after an 8 month interlude are shown in (b) and (d).

We don't currently know the mechanism behind the degradation of the nanowires over time. ZnO is an amphoteric material [10], which means that it can dissolve in both basic and acidic conditions. As the nanowires are initially intact when first contacted, the dissolution over time suggests than an interaction between the nanowires and the atmosphere is what drives the material degradation. Furthermore, we have seen ZnO nanowires remain intact when kept under the initial PMMA layer used for electron beam lithography for up to one year, and only degrade over time once the PMMA layer has been lifted off. This reinforces the idea that an atmospheric interaction causes the dissolution of the ZnO nanowires. ZnO nanowires have been reported to dissolve in water over time [236], which may condense from the atmosphere and degrade the nanowires over time.

Another possible mechanism for the degradation of the nanowires over time is carbon capture from the environment. It is well established that PEI captures CO_2 from the atmosphere [237, 238, 239, 240, 241], which may be present on the surface of the nanowires, and that the captured CO_2 molecules are acidic [242, 243, 244]. PEI has a complex interaction with different precursors during the hydrothermal growth, as detailed in Chapters 2 and 5, but it is also thought to bind to the non-polar facets of ZnO while the nanowires are nucleating and growing.

It is not known how much PEI remains on the surface of the nanowires after the hydrothermal growth. Thorough rinsing [174, 74] and high-temperature annealing [245, 246, 73] are typically attributed to removing any residual PEI after nanowire growth, although this is not often directly investigated. Both annealed and unannealed nanowires contacted in this chapter show material degradation over time; if PEI is removed from nanowire surfaces during the annealing process, and CO_2 capture by the PEI is responsible for the material degradation, we would expect the unannealed nanowires to degrade, while the annealed nanowires remain intact. As this is not the case, it is unlikely that there is enough residual PEI on the surface to contribute to material degradation.

However, surfaces of ZnO interact with carbon molecules in the atmosphere [182, 247], and can capture CO_2 without the presence of PEI [248]. Carbon in the form of CO or CO_2 can also generate formate species ($HCHO_2^-$) [249, 250], which are also acidic. Atmospheric interactions with carbon and carbon complexes may still play a role in the degradation of the nanowires, even if the PEI has been completely removed from the nanowire surface.

Nanowires which have degraded eventually over time also leave a residue on

the substrate in their vicinity, even when they are initially intact when lifted off. Figure 8.22 shows an SEM image of partially dissolved ZnO nanowires from UC2 - S2 taken under backscatter conditions. The backscatter measurements are coupled with energy dispersive x-ray spectroscopy (EDS) measurements, which is a technique used to determine the elemental make-up of a material by measuring the energy of x-rays released when the material is bombarded with electrons. Figure 8.22(a) shows the backscatter image of the nanowires, with a clear contrast difference between the nanowires and the residue. Figure 8.22(b) shows an EDS measurement of carbon, which has been overlaid with the backscatter image. The highest concentration of carbon is located in the residue material. Figure 8.22(c) shows an EDS map of Zn (green) and O (blue), also overlaid the backscatter image. Although there are trace amounts of Zn within the residue, the majority of the Zn is confined to the nanowires. Finally, Figure 8.22(d) shows C, Zn, and O overlaid with the backscatter image. This clearly suggests that the residue is rich in C compared to other parts of the image, which supports the idea of carbon accumulation from the atmosphere.

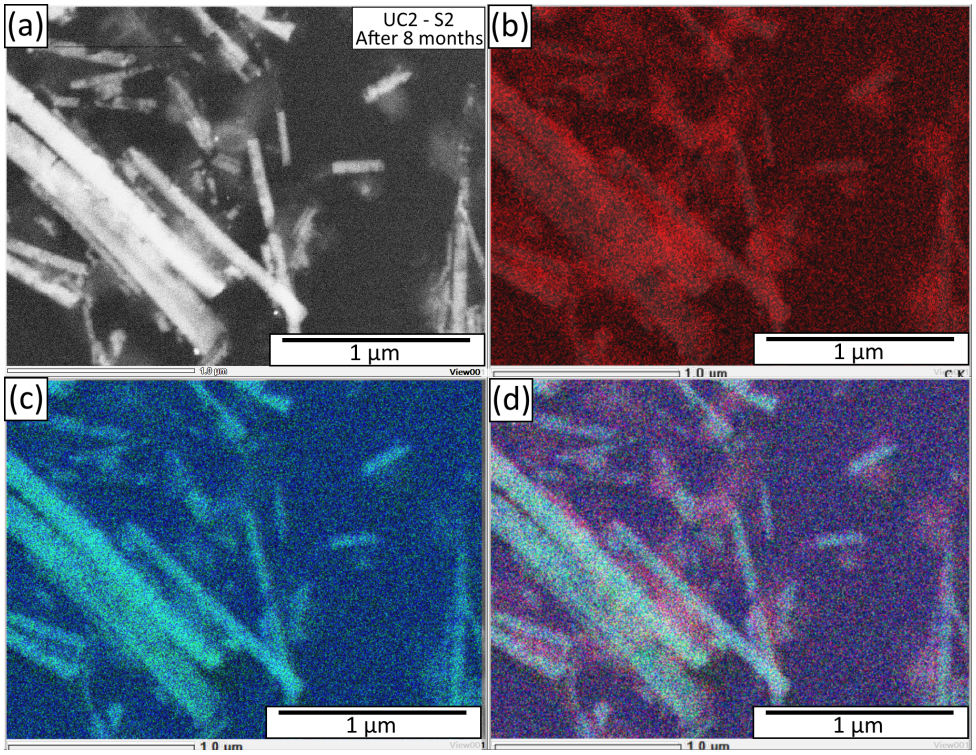

Figure 8.22: (a) A backscatter image of etched ZnO nanowires which are surrounded by amorphous residue. (b) An EDS map of C (red) which is superimposed over the backscatter image shown in (a). (c) An EDS map of Zn (green) and O (blue) which is superimposed over the backscatter image in (a). (d) A composite EDS map showing C, Zn, and O. The residue clearly has a high concentration of C compared to the surrounding substrate/nanowires.

8.8 Summary

In summary, two functioning FETs were fabricated in total. One of these FETs (UNSW1 - S1 - WF17) used an unannealed nanowire grown vertically with 1.5 mM of PEI(M_W = 2000 g/mol.) The device operated with an on-off ratio of 10^4 and a threshold voltage of -7 V, a transconductance of 1.65 nS, and a minimum subthreshold swing of 937 mV/decade. The field-dependent mobility of the FET is approximately 0.11 $cm^2\ V^{-1}\ s^{-1}$. The second FET (UC1 - S3 - WF3) used a lateral secondary nanowire which was isolated from a field-dependent hierarchical FET. The individual secondary nanowire operated with a threshold voltage of -6.2 V, an on-off ratio of 10^2, a transconductance 30.1 nS, and a subthreshold swing of 845 mV/decade. The mobility was calculated to be 2.96 $cm^2\ V^{-1}\ s^{-1}$.

Other contacted nanowires showed consistent back-to-back Schottky behaviour, but were field independent. The measurements on single ZnO nanowires presented in this chapter raise several outstanding questions about the material properties of ZnO nanowires, their reactions with the environment, and the fabrication of ZnO nanowire devices. These can be summarised as follows:

- **What determines the Schottky barrier height and ideality factor of single nanowire contacts?**
  While there are reports on the various factors that influence the Schottky barrier height [251], the results presented here show a variety of barrier heights despite using ostensibly identical or very similar nanowires and contact metals. While there is a clear relationship between the Schottky barrier heights and ideality factors of two contacts on a single nanowire, there isn't any obvious relationship between the barrier heights/ideality factors of the contacts and the physical properties of the contacted nanowire. Determining the variables which influence the Schottky barrier height/ideality factor of a contact would allow for more reliable and reproducible fabrication of a number of single nanowire devices, which utilise both Schottky and Ohmic contacts.

- **What determines the field dependence of ZnO nanowires?**
  We have seen one example of a vertically-grown ZnO nanowire from the UNSW batch which shows reliable field dependence (specifically UNSW1 - S1 - WF17 in Section 8.3.2). Other nanowires contacted on the same chip do not show field dependence, even though they originate from the same growth substrate and are contacted the same way. Why is this nanowire in particular field dependent, while the other nanowires are not? Similarly, a field dependent secondary nanowire is contacted in Section 8.4, and shows response to gate voltages de-

spite the relatively high leakage currents. This is unsurprising, as the secondary nanowires are field-dependent when used in lateral FETs, but what are the critical differences between the secondary nanowires and the vertical nanowires which determine field dependence?

- **What causes the conducting-to-insulating transition of the UC2 nanowires contacted in Section 8.5?**
  All of the nanowires contacted from UC2 in Section 8.5 show a dramatic transition after liftoff between conductive and insulating states over 48 hours. This transition can be temporarily reversed by exposing the samples to an electron beam, such as an SEM. What causes this initial transition, and what mechanism allows it to be reversed? If the transition occurs due to interactions with the nanowire and the atmosphere, why doesn't encapsulation in PMMA retain the conductive state after the device is exposed to the electron beam? And why do other single nanowire devices not show the same transitions over time?

- **What causes the ZnO nanowires to dissolve over time after liftoff?**
  The nanowires contacted from the UC1 and UC2 batches of nanowires (in Sections 8.4 and 8.5 respectively) show dramatic degradation over time when stored in plastic containers in ambient air, eventually dissolving entirely over the course of at least 8 months. Interactions between atmospheric carbon and the ZnO nanowire surface is one possible mechanism for this dissolution, as are interactions with atmospheric water. However, if either of these mechanisms destroy the ZnO nanowires over time, why do other nanowires grown under identical conditions - including the untransferred nanowires which remain on the dedicated growth substrates - remain intact even after several years?

The unanswered questions presented in this chapter motivate a substantial amount of future work, which is presented in Chapter 9.

Chapter 9

Conclusion and future work

9.1 Conclusion

This thesis has explored the hydrothermal synthesis of ZnO nanowires and their application in field-effect transistors. Field-effect transistors have been successfully fabricated by bridging electrodes with hierarchical ZnO nanowires, grown via both PEI-mediated one-pot and modular two-pot hydrothermal growths. Significantly, these devices show field dependence without requiring high-temperature annealing. One-pot devices can be used dry, with on-off ratios of 10^3 - 10^5 and threshold voltages between -7.5 V to 5 V. Two-pot devices are measured in a wet environment using back and top gates, with on-off ratios and threshold voltages of 10^5 and 8 V, and 10^3 - 10^4 and 0.4 - 0.9 V, respectively. Vertically-grown nanowires have been individually contacted using electron-beam lithography, although only one nanowire showed field dependence. All of these nanowires showed complete dissolution over an 8 month period, and a conducting-to-insulating transition over 48 hours. This transition can be temporarily reversed by exposure to an electron beam.

9.1.1 Hydrothermal synthesis of vertical ZnO nanowires

The influence of polyethylenimine (PEI) on the hydrothermal growth of vertical ZnO nanowires from seeded substrates was thoroughly investigated. Hydrothermal growths were carried out using PEI at a range concentrations between 2 mM to 8 mM, with PEI molecular weights of 800, 1300, and 2000 g/mol. These hydrothermal growths resulted in either homogeneous nanowires, hierarchical nanowires, thin ZnO films, growth suppression, or substrate etching, depending on the PEI concentration used.

The homogeneous ZnO nanowires were compared to control ZnO nanowires, which were grown without PEI. All of these homogeneous nanowires had improved

lengths over the control nanowires, which had average lengths of 1.6 μm. The longest homogeneous nanowires were grown with 8 mM of PEI(M_W = 800 g/mol), with an average length of 10.5 μm. Similarly, all of the homogeneous nanowires had improved aspect ratios over the control nanowires, which had average aspect ratios of 32. The nanowires with the highest aspect ratios were grown using 6 mM of PEI(M_W = 800 g/mol), which had average aspect ratios of 153.

The synthesis of hierarchical ZnO nanowires occurs at 4 mM of PEI(M_W = 1300 g/mol). These nanowires consist of a large primary nanowire which abruptly terminates in a thin, long secondary nanowire. These secondary nanowires are up to 10 μm long and below 50 nm in diameter. The synthesis of the hierarchical nanowires is attributed to two separate growth phases within the single PEI-mediated hydrothermal growth.

9.1.2 PEI-mediated growth of hierarchical ZnO nanowire FETs

ZnO nanowires were grown laterally from ZnO/Ti films that were patterned on SiO_2/Si device substrates. These were grown using identical concentrations and molecular weights of PEI used in the vertical ZnO nanowire synthesis. Hierarchical nanowires were synthesised using 8 mM of PEI(M_W = 800 g/mol), 3 & 4 mM of PEI(M_W = 1300 g/mol), and 2 & 3 mM of PEI(M_W = 2000 g/mol). FETs were fabricated by allowing the secondary nanowire portion of the hierarchical nanowires to intersect between pairs of ZnO/Ti films, which were used as source and drain electrodes. All of these hierarchical nanowire FETs showed significant field dependence without requiring any annealing step, with on-off ratios between 10^3 - 10^5 and threshold voltages between -7.5 V to 5 V.

Persistent photoconductivity measurements of the hierarchical nanowire FETs show that depleting oxygen/hydroxyl surface states on the nanowire sufficiently reduce the charge carrier concentration to allow for as-grown field dependence. These conclusions are supported by persistent photoconductivity measurements of field-independent FETs which are bridged with primary nanowires. The ZnO nanowire surface and the surface-to-volume ratio therefore play a critical role in determining their suitability in FET applications.

9.1.3 Modular growth of hierarchical ZnO nanowire FETs

The previous hydrothermal growth of hierarchical ZnO nanowires relies on two growth phases within a PEI-mediated hydrothermal growth. Lateral hierarchical

nanowires were grown on SiO_2/Si device substrates in a modular fashion by separating the two growth phases into individual primary and secondary hydrothermal growths. The preheat time of the primary growth and presence of PEI in both growths were investigated to optimise the reproducibility of the synthesis route. The most reproducible combination was found to be a primary growth preheated for 20 minutes, with neither the primary or secondary growth containing PEI. This yielded a reproducibility of 50%.

FETs were fabricated by bridging separated ZnO/Ti films on the SiO_2/Si substrate. These hierarchical nanowire FETs showed unreliable field dependence when measured in air, with only some devices responding to applied fields. This is in contrast with the PEI-mediated hierarchical nanowires FETs, which consistently show field dependence. The best modular-grown FET operates with an on-off ratio of 10^4 and a threshold voltage of $\approx$0 V. Devices which are field-independent in air can reliably be used as FETs by back-gating and top-gating the devices in a wet environment, using de-ionised H_2O as the dielectric. A device which is field-independent in air is wet back-gated, and operates with an on-off ratio of 10^5 and a threshold voltage of $\approx$8 V. Wet top-gated devices operate with on-off ratios of 10^3 - 10^4, and threshold voltages within 0.4 - 0.9 V. These FETs have significantly low subthreshold swings on the order of 80 mV/decade.

9.1.4 Individually contacted ZnO nanowires

Vertical ZnO nanowires were hydrothermally synthesised on dedicated growth substrates and then transferred to SiO_2/Si and HfO_2/SiO_2/Si device substrates. After being transferred, the nanowires were individually electrically contacted using electron beam lithography. The nanowires were grown using 1.5 mM of PEI(M_W = 2000 g/mol) and 8 & 6 mM of PEI(M_W = 800 g/mol). All of the contacted nanowires show back-to-back Schottky contact behaviour. Only one of these contacted nanowires showed field dependence, which was grown using 1.5 mM of PEI(M_W = 2000 g/mol). This FET operates with an on-off ratio of 10^4 and a threshold voltage of -7 V. The transconductance of the FET is 1.65 nS, and the mobility is calculated to be 0.106 cm^2 V^{-1} s^{-1}. Other nanowires contacted on the same device substrate do not show field dependence.

Secondary nanowires were also isolated from lateral PEI-mediated hierarchical nanowires and contacted on an SiO_2/Si device substrate. These hierarchical nanowires were grown from lateral substrates using 8 mM of PEI(M_W = 800 g/mol). The SiO_2/Si substrate allows excessive leakage currents due to a damaged dielectric,

although one contacted nanowire can be measured. This FET shows field dependence, with an on-off ratio of 10^2 and a threshold voltage of -6.2 V. The transconductance of this FET is 30.1 nS, and the mobility is calculated to be 2.964 $cm^2\ V^{-1}\ s^{-1}$.

All of the vertical nanowires grown with PEI(M_W = 800 g/mol) completely disappear from the device substrate over at most 8 months. This may be caused by carbon accumulation or by exposure to atmospheric water. Additionally, a portion of these nanowires undergo a conducting-to-insulating transition over 48 hours. This transition can be temporarily reversed by exposure to an electron beam. The conducting-to-insulating transition and its reversibility is likely caused by an accumulation of depleting surface states, which can be temporarily removed by an electron beam. This may be related to the mechanism which causes the disappearance of the nanowires over time.

9.2 Future work

This research topic could continue in several different directions if more time was devoted to it. These individual research projects could specifically continue the work of each results chapter; namely, the vertical hydrothermal growth of ZnO nanowires, the PEI-mediated and modular growth of hierarchical nanowire FETs, and the individually contacted ZnO nanowires. These further projects could improve the applications of ZnO nanowires in FETs from a practical point of view, and also shed light on fundamental questions regarding the material properties of ZnO nanowires which remain unanswered.

9.2.1 PEI-mediated hierarchical nanowire growth over time

The synthesis of hierarchical nanowires in a single PEI-mediated hydrothermal growth is attributed to two distinct growth phases, where the second growth phase is driven by a gradual release of Zn^{2+} ions which have complexed with PEI molecules. Strong empirical evidence has been presented in this thesis to argue that this is the case, but quantitative measurements of the growth solution would further clarify the exact growth mechanism, and the timeframe over which the secondary nanowires are grown. The concentration of zinc over time in the hydrothermal growth solution is able to be measured on the parts-per-million level by using atomic absorption spectroscopy [252], and the hydrothermal growth of ZnO nanowires can even be imaged in situ using transmission electron microscopy [253]. Measurements such as these could potentially identify when the secondary growth phase specifically begins during the hydrothermal growth, and what the exact growth conditions are. Hydrothermal growth condi-

tions could then be tailored to emulate the secondary growth phase over the duration of the entire hydrothermal growth, omitting the primary growth phase entirely. This could lead to a more efficient and reliable secondary nanowire synthesis, which may not require the use of PEI.

9.2.2 Hierarchical nanowire FETs as device platforms for biosensors

Modular hierarchical-nanowire FETs are measured in wet environments using deionised water as a gate dielectric in Chapter 7. This is used to achieve field dependence of the devices, allowing for operation in back-gate and top-gate configurations. Developing field-effect transistors which operate in wet environments paves the way for the fabrication of biosensors, which have been identified as an important emerging application of nanoelectronics [254]. Although field-effect transistors are important devices for semiconducting nanowire biosensors [255], biosensors are rarely based on ZnO nanowire field-effect transistors [256]. Biosensors which do use ZnO nanowires as field-effect transistors use individually contacted nanowires which are fabricated using high-temperature methods [257, 258]. The long-term applicability of these devices remains uncertain, as ZnO nanowires rapidly dissolve in many liquids used for biosensing applications [236], and are ideally disposable in the first place. This discourages devices which are fabricated using expensive or laborious processes, such as electron beam lithography.

In contrast, the fabrication of PEI-mediated and modular hierarchical nanowires in Chapters 6 and 7 is comparatively inexpensive and scalable, as the growth substrates also double as the device substrates. Furthermore, the hydrothermal growth is perfectly suited for industrial throughputs, as many nanowire devices and FETs can be grown in parallel. As such, there is a real opportunity to use both the PEI-mediated and modular hierarchical nanowire FETs presented in this thesis as device platforms for biosensing. This would require further research into the functionalisation of the surface of the hierarchical nanowires, and more research into maximising the reproducibility of electrical characteristics between devices. This may favour a modular approach to the hierarchical nanowire synthesis, as there is ostensibly more control over the growth conditions.

9.2.3 ZnO nanowire sensitivity to electron beam exposure

Some of the nanowires contacted in Chapter 8 show a drastic transition from an initially conductive state into an insulating state over 48 hours. This transition can be temporarily reversed and the conductivity restored by exposing the nanowires to an electron beam, although the nanowires return to an insulating state after another

48 hours. This is attributed to depleting oxygen and hydroxyl states on the surface of the nanowire which trap electrons. If the conducting-to-insulating transition is mediated by surface states which accumulate from the ambient environment, this may be exploited to serve as the basis for an environmental detector or monitor based on the resistance of a nanowire. Although it is impractical to refresh the conductance of the nanowire using an electron beam, a similar effect might possibly be achieved by using ultraviolet light.

In any case, experiments should be performed to conclusively determine what surface species are adsorping to affect the nanowire resistance, or whether the conductance transition is driven by a different mechanism. One possible technique that could be used is x-ray photoelectron spectroscopy (XPS), which is useful for determining the elemental makeup of the surface of materials. These experiments would most likely have to be conducted on separate nanowires with similar diameters which were contacted at the same time, rather than repeated measurements of a single nanowire, as the XPS measurements may intrinsically change the surface of the nanowire.

The electron-beam induced insulating-to-conducting transition of the material has wide implications for the characterisation of ZnO nanowires and ZnO nanowire devices. ZnO nanowire devices are typically imaged using techniques which involve exposure to electron beams, such as scanning electron microscopy, and techniques which use electron beams may be employed in their fabrication, such as electron beam lithography. The sensitivity of regular ZnO nanowires to these experimental methods should be determined in order to assess whether they may affect fabricated devices in unintended ways. The electron beam doses that the ZnO nanowires were exposed to in this thesis were relatively uncontrolled, as the aperture of an SEM was used as the electron beam source. A systematic study could be performed by using an electron beam lithography system, where the exact electron beam dose can be specified. Specified electron beam dosages could be followed up by XPS measurements, which would paint a comprehensive picture of the ZnO nanowire surface states, and how the surface may unintentionally change during regular experimental procedures such as SEM imaging.

9.2.4 ZnO nanowire dissolution over time

Nanowires which are contacted from UC1 and UC2 in Chapter 8 dissolve over an 8 month period. If there were sufficient time to explore this further, a series of experiments would be dedicated to tracking this dissolution more carefully over time at regular intervals, using further SEM measurements. These experiments would ideally

be performed in conjunction with further XPS measurements, to track how the surfaces of the nanowires change over time. Furthermore, this set of experiments would tie in to the transitions between conducting and insulating states of the nanowire, as the characterisations to determine how the surface states evolve over time may influence the results. These experiments may have wide-reaching implications regarding the ageing of ZnO nanowires and ZnO nanowire devices in the atmosphere.

Appendix A

Electron beam lithography procedure

A.1 Electron beam lithography

As discussed in Section 4.2.1 in Chapter 4, photolithography is a method of patterning areas of a substrate using ultraviolet light. The smallest feature size is therefore theoretically limited to the wavelength of the UV light, due to the diffraction limit. In practice, the maximum resolution of photolithography is usually much larger than the theoretical limit, and is typically on the order of microns. While this isn't an issue when defining relatively large electrodes or other features, it poses a problem if one wishes to make contact to individual nanowires, which requires resolutions on the order of hundreds or even tens of nanometres.

To this end, electron beam lithography (EBL) is a relatively commonly technique used to fabricate electronic devices using single nanowires. EBL is analogous to photolithography, although the lithographic resist is exposed using a beam of collimated electrons rather than ultraviolet light. This offers much greater resolution than photolithography, in the same way that electron microscopy offers much greater resolution than optical microscopy. It also affords a greater flexibility over the design of the features to be patterned, as the patterns are not constrained to a fixed mask, unlike photolithography. This allows for custom-made patterns designed on-the-fly to suit specific nanowires.

EBL has been used throughout this thesis to fabricate the FETs and other electronic devices which make use of single ZnO nanowires, as in Chapter 8. This appendix aims to describe the steps used to prepare single nanowires for patterning, and the EBL process itself.

A.1.1 Device substrate fabrication

The lateral ZnO nanowire FETs employed in Chapters 7 and 6 use a single substrate for nanowire growth and FET fabrication. In comparison, when contacting individual nanowires using electron beam lithography (EBL), nanowires are first grown on a dedicated growth substrate, and then transferred to a separate device substrate. The growth of vertical nanowires is described in Chapter 5. The fabrication of device substrates for EBL is very similar to the fabrication of lateral growth substrates (described in Section 4.2 of Chapter 4), although regular metals are used for electrodes instead of ZnO/Ti.

As the single-nanowire FETs fabricated in this work use a global back gate, we begin with an SiO_2 (100 nm) / p^+-Si wafer, with the SiO_2 layer ultimately serving as a gate dielectric. The wafers are cleaned and protected with AZ1518/PDMS before depositing a 5/50 nm Cr/Au layer on the wafer back to serve as a gate electrode. After the wafers have been protected and their backs metallised, they are cleaved into 1.5×1.1 cm substrates and the protective layers removed in acetone.

Electron beam lithography is designed to pattern and expose minute areas of the substrate, which makes it unsuitable for defining the comparatively large metal pads used to electrically measure the contacted nanowires via probing. As such, we use a photolithography step to define the bulk area of the electrode structure, which is then in turn contacted using EBL. To this end, after the substrates have been cleaved and cleaned, they are prepared for photolithography as per Section 4.2.1 of Chapter 4. The AZ1518-coated substrates are exposed for 10 seconds using the Karl Suss MJB3, and developed in 3:1 AZ326:DI H_2O for 40 seconds before being rinsed twice.

The mask used to define the electrodes is shown schematically in Figure A.1. Each chip features 15 pairs of electrodes, which will eventually be used to individually contact 15 separate nanowires. The gaps between electrodes are either 20 μm or 40 μm, depending on the exact mask used. The electrode gaps are intentionally grouped at the centre of the chip, which reduces any astigmatism or other imperfections in the electron beam lithography alignment. Because the dimensions and tolerances used in EBL are on the order of tens to hundreds of nanometres, small misalignments can completely ruin the EBL process. The mask also features a right-angle cross-bar. This cross-bar is used to align the EBL system, and also serves as a reference point during the EBL process.

After photolithography, Ti/Au ($\approx$80/20 nm) is deposited on the substrates using the Angstrom Engineering NexDep evaporator. The Ti layer is deposited using a elec-

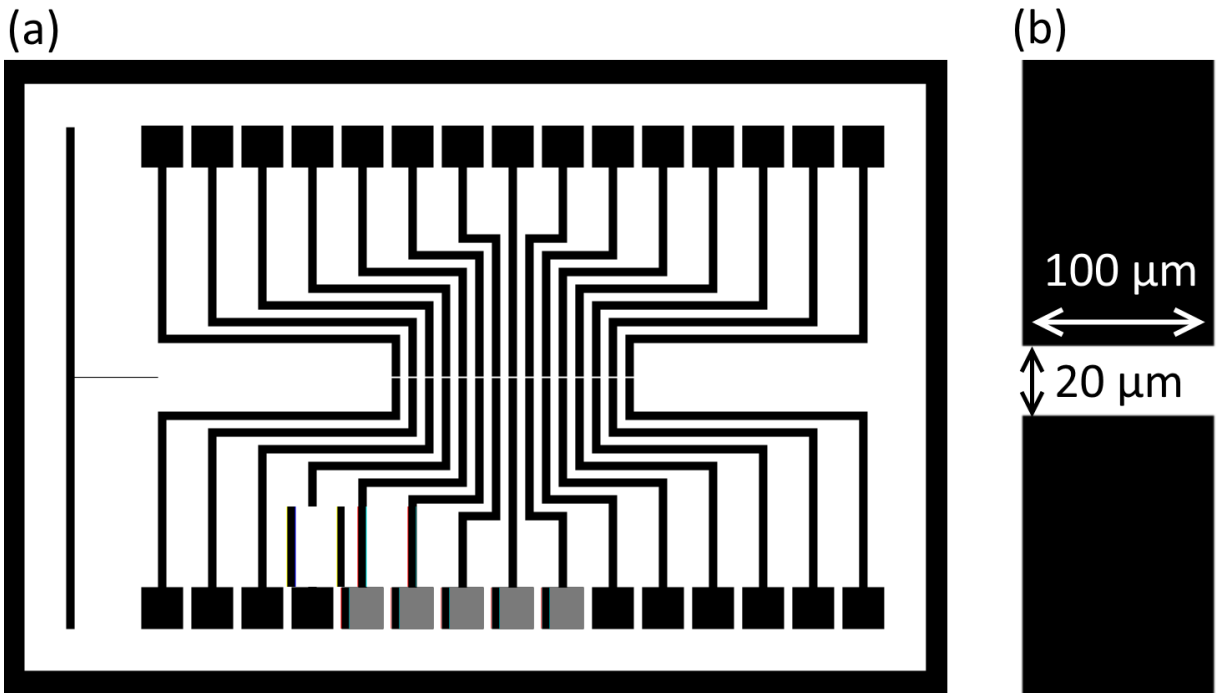

Figure A.1: (a) The photolithographic mask design used to define the large electrodes for EBL. The black portions of the schematic appear as holes in the mask, while the white portions are chrome. The cross-bar (shown on the far left of the schematic) is used for alignment purposes. (b) A close-up of one of the electrode gaps (not to scale.) The electrodes are spaced 20 μm apart, and are 100 μm in width. We have also made use of a 40 μm gap variant of the mask.

tron gun powered by a Telemark TT6 power supply. The Ti used is 99.995% pure Ti wire sourced from Kurt J. Lesker, held in a graphite crucible. The Au (Regal Castings Ltd.) is resistively evaporated using a tungsten boat. The Ti layer serves as an adhesion layer, while the Au layer prevents oxidisation. Once the Ti/Au electrodes have been deposited, the device substrates are lifted off in acetone in cleaned using IPA.

A.1.2 Nanowire transfer and imaging

Once the device substrates have been fabricated, the vertical nanowires we wish to contact are transferred from their growth substrate to the device substrates. We have tried several methods of transfer, although the best method (and the method utilised in this thesis) is the tex-wipe transfer method, adopted from the nanoelectronics group at the University of New South Wales. A small triangle is cut from a cleanroom-grade tex-wipe using a dedicated pair of scissors, with particular care taken to obtain sharp and crisp corners free of fibers. The tex-wipe triangle is held using a pair of tweezers and the tip of a corner gently drawn across the surface of the nanowire growth substrate several times, which accumulates nanowires on the tex-wipe tip.

The tip of the corner is then carefully "dotted" between the electrode gaps on the device substrate, akin to pointillism – indeed, this particular transfer method is perhaps more of an art than a science, requiring a steady hand not only to place the tex-wipe tip roughly in between the electrodes, but also to transfer the right amount of nanomaterials. If too few nanowires are transferred, there won't be enough nanowires suitable for contact via EBL. Conversely, if too many nanowires are transferred, the electrode gaps may be unintentionally bridged with nanowires, or the nanowires clumped in too dense aggregates, which makes it impossible to contact single nanowires individually. It is best to err on the side of transferring too few nanowires, and then assess using optical microscopy. If more nanowires are required, the tex-wipe tip can be re-applied to the device substrate (or growth substrate) as many times as necessary. As with everything else in life, practice makes perfect.

The device substrate is imaged using scanning electron microscopy (SEM) once a suitable number of nanowires have been transferred from the growth substrate. These images serve as a record of the locations of the nanowires. During the EBL process, the nanowires will be very difficult to see underneath the EBL resist, so it is critical to know where the nanowires lie between the electrodes. The images also have to contain suitable reference points, such as small irregularities in the photolithographically-defined electrode edges or comparatively large nanostructures, which will be visible underneath the EBL resist layer.

The most useful images are taken at a magnification roughly equivalent to the images acquired during the EBL process. This magnification is fixed by the width of the writefield (explained in Section A.1.3). This corresponds to 2,400x magnification for the EBL performed in this thesis. The bulk of the device substrates in this thesis have been imaged using Victoria University's JEOL 6500F FESEM, which is only capable of acquiring images at quantised magnification values. The closest magnification for this SEM is 2,500x.

It is also useful to map the entire electrode gap and nearby regions of the device substrate using SEM, which requires 9 to 12 separate SEM images for each pair of electrodes, depending on the electrode gap length (20 μm or 40 μm.) Figure A.2 shows a single SEM image of a device substrate - nanowires are clearly visible between the photolithographically-defined electrodes, the edges of which are also in the frame of the image. The bottom-left inset of Figure A.2 shows a pair of electrodes roughly divided into 25$\times$25 μm areas, which need to be individually imaged to map the entire electrode area. This ensures that the location of any nanowire suitable for contact via EBL has been captured, and can be inferred from reference points during the EBL process. The main body of Figure A.2 is taken from position 5.

A.1.3 Electron beam lithography

The first step in the EBL process is to apply an e-beam resist, which is insoluble in developer unless exposed to an electron beam. We use a bi-layer stack of polymethylmetharcylite (PMMA) as our resist, which is a very common polymer used widely as an e-beam resist throughout the literature. The first layer of PMMA has a low molecular weight (LMW) (M_W = 120,000 g/mol), which is dissolved in chlorobenzene at 4% by weight. This is spincoated onto the substrate surface at 3000 RPM for 1 minute using a spin coater. After the first layer of PMMA has been applied, the device substrate is placed into a convection oven for 30 minutes at 80°C to bake off excess solvent. After this first soft bake, a high molecular weight (HMW) (M_W = 996,000 g/mol) layer of PMMA is applied to the device substrate via spin coating at 3000 RPM for 1 minute. This HMW PMMA is dissolved in O-xylene at 2.5% by weight. After the HMW layer has been applied, the substrate is returned into the convection oven for another 30 minutes to ensure there is no residual solvent. Both of the LMW and HMW PMMA solutions have been prepared at the University of Canterbury.

The bi-layer stack of PMMA is used in favour of a single PMMA layer as it creates an undercut in the resist after exposure and development. The LMW PMMA is

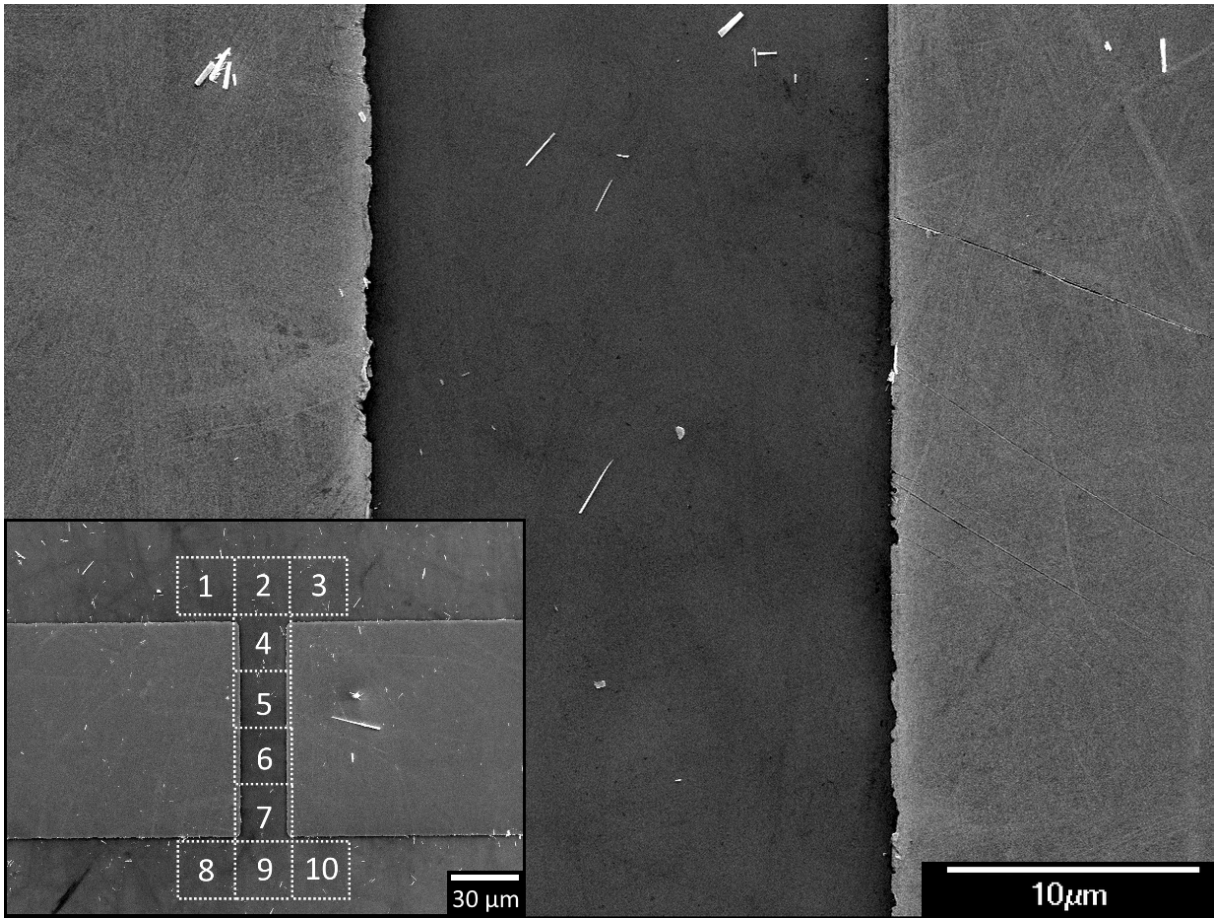

Figure A.2: An SEM image taken between a pair of electrodes from a device substrate. Nanowires are clearly visible, and can be located later on by comparing their position with a point on the electrode edge. Inset: A map showing a pair of electrodes separated into 25×25 μm areas, which must be individually imaged to completely map the electrode pair.

more susceptible to e-beam exposure, and a comparatively larger portion is exposed compared to the HMW layer. When the exposed portions of the HMW and LMW layers are removed through development, the LMW layer slightly undercuts the HMW layer, as shown schematically in Figure A.3. After the samples are eventually metallised, the LMW undercut significantly improves the liftoff, as the deposited metal is not in contact with the sidewall of the LMW PMMA. This is critical for high-resolution lithography with small patterned features. The height of the bi-layer is typically 300 nm thick, which has been measured using a Veeco Dektak 150 profilometer.

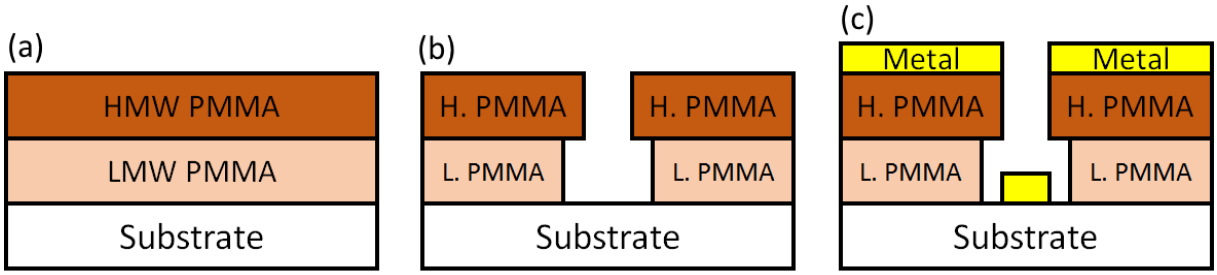

Figure A.3: (a) The PMMA bi-layer prior to exposure. (b) After exposure and development, the LMW layer undercuts the HMW layer. (c) Liftoff is made easier after metallisation as the metal on the sample doesn't touch the PMMA sidewall.

After the device substrates have spun with PMMA, the nanowires are ready to be contacted via EBL. The bulk of the single nanowire devices in this thesis were contacted using the Raith 150 at the University of Canterbury. The Raith 150 doubles as an SEM and as an EBL system. Samples are attached to the EBL chuck by a hinged clip in the loadlock. After the loading procedure, a robot arm moves the chuck into the EBL chamber. The chuck is positioned within the chamber using a joystick, and an internal infrared camera is used to gauge the position of the sample. All of the EBL work using the Raith 150 was carried out with an accelerating voltage of 10 kV and an aperture size of 10 μm. It should be noted that there are several steps taken to ensure the alignment of the electron beam is correct, along with measurements of the beam current. The description of these steps is omitted for brevity.

Imaging the device substrates during EBL poses an obvious problem. Other than the use of the infrared camera, the only way to image the substrates is using the Raith 150 as an SEM. However, this unintentionally exposes vast areas of the PMMA to the electron beam, meaning the portions of the PMMA imaged via SEM will be dissolved during development. Therefore most of the EBL work is done semi-blind, with the electron beam blanked for most of the time. To do this, the sample is first positioned slightly outside of the SEM column using the joystick controller and

infrared camera. Once the sample is just out of view of the column, the beamline is unblanked and the corner of the substrate brought into the field of view. Once the corner of the substrate can be seen, the chuck is rapidly moved so that the beam traverses to the edge of the cross-bar. While this does expose the PMMA between the substrate corner and the cross-bar, the nanowires and electrode gaps are far in the centre of the substrate, ensuring they aren't accidentally exposed to the electron beam. This procedure is shown schematically in Figure A.4.

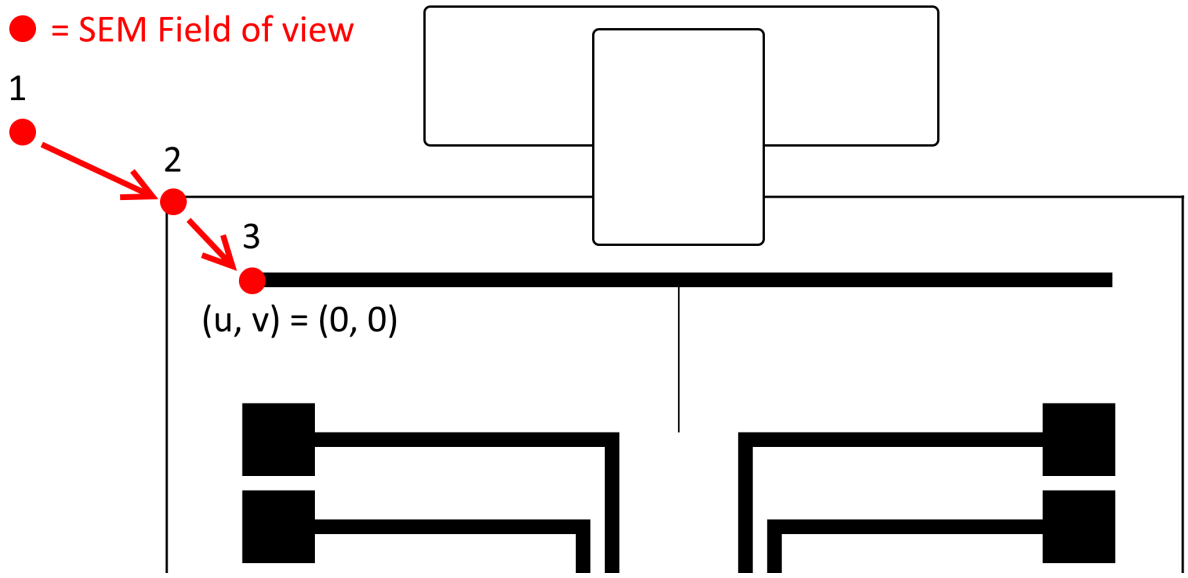

Figure A.4: A schematic showing the $(u, v) = (0, 0)$ origin definition. The SEM field of view (red dot) starts (1) outside of the sample, before (2) moving to the corner of the sample, and from there moving (3) to the edge of the cross-bar, where the (u, v) origin is defined.

The Raith 150 uses a set of coordinates, (u, v), that are separate from the lab coordinates (x, y). The (u, v) coordinate system allows for navigation of the device substrate without directly imaging the sample using SEM. First, a $(u, v) = (0, 0)$ origin is established at the edge of the cross-bar on the substrate. The (u, v) coordinate system is initially parallel to the (x, y) coordinate system, and usually needs to be rotated to account for the angle θ between the two coordinate systems. Two points on the cross-bar(P1 and P2) are used to define the u axis, and the (u, v) coordinate system is then rotated by θ, schematically shown in Figure A.5. This aligns the (u, v) coordinate system with the layout of the chip.

Once a suitable (u, v) = (0, 0) origin has been established and the coordinate system has been rotated, the sample can be navigated by moving the chuck using stepper motors. These stepper motors allow movement in both the u or v directions while the electron beam is blanked. If the $(u, v) = (0, 0)$ origin is a known point on

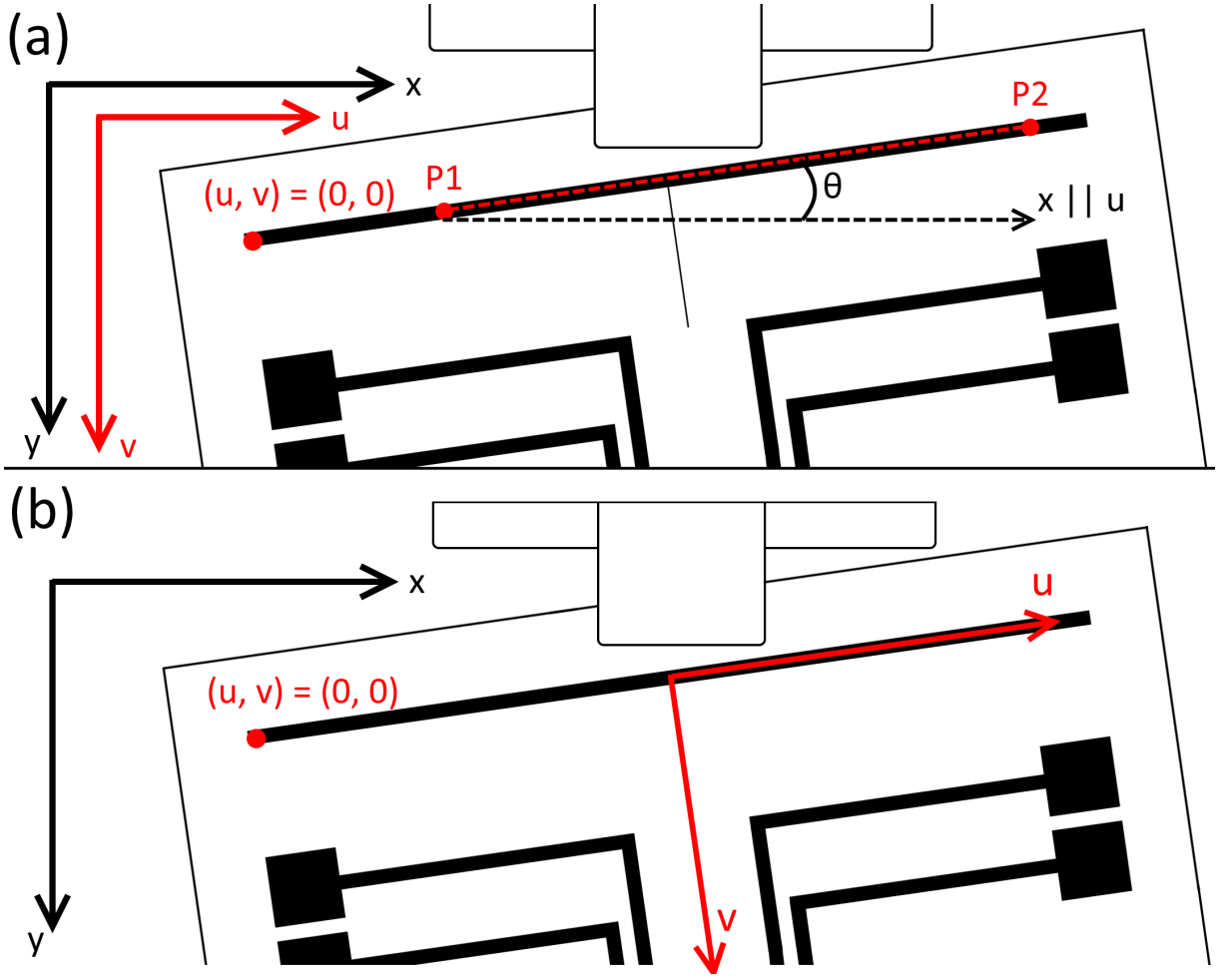

Figure A.5: A schematic showing the angle correction of the u axis. The (u, v) and (x, y) axes are initially parallel, but as the sample is usually loaded at an angle, the axis needs to be slightly rotated. Two points P1 and P2, shown in (a), are chosen from the cross-bar, which is used to define the u axis. After the coordinate system has been rotated by θ, it is aligned with the substrate, which makes navigation of the sample easier.

the photolithographically-defined Ti/Au pattern, and the photolithographic pattern is known, the electrode gaps can be reliably navigated to without exposing the sample to the electron beam. This process is shown in Figure A.6.

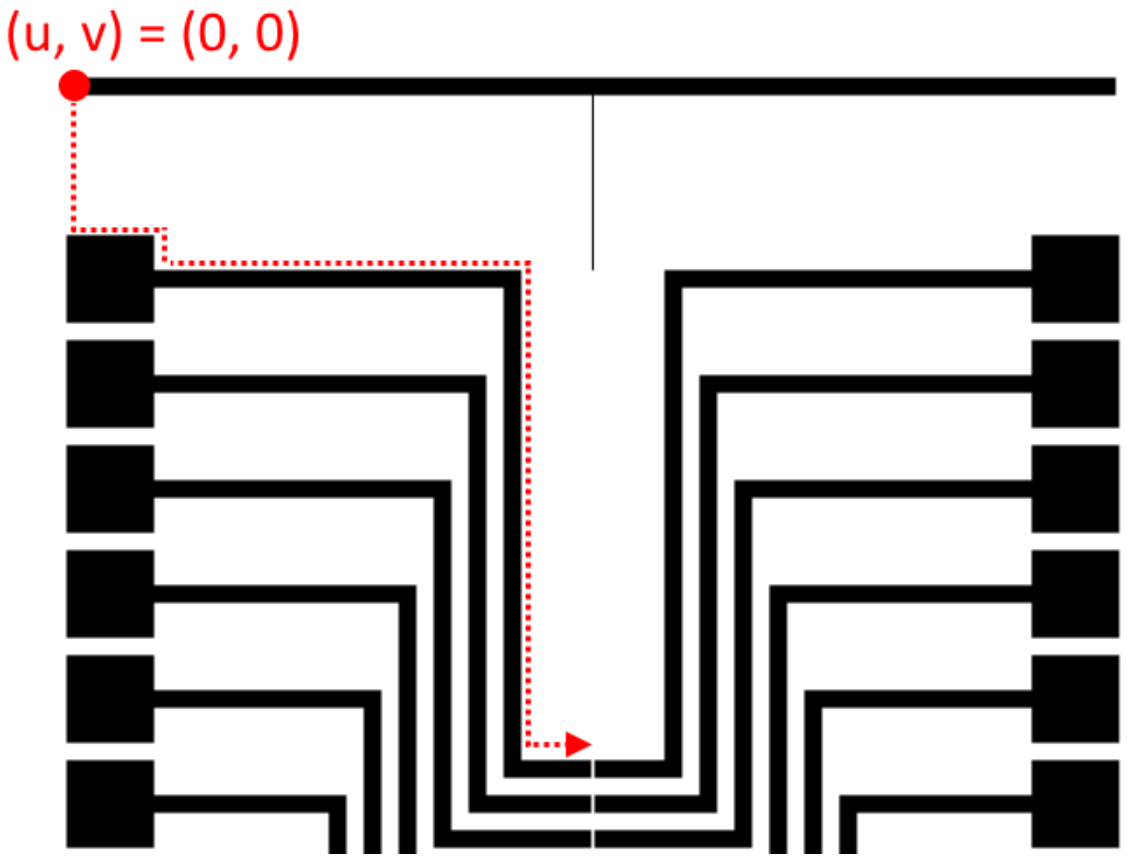

Figure A.6: The path taken from the (u, v) origin to the first writefield via stepper motors is shown by the red line. This ensures the PMMA remains unexposed to the electron beam.

When the electrode gaps are underneath the SEM column, the actual EBL process can begin. A snapshot of the sample is acquired with a "slowscan", which is a low-resolution SEM image captured in a single raster. The dimensions of the slowscan are determined by the size of the writefield (WF), which is the maximum area the Raith 150 can pattern for a fixed stage position. We consistently use a writefield size of 25 $\times$ 25 microns for all of the EBL performed using the Raith 150. Although the slowscan does expose the entire writefield to the electron beam, the exposure from a single slowscan isn't significant enough to affect the PMMA. However, if 3 or 4 consecutive slowscans are taken of the same writefield, the PMMA will be exposed and removed during the development process.

The majority of the nanowires underneath the PMMA are unable to be seen in the slowscan image. This is why SEM images of the nanowires are taken before the

PMMA bi-layer is applied. Figure A.7 shows an SEM image of part of a channel, taken before the sample has been spincoated with PMMA, and a slowscan of the same area. The nanowire to be contacted is highlighted with a dotted box, and shown in higher magnification in the upper-right inset. While this nanowire is invisible underneath the PMMA, a few large nanowires can be seen in both SEM and slowscan images. These large nanowires (numbered 1, 2, and 3) are used as common reference points to triangulate the position of the nanowire to be contacted in the slowscan image. This is most easily done by measuring the distance of the nanowire ends from the reference points in the SEM image using ImageJ, which is a free piece of software designed for scientific micrograph analysis.

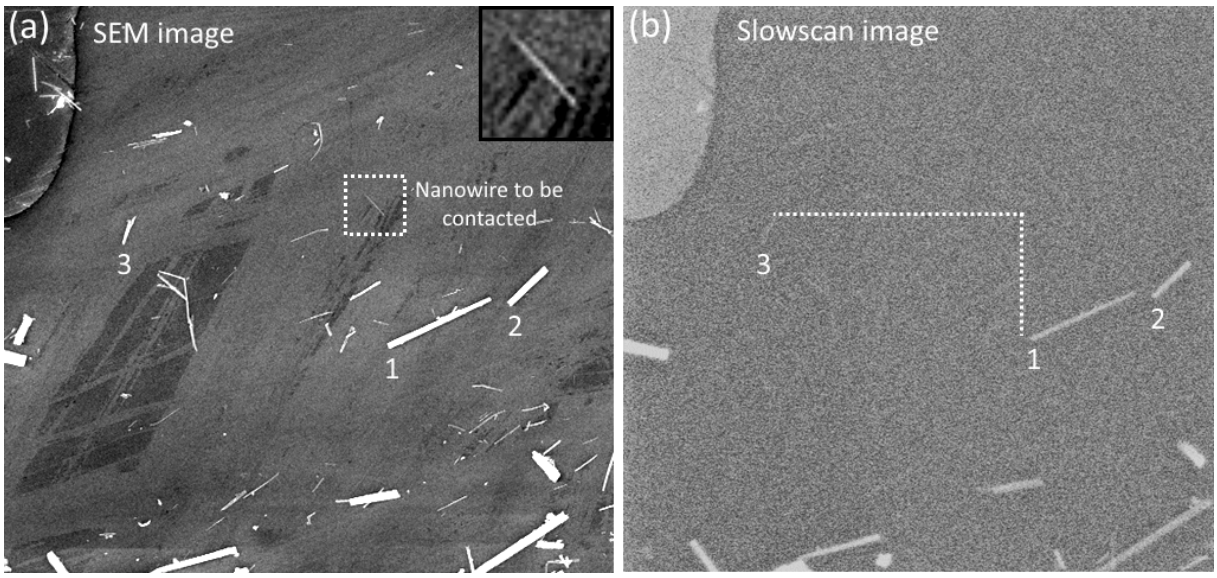

Figure A.7: (a) An SEM image of nanowires deposited on a channel, before PMMA has been spincoated. A box highlights the nanowire to be contacted, which is shown in the upper-right inset. (b) A corresponding slowscan image of the same location. Large nanowires (labelled 1, 2, and 3 in both images) can be used to triangulate the position of the nanowire.

Once the nanowire can be reliably located in the slowscan image, the EBL pattern is designed by dictating which portions of the writefield are to be exposed using the GDS editor, which is part of the Raith 150 software. These designs are superimposed over the slowscan image. The pattern is positioned in relation to the reference points (measured from the SEM images) by comparing the distance between points on the slowscan image using the coordinate system. To make this process easier, the Raith 150 introduces a third set of coordinates (U, V) local to the writefield, with the centre of the writefield designated $(U, V) = (0, 0)$. Figure A.8 shows the pattern designed in the GDS editor and its overlay with the slowscan image.

After the pattern has been designed and positioned accordingly, the Raith 150

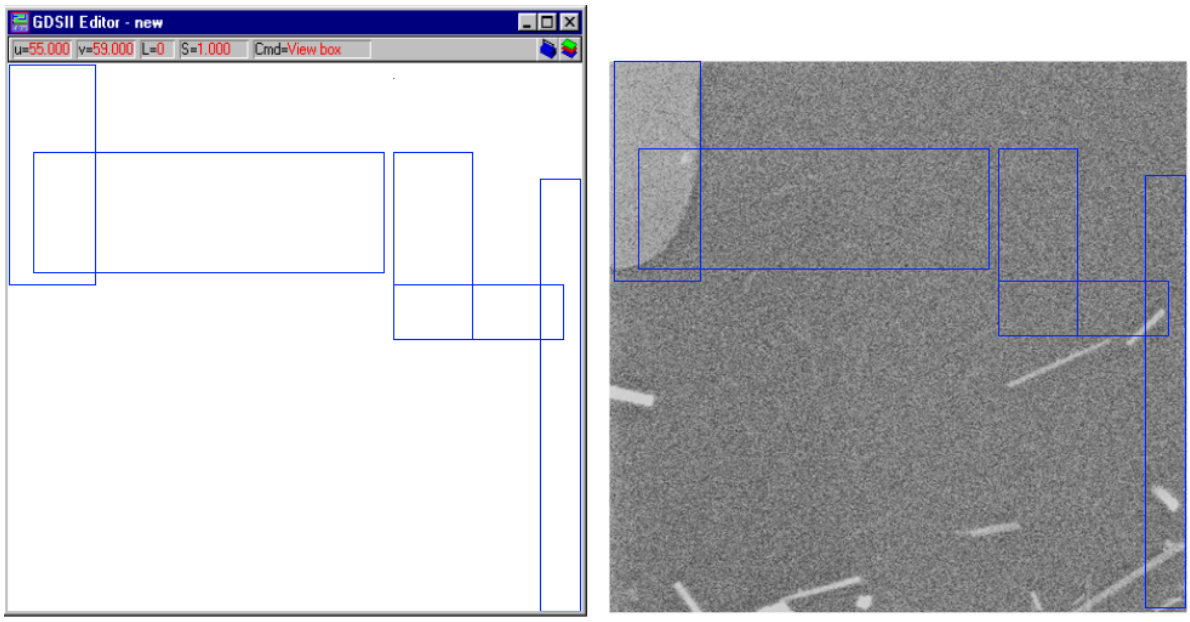

Figure A.8: The GDS editor (left), used to design custom patterns, and the slowscan overlay (right) relating the pattern to the writefield.

relates the (U, V) coordinate system back to the lab (x, y) coordinate system and the writefield is finally exposed. It is often necessary to connect the exposed regions of the nanowire/writefield with the large photolithographically defined electrodes, which is typically more than a writefield's distance away. The stepper motor is moved 20 microns towards the electrode, and a new slowscan image is taken. Because the size of the writefield is 25 microns, the new and old writefields partially overlap. A large square (usually 22 $\times$ 22 microns) is written in the new writefield, which connects the initial patterns. This process is repeated until the electrode is thoroughly exposed, and then the stage is stepped an equal number of times in the opposite direction to return it back to the initial writefield. The process is then repeated in the opposite direction until the second electrode has been exposed, ensuring that the EBL-exposed portions of the PMMA will connect to both electrodes.

This process is schematically shown in Figure A.9. The nanowire contact design is shown in blue. The stepper motor has moved 20 μm to the right, and the edge of the new writefield is shown by the black dotted line that runs vertically down the centre of the figure. The 22 $\times$ 22 μm square is shown by the yellow dotted box in the new writefield. The part where the two writefields overlap is shown by the blue diagonally-shaded area.

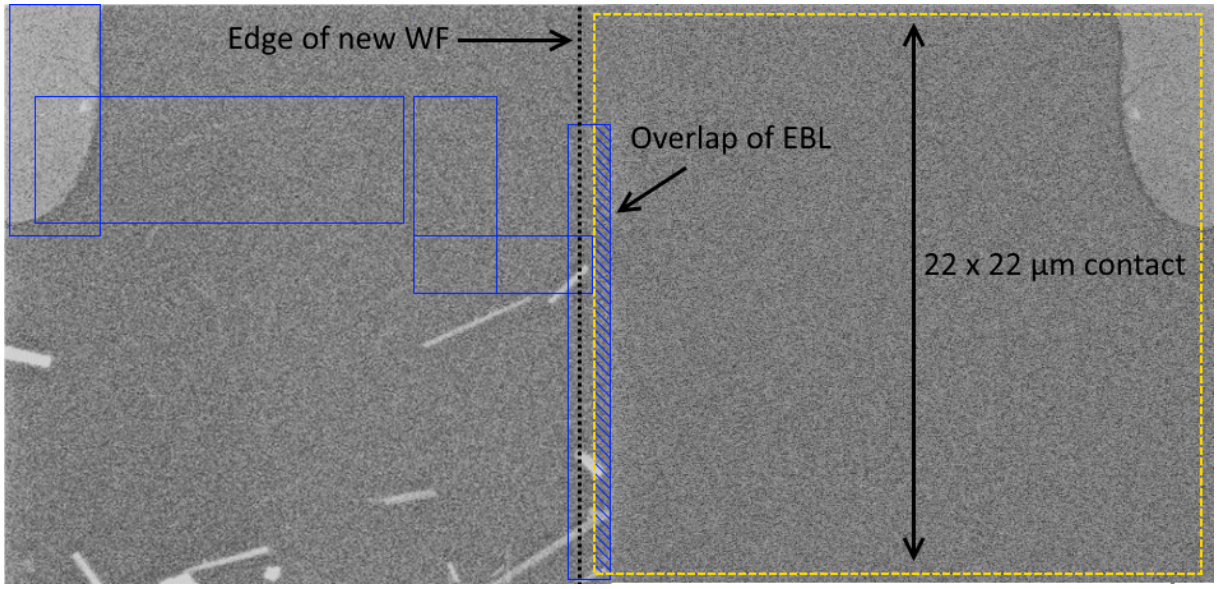

Figure A.9: Overlapping writefields to create a continuous exposure using the GDS editor.

A.1.4 Development and metal deposition

Once the samples have been patterned, the exposed PMMA is dissolved through a development step, akin to photolithographic development. Samples are gently agitated in a 1:3 mixture of methyl isobutyl ketone (MIBK):IPA for 40 seconds, which is a very common developer used in conjunction with PMMA throughout the literature. After the samples have been developed, they are rinsed in pure IPA to remove any residue.

Although the nanowires are very small, the EBL results can usually be assessed using optical microscopy, provided that the PMMA channel isn't too thin to resolve. Figure A.10 shows an optical microscope image of a sample after development. The photolithographically defined electrodes (referred to as the PL electrodes) can be seen in the top-right and bottom-left of the image. The bulk of the electrodes are still underneath the PMMA, although windows have been opened on each electrode through EBL and development. The channel between the two PL electrodes runs diagonally through the centre of the image. This too is underneath PMMA, although leads have been defined through EBL to make contact to the nanowire. The nanowire itself is highlighted by the dashed black box, and is shown in high-contrast in the upper-right corner of the image. Although this image has been taken with an optical microscope, the two individual ends of the nanowire can be seen, as well as the PMMA channel separating the nanowire contacts. The PMMA channel is particularly large in this image, and can be much more difficult to resolve if the nanowire contacts are spaced closer together.

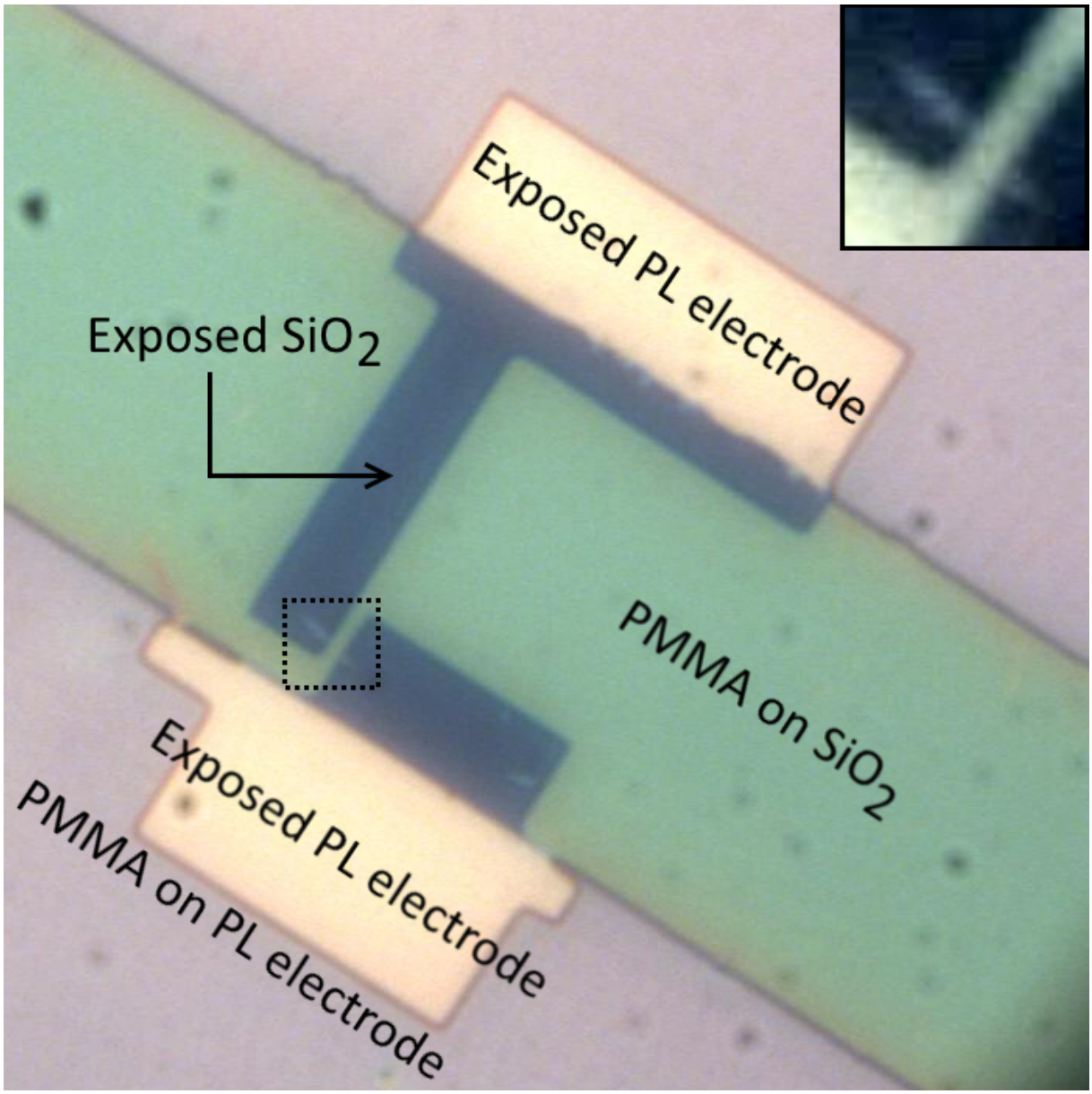

Figure A.10: Optical image of an EBL sample post-development.

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