

High Impedance Amplifiers for Non-Contact Bio-Potential Sensing

by

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Abstract

This research develops a non-contact bio-potential sensor which can quickly respond to input transient events, is insensitive to mechanical disturbances, and operates with a bandwidth from 0.04 Hz – 20 kHz, with input voltage noise spectral density of $200\text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz.

Initial investigations focused on the development of an active biasing scheme to control the sensors input impedance in response to input transient events. This scheme was found to significantly reduce the settling time of the sensor; however the input impedance was degraded, and the device was sensitive to distance fluctuations. Further research was undertaken, and a circuit developed to preserve fast settling times, whilst decreasing the sensitivity to distance fluctuations.

A novel amplifier biasing network was developed using a pair of junction field effect transistors (JFETs), which actively compensates for DC and low frequency interference, whilst maintaining high impedance at signal frequencies. This biasing network significantly reduces the settling time, allowing bio-potentials to be measured quickly after sensor application, and speeding up recovery when the sensor is in saturation.

Further work focused on reducing the sensitivity to mechanical disturbances even further. A positive feedback path with low phase error was introduced to reduce the effective input capacitance of the sensor. Tuning of the positive feedback loop gain was achieved with coarse and fine control potentiometers, allowing very precise gains to be achieved. The sensor was found to be insensitive to distance fluctuations of up to 0.5 mm at 1 Hz, and up to 2 mm at 5 kHz.

As a complement to the non-contact sensor, an amplifier to measure differential bio-potentials was developed. This differential amplifier achieved a CMRR of greater than 100 dB up to 10 kHz. Precise fixed gains of 20 ± 0.02 dB, 40 ± 0.01 dB, 60 ± 0.03 dB, and 80 ± 0.3 dB were achieved, with input voltage noise density of $15 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz.

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Contents

1	Introduction	1
1.1	Motivation	1
1.2	Problem Definition	2
1.3	Research Goals	3
2	Background	5
2.1	Bioelectricity	5
2.2	History of Electrophysiology	5
2.3	Contact Sensors	8
2.4	Non-Contact Sensors	9
2.5	Operational Amplifier Imperfections	13
3	Laboratory Environment	17
3.1	Shielding, Guarding and Grounding	17
3.2	Shielded Test environment	33
4	Methodology	35
4.1	Input Capacitance Measurement	35
4.2	Input Bias Current Measurement	37
4.3	Transfer Function Measurements	41
4.4	Noise Measurements	45
4.5	Gain vs Distance Characterisation	47

5	Differential Amplification System	51
5.1	Requirements	51
5.2	Design and Evaluation	54
5.2.1	System Overview	54
5.2.2	Instrumentation Amplifier	55
5.2.3	Anti-Aliasing Filters	61
5.2.4	High Gain Amplifier	64
5.2.5	Power Supply	70
5.2.6	Enclosure Design and System Integration	73
6	Sensor Design	77
6.1	Overview	77
6.2	Amplifier Design	79
6.3	Electrode Design	83
6.4	High Impedance Biasing	87
6.5	Input Capacitance Neutralisation	106
6.6	Integration	110
7	Sensor Evaluation	117
7.1	PCB Leakage	117
7.2	Frequency Response	117
7.3	Gain vs Distance	120
7.4	Input Impedance Estimation	122
7.5	Settling Time	123
7.6	Noise Measurement	125
7.7	ECG Recording	126
8	Conclusion and Recommendations for Extension	129
8.1	Contributions	129
8.2	Conclusions	130
8.3	Limitations	132
8.4	Recommendations	132

<i>CONTENTS</i>	vii
A Spice Simulation for High Impedance Circuits	135
B Sensor Calibration	137
B.1 Laboratory Equipment	137
B.2 Method	137
B.3 Notes for future calibrators	140
C Circuit Diagrams and PCB layouts	141

Chapter 1

Introduction

This chapter presents the motivation for undertaking this research, and identifies the problems to be solved.

1.1 Motivation

Non-contact bio-potential sensors are poised to make a significant impact in the way electrophysiological signals are monitored and applied. Conventional contact bio-potential sensors require adhesive electrolyte gels, skin hydration, and in some cases, skin abrasion to obtain bio-potentials from patients (Spinelli and Haberman, 2010). These methods are time consuming, and uncomfortable, but they do result in high fidelity bio-potential signals, and as such are the standard for electrophysiological diagnosis (Chi et al., 2010a). Problems occur with these sensors when long term monitoring is required. The electrolyte gel causes skin irritation, and dries out over time, necessitating regular reapplication (Sullivan et al., 2007). The use of electrolyte gels also limits the spatial density achievable with these sensors. If electrodes are too close together the gel, which is conductive, can short circuit between the electrodes, degrading the spatial accuracy (Sullivan et al., 2007).

Non-contact sensors allow bio-potentials to be obtained without making direct contact to the body, and require no prior preparation of the skin, nor the use

of electrolyte gels. This allows these sensors to be quickly and comfortably applied to the body, enabling portable electrophysiological monitoring systems to be developed for emergency services, long term monitoring for diagnosis, and personal health monitoring. The absence of electrolyte gels allows non-contact sensors to be applied in higher density than contact electrodes, allowing bio-potential recording with higher spatial resolution (Clippingdale et al., 1994). These non-contact sensor systems will increase electrophysiological information available to emergency services, health professionals, and anyone interested in their own physiology. This increase in information could provide a deeper understanding of the human bio-electric system, uncovering early signs of disease, and the mechanisms of recovery.

Contact sensors can draw potentially harmful, real charge currents from the body (Harland et al., 2002). Non-contact sensors by contrast draw only a displacement current which flows through the source capacitance, making them intrinsically safe.

Non-contact sensors look set to widen the possible applications of bio-potential sensing. Non-contact sensors can be embedded into furniture, such as an operating table or chair (Lim et al., 2007, 2006), or incorporated into clothing (Chi et al., 2010b) to allow comfortable, long term electrophysiological monitoring. The higher spatial resolution achievable allows high density application of bio-potential sensors (Chi et al., 2009). This increased density could be used to sense, and image the electric potential of the entire body, providing an excellent tool for medical diagnosis.

1.2 Problem Definition

Non-contact bio-potential sensing has been in development since the late 60s. Since then problems with bio-compatibility (Lagow et al., 1971), high source impedances (Clippingdale et al., 1994), noise (Chi et al., 2011b), and sensitiv-

ity to motion (Chi and Cauwenberghs, 2009) have largely been solved. The first commercially available sensor was released in 2011 by Plessey Semiconductors (Plessey Semiconductors, 2011), but this technology still presents problems that remain to be solved.

The ultra high input impedances of non-contact sensors ($> 1 \text{ T}\Omega$) make these devices highly susceptible to electrical interference. In fact this is entirely the point of these sensors; to be sensitive to the small potentials associated with biological signals. The problem with this high susceptibility is that potentials much larger than those originating from biological systems are present in the environment. The low voltage circuits used for non-contact sensors are at high risk of saturation from the influence of these interference potentials. Time constants in the 10s of seconds are produced due to the capacitive source impedance (typically 10 pF), and ultra high input impedances ($> 1 \text{ T}\Omega$) of non-contact sensors. This means when the sensor is subject to an input transient that causes saturation, the bio-potential signal will be lost for an unacceptably long period of time.

This research aims to apply well defined techniques to create a sensor capable of measuring bio-potentials from the surface of the body, without making direct contact. Furthermore it aims to address the unsolved (as far as the author is aware) problem with such sensors of extremely long settling times, in order to create a device which is more robust to low frequency electrical interference. In addition to developing the bio-potential sensor, a differential amplifier to acquire bio-potential measurements will be developed. These points are summarised in the research goals below.

1.3 Research Goals

- Design and build a wide bandwidth ($0.1 \text{ Hz} - 20 \text{ kHz}$) non-contact sensor
- Develop original methods to reduce the settling time of non-contact sensors

- Build a system to acquire differential bio-potential signals

Chapter 2

Background

2.1 Bioelectricity

2.2 History of Electrophysiology

This section outlines the history of electro-physiology; from early research into the nature of electricity to the instrumentation which enabled characterisation of bio-electric systems and medical diagnosis. This history shows how the development of measurement equipment is inseparable from the advancement of electro-physiological knowledge.

In the mid 18th century the nature of electricity was being investigated. Natural electricity was known as lightning, and artificial electricity was generated by electrostatic generators. Around the same time there were peculiar tales from Dutch South America of an eel which produced a shock likened to that from an electrostatic generator, could this be an animal electricity? (Finger and Piccolino, 2011) By 1772 samples of these eels had made their way to Europe where fellow of the royal society, John Walsh performed demonstrations to royal society members. He passed the force from the eel through a chain of people so they could feel the shock. These demonstrations gained popularity for the idea that the shock

was of an electrical nature (Piccolino and Bresadola, 2002).

In 1791 Luigi Galvani published his experiments creating contractions in dissected frog legs. Galvani connected the frog's sciatic nerve to muscles and observed the legs twitching (Piccolino, 1998). Galvani proposed that there is an intrinsic electricity to animals, identifying the brain and nerves as the distributors of the electricity and the muscles as the receivers (Hoff, 1936). Galvani's conclusions were refuted by Alessandro Volta, who claimed the electrical activity observed came from the contact of two dissimilar metals. This principle would lead Volta to develop the voltaic pile (Piccolino, 1998). Galvani recreated his experiments connecting nerve and muscle using moistened paper instead of metal, however Volta still refuted his findings, stating there is still heterogeneous matter involved which would create weak electric effects (Moruzzi, 1996).

The success of the voltaic pile gave Volta celebrity status, which seemed to sway popular opinion. Galvani's ideas were passed off as mystifying pseudoscience, not a popular thing in the age of reason (Piccolino, 1998). In 1825 Leopoldo Nobili invented the astatic galvanometer, a device which used two coils in opposite directions to restore the indicating needle, as opposed to the earlier designs which used the earth's magnetic field as the restoring force (Bennett, 1999). This device was far more sensitive than previous instruments and Nobili used it to repeat Galvani's experiments. Nobili measured currents from the nerve to the muscle of a frog's leg; however interpreted them as originating from thermoelectric effects, ignoring the possibility that the current could originate from the biological system. This misinterpretation is a testament to the lasting effects of Volta's objections. It would take until 1842 with Carlo Matteucci's biological pile for bio-electricity to become an accepted phenomenon. Matteucci stacked cut sections of muscle and measured the potential difference across the stack, noticing that the more layers of muscle, the greater the potential (Moruzzi, 1996). Thanks to the development of more sensitive galvanometers, and the findings of Matteucci, progress in the field of electro-physiology accel-

erated. In 1848 Emil du Bois-Reymond detected the action potential of muscle contraction (Moruzzi, 1996), and in 1849 Herman Helmholtz measured the speed of nerve conduction (Bennett, 1999). The first cardiac potentials were measured by August Desire Waller in 1887. Waller used a sensitive current measuring device developed by Gabriel Lippman called the capillary electrometer; a thin glass cylinder with two layers of mercury separated by dilute sulfuric acid. Wires connected to the mercury layers were used to sense electric current, with the height of the mercury responding to the intensity of the current (Fisch, 2000). In 1903 Willem Einthoven published his work on measuring cardiac signals, identifying the PQRST waves, introducing and advocating for the 3 lead ECG measurement as a diagnostic tool. Einthoven measured cardiac potentials using his device called the string galvanometer. The hands and feet of the subject were immersed in jars of saline solution which connected to the string galvanometer to measure the differential currents (Cajavilca and Varon, 2008). This device was the grandfather of modern ECG recording. Into the 1920s vacuum tube amplifiers were used by Herbert Gasser to measure and classify nerve fibers. Jan Toennies joined Gasser in the mid 1930s, where he built high impedance cathode follower amplifiers and differential amplifiers. These amplifiers were soon in laboratories all over the world, including that of Alan Hodgkin and Andrew Huxley who would improve on these amplifiers by developing unique operational amplifiers to measure the potentials of individual cells (Schoenfeld, 2002).

The high impedance amplifiers of Toennies, and the operational amplifiers of Hodgkin and Huxley were progressively shrunk in size, and cost, and their reliability improved, allowing their application in compact designs. These developments allowed electro-physiological measurements to become the ubiquitous diagnostic tools they are today.

2.3 Contact Sensors

This section gives an introduction to bio-potential sensing with the ubiquitous contact electrodes.

Bio-potentials originate from cell membranes separating potassium, sodium and to a lesser extend calcium ions, creating a potential difference between the inside and outside of the cells (Webster, 1999). This is known as the resting potential. Some cells are excitable, responding to electric stimulation they create what is known as an action potential (Webster, 1999). These action potentials are what is measured when bio-potential measurements are taken.

The bio-potentials which are measured in clinical electro-physiology are:

- Electrocardiography (ECG) - action potentials of the heart
- Electroencephalography (EEG) - action potentials of neurons
- Electromyography (EMG) - action potentials of the muscles
- Electrocochleography (ECochG) - action potentials of the auditory nerve

These bio-potentials are typically measured at the surface of the body, apart from the ECochG of which non-invasive measurement is still being developed (Masood et al., 2012).

The standard way of measuring bio-potentials from the surface of the body uses silver chloride (AgCl) electrodes, with a conductive gel containing sodium, potassium and chloride ions (Northrop, 2003). The AgCl electrodes and conductive electrolyte gel are used together as they form a fairly stable junction, or half cell potential minimising electro-chemical noise (Webster, 1999).

Whilst contact electrodes provide high quality electro-physiological measurements there are some non-ideal properties which limit their use in some applications. Chemical reactions at the skin-electrolyte boundary cause skin irritation

under prolonged use making them unsuitable for sustained periods of monitoring (Lagow et al., 1971). Furthermore the electrolyte gel that is used to increase conduction dries out over time, reducing the coupling from skin to electrode resulting in signal degradation (Northrop, 2003). Electro-chemical reactions also create voltages at the electrode plate referred to as half cell potentials. The half cell potential fluctuates depending on the elements present at the contact points adding noise to bio-potential measurements (Northrop, 2003). The use of conductive gels also limits the spatial resolution achievable with traditional electrodes as electrodes in close proximity can become short circuited through the gel (Prance et al., 2000). These problems can be overcome by using capacitive electrodes as they do not require conductive gels for skin to electrode coupling. This can result in reduced preparation time, higher spatial resolution, and (with inert insulating materials) lower skin irritation under long-term use. Furthermore if the potentials are measured without contact to the body, no half cell potentials will occur, and thus the intrinsic noise of the sensors will be lower than that of contact electrodes.

2.4 Non-Contact Sensors

This section introduces the bio-potential sensing devices which constitute the focus of this research. These sensors are referred to synonymously as capacitive, displacement current or electric potential sensors. Furthermore we can define two groups of capacitive sensor, *insulated sensors* where subject and electrode are in contact and *non-contact* where the subject and electrode are separated by some other medium. These sensors have found applications in non destructive testing, electrical circuit imaging, nuclear magnetic resonance and as is the focus of this work, in detecting electro-physiological signals (Beardsmore-Rust et al., 2009).

Capacitive bio-potential sensors were developed for long-term electrocardiographic monitoring of astronauts as these sensors do not require electrolytic gels thereby reducing the irritation of the skin under long-term use (Lopez and Richardson, 1969).

In a capacitive bio-potential sensor a high pass filter is formed with the coupling capacitance from skin to electrode and the input impedance of the amplifier. To obtain the low frequency response of electro-physiological signals (down to 0.1Hz) the pole formed by coupling capacitance and input impedance must be kept below the desired low frequency response. Because the input is capacitively coupled to the source a DC current path must be provided for the amplifier's bias current in order to maintain a stable operating point (Horowitz, 1989). The impedance of the bias current path adds in parallel with the input impedance of the amplifier, reducing the overall impedance seen at the input. Because of the difficulty in creating high impedance bias current paths early capacitive sensors focused on increasing the skin to electrode capacitance.

The early capacitive bio-potential sensors used high-permittivity materials for the insulating layer to increase the skin to electrode coupling. They also required direct contact with the skin as the capacitance is inversely proportionate with the skin to electrode distance.

The first successful capacitive bio-potential sensors used anodized aluminium electrodes connected to a junction field effect transistor (JFET) buffer with an input resistance of greater than $1\text{G}\Omega$. This configuration was able to produce high quality electrocardiograms with minimal distortion when compared to conventional electrodes (Lopez and Richardson, 1969). Anodized aluminium was found to be unsuitable for long-term use as the oxide layer was prone to breakdown over time. The porous aluminium oxide absorbed sweat which is high in NaCl and the chloride ions reacted with the aluminium to breakdown the insulation. An improved dielectric resistant to chloride was developed using anodized tantalum. The electrodes were soaked in NaCl solution for 3 days and no deterioration in performance was observed (Lagow et al., 1971).

Further relaxation of input impedance requirements was achieved using ultra

high-permittivity barium titanate ceramic electrodes resulting in coupling capacitances of hundreds of nanofarads (Matsuo et al., 1973). This relaxed the input impedance requirement for acquiring electro-physiological frequency signals to a mere $20\text{M}\Omega$.

The intrinsic noise of an electrode results from the electro-chemical interaction of the electrode and an electrolyte. In the insulated sensor case, sweat is the electrolyte and noise is generated from the interaction with the dielectric. The noise voltage of the electrode when immersed in an electrolytic solution was shown to be lower than a silver electrode confirming the stability of the barium titanate dielectric. However the barium titanate ceramic was seen to exhibit piezoelectric effects under mechanical stress, generating large noise voltages. Thus the practicality of ultra-high permittivity sensors is limited to low vibration applications (Matsuo et al., 1973).

One of the claimed benefits of these early capacitive sensors was the reduction of motion artifacts caused by patient movements during monitoring (Grishanovich and Yarmolinskii, 1984). This claim is only valid when the skin and electrode are in perfect contact as any change in electrode to skin distance modulates the coupling capacitance, which alters the response of the amplifier.

Due to electronic amplifier limitations early capacitive bio-potential sensor design focused on using chemically stable high-permittivity insulation to increase capacitive coupling from subject to electrode rather than increase the input impedance of the amplifier. Despite the demonstration of the benefits of capacitive bio-potential sensors; lower intrinsic noise, no polarizing potentials (Matsuo et al., 1973), reduced skin irritation (Lagow et al., 1971), and reduced motion artifacts (Grishanovich and Yarmolinskii, 1984) they failed to obtain widespread use. One reason cited for this was the manufacturing difficulties in producing high quality dielectric layers on electrodes (Grishanovich and Yarmolinskii, 1984). Furthermore these sensors were large due to semiconductor process limitations, costly,

and despite claims to the contrary, prone to motion artifacts due to imperfect skin electrode contact (Alizadeh-Taheri et al., 1996). Regardless of the reasons research into capacitive bio-potential sensors was sparse until a resurgence of interest in the 1990s.

Improvements in semiconductor manufacturing which enabled ultra high impedance devices to be implemented in small packages has driven the development of non-contact sensors since the early 1990s. Clippingdale et al. (1994) were able to develop stable capacitively coupled amplifiers with input resistance as high as $10^{16}\Omega$ and input capacitance as low as 10^{-17}F . This relaxed the high coupling capacitance requirement of earlier designs, enabling electrocardiographic signals to be obtained without contact to the body. It also removed the need for ultra high permittivity materials for electrode insulation, allowing standard micro-fabrication insulating techniques to be used such as silicon dioxide and silicon nitride. Electrode and amplifier could now be fabricated together reducing the size of the sensors. This allowed EEG recording to be performed with greater spatial resolution than previous contact electrode based systems (Alizadeh-Taheri et al., 1996).

The introduction of ultra high impedance inputs and lower coupling capacitances introduced a new set of problems to be solved. The high impedance increases susceptibility to electromagnetic interference, both external to and on the circuit board. The smaller coupling capacitances form a capacitive voltage divider with the sensor input capacitance attenuating the signal at the input. Furthermore, if the coupling capacitance varies, this attenuation varies, and mechanical vibrations are seen as electrical signals.

Prance et al. (2000) improved their previous design Clippingdale et al. (1994) by using the INA116 instrumentation amplifier, giving a lower noise sensor, and reportedly a stable output without any input biasing circuitry. The conditions for testing this device are not given, and it is assumed that tests were conducted in a well shielded environment. In a real world environment DC and low frequency

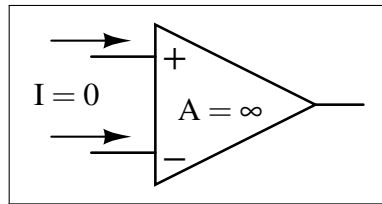


Figure 2.1: Ideal Op-amp

electric fields would cause the sensor to drift away from the bias voltage, possibly causing the amplifier to saturate.

The basic design for non-contact sensors has not changed since (Prance et al., 2000), with further progress being made in reducing the noise of these sensors (Chi et al., 2011a), and creating applications for these sensors (Lim et al., 2007, 2006). Further coverage of the state of the art in non-contact sensors will be given with reference to the sensor design in Chapter 6.

2.5 Operational Amplifier Imperfections

This section discusses the imperfections associated with operational amplifier (op-amp) circuits. The focus will be on imperfections which are relevant to this work, and the situations where errors due to these imperfections may occur. Circuit analysis rules for an ideal op-amp are given, providing a starting point to discuss deviations from the ideal model. The imperfections covered are; gain and bandwidth, input bias currents, common mode rejection, and input impedance.

2.5.1 The Ideal Op-Amp

In (Horowitz, 1989) two golden rules for analysis of op-amp circuits with negative feedback are given:

1. The output will try to maintain zero volts across the inputs

2. The inputs draw no current

Rule 1 is equivalent to assuming that the op-amp open loop voltage gain is infinite. Rule 2 implies that the input impedance of the op-amp is infinite. In reality neither of these conditions can be true, but in most situations the errors produced by following these rules are minimal, and circuit analysis is greatly simplified. The following sections will describe situations where following these rules will result in unacceptable errors.

2.5.2 Gain and Bandwidth

Operational amplifiers are often bandwidth limited to ensure their stability. This bandwidth limiting is referred to as dominant pole compensation, and is achieved by introducing a pole in the response to reduce the gain of the op amp at higher frequencies. As the closed loop gain of the op amp is increased, the bandwidth of a compensated op amp will decrease. For this reason the amplifier bandwidth is referred to as the gain-bandwidth product (GBW). The GBW is approximately constant, so that for a given closed loop gain the bandwidth of the op amp can be calculated. The bandwidth restrictions of op amps should always be considered with respect to the desired circuit bandwidth, particularly in high frequency, high gain, or precision circuits. Higher bandwidth op amps should be used with care as with increased bandwidth thermal noise effects can become large.

2.5.3 Input Bias Current

The input stage of an op amp consists of a differential amplifier. This amplifier requires some current and voltage in order to operate in a predictable way (Putten, 1996). Bipolar junction transistor (BJT) inputs require a bias current to flow at the input of approximately 100 nA (Sedra and Smith, 2004). FET input op amps, theoretically require no input current to operate. In practice leakage currents are unavoidable and these currents make up the input bias current of a FET amplifier (of the order of pA's). In addition to the input leakages of FET amplifiers, input protection circuits are often used with these amplifiers, which add further leakages

at the input.

The input bias current will flow through the source impedance, causing a voltage drop across this impedance. If source impedances are high, this voltage will cause a significant measurement error. Furthermore if the source impedance is capacitive the DC bias current can not flow through the source impedance, instead it charges the input of the amplifier, eventually resulting in amplifier saturation.

Amplifier input bias current should be considered where ever large source impedances are unavoidable, and particularly when capacitive sources are used. FET amplifiers typically have lower bias currents than BJTs. However the bias current of a FET rises dramatically with temperature, such that at high temperatures, a BJT may produce lower input bias currents.

2.5.4 Common Mode Rejection

The common mode rejection (CMR) describes the ability of the amplifier to reject signals which are common to both inputs. CMR is usually quoted as the common mode rejection ratio (CMRR). The CMRR is a comparison of the common mode gain to the differential gain, expressed in decibels and given by:

$$\text{CMRR} = 10\log_{10} \left(\frac{A_d}{A_{cm}} \right)^2$$

Where A_d = differential gain, and A_{cm} = common mode gain.

Ideally the common mode gain will be zero, resulting in an infinite CMRR. This condition requires the input transistors to perfectly cancel common mode signals. In reality the input transistors will not be perfectly matched, and so a common mode signal will be transformed into a differential signal (Sedra and Smith, 2004). In addition to the intrinsic CMRR of the op amp, external impedances will further reduce the CMR. The common mode voltage is transferred to an interference voltage at the output of the differential amplifier according to the following equation:

$$v_{int} = V_{cm} \left(\frac{1}{\text{CMRR}} + \frac{Z_d}{Z_c} \right) \quad (2.1)$$

Where v_{int} = interference voltage at the output, V_{cm} = common mode voltage at the input, $\text{CMRR} = \frac{A_d}{A_{cm}}$, Z_d = difference between source impedances, Z_c = common mode input impedance of the amplifier (Winter and Webster, 1983).

The common mode rejection needs to be considered where ever signals are in the presence of large interference signals.

2.5.5 Input Impedance

2 stated that the inputs to an op amp draw no current. This implies that the input impedance of the op amp is infinite, which is far from the case. The source impedance and the input impedance form a voltage divider circuit. If high source impedances are necessary, the input impedance is required to be at least 100 times as large as the source impedance for an error less than 1%. A BJT is a current controlled device, and as such is inherently low impedance. Electronic feedback techniques can be used to increase the input impedance of BJT amplifiers from $k\Omega$ s to $M\Omega$ s, however this only allows for source impedances in the $k\Omega$ s. FET amplifiers have much higher input impedances, and using the same feedback techniques can be made to produce input impedances greater than $1\text{ T}\Omega$.

Whenever high source impedance is required, the input impedance of the amplifier is a critical parameter. If source impedances are higher than a few $k\Omega$ s, or very precise measurements are required, FET input amplifiers should be considered.

Chapter 3

Laboratory Environment

This chapter presents background theory on techniques to mitigate electromagnetic interference, and presents the design of the shielded enclosure used for all circuit testing in this work.

3.1 Shielding, Guarding and Grounding

Electric and magnetic fields are a ubiquitous feature of life on Earth. Natural and manmade sources contribute to a complex field spanning the entire frequency spectrum. Human bio-potentials range in amplitude from $< 1\mu\text{V}$ for ECoG (Masood et al., 2012) to $> 10\text{mV}$ for EMG (Webster, 1999), and span frequencies from DC for EOG to 4kHz (Poch-Broto et al., 2009) and higher for ECoG. A device which is sensitive enough to measure these bio-potentials is also sensitive to other electric potentials such as; the mains power supply, 50Hz and harmonics; digital electronics, a wide range of frequencies dependant on slope of pulses; power switching transients such as room lighting or appliances, pulses containing a wide range of frequencies; and moving electrostatic potentials such as static build up on patients, generally low frequency (Putten, 1996). In order to measure electronic characteristics of such sensitive devices it is necessary to create a controlled environment to minimise the introduction of electromagnetic interference

(EMI).

This section introduces shielding, guarding and grounding techniques for the reduction of EMI. Some background theory will be given on these topics, giving general guidelines for their implementation.

3.1.1 Grounding

This section covers grounding techniques for minimising interference in electrical systems; presenting the definition of an ideal ground, and the practical limitations. These limitations will be used to inform optimal grounding schemes for reducing interference in electrical systems. Further discussion of ground current paths illuminate best practices for grounding Printed Circuit Boards (PCBs).

An electrical circuit requires a source of potential difference (battery or power supply), and connections from the higher potential to the lower potential through components to complete the circuit. The lower potential point is often referred to as ground. Ground is defined as a point or plane which provides a reference potential for an electrical circuit or system (Ott, 1988). In an ideal ground, the assumption is that all points connected to ground are at the same potential. This definition deemphasizes the fact that ground is part of the circuit, carrying current. As ground connections are made from conductors with some non-zero impedance, a drop in potential will occur across the ground system. This is often called an IR drop in reference to ohms law ($V = IR$) referring to the origin of the potential drop due to current flowing through a resistance.

Grounding Schemes

Figure 3.1 shows a series grounding scheme where the reference points of two circuits are connected to different points on the same ground conductor. In an ideal ground R_1 and R_2 will be zero and points A and B will be at ground potential. In reality, there is some non-zero impedance and so points A and B will not be at

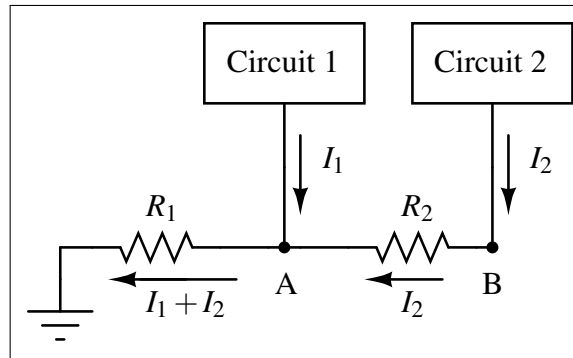


Figure 3.1: Series Ground System

the same potential. Taking ground to be 0V and using Kirchhoff's laws we can show that the potentials at A and B are:

$$A = R_1(I_1 + I_2) \quad (3.1)$$

$$B = A + R_2 I_2 \quad (3.2)$$

(3.1) and (3.2) show that the circuits see different reference potentials, and that these potentials are a function of the current and resistance in the ground conductor. If circuit 1 is an amplifier with a small input signal, and circuit 2 is a high current motor driver circuit, the current I_2 will cause disastrous interference in circuit 1. This interference can be eliminated by separating the ground connections so that each circuit returns to ground through a separate conductor.

This system, called a parallel ground or star ground, is shown in figure 3.2. Each circuit's reference potential is now only dependant on its own ground current and the impedance of the ground conductor. This scheme allows circuits with higher ground currents to be used alongside sensitive circuits without causing interference. This scheme is preferable when ground current frequencies are low; at higher frequencies the longer ground connections can radiate electromagnetic

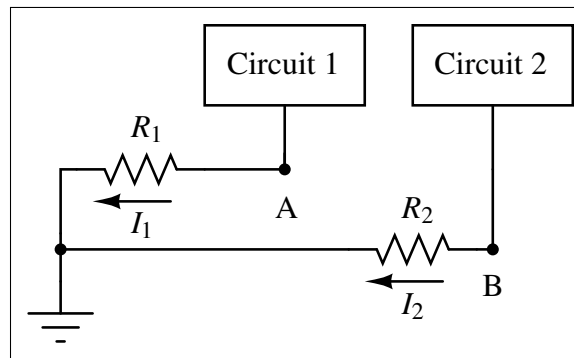


Figure 3.2: Parallel Ground System

interference (EMI), and the inductance of the ground current path can cause significant potential drops to occur.

PCB Grounding

A convenient way to apply ground in a PCB is to dedicate a layer of the board to ground, referred to as a ground plane. This allows ground connections to be made through vias to the ground plane where current can return to the voltage source. Figure 3.3 shows a simple example of current flow on a PCB. A current source drives a conductor on the top layer of a double sided PCB, and the ground current flows through vias to the ground plane on the other side of the PCB.

Current paths through the ground plane for DC, and $AC > 1\text{MHz}$ are represented by the dashed lines, and current through the top layer conductor with solid lines. Current will always follow the path of least impedance. At DC and low frequencies the impedance will be mostly resistive. This relates to a straight line across the ground plane, as shown by the dashed line labelled DC path. At high frequencies ($>1\text{MHz}$), the impedance of the ground current path is dominated by inductance. The inductance is proportional to the area of the loop formed by the current path, so the path of least inductance is one which minimises the loop area.

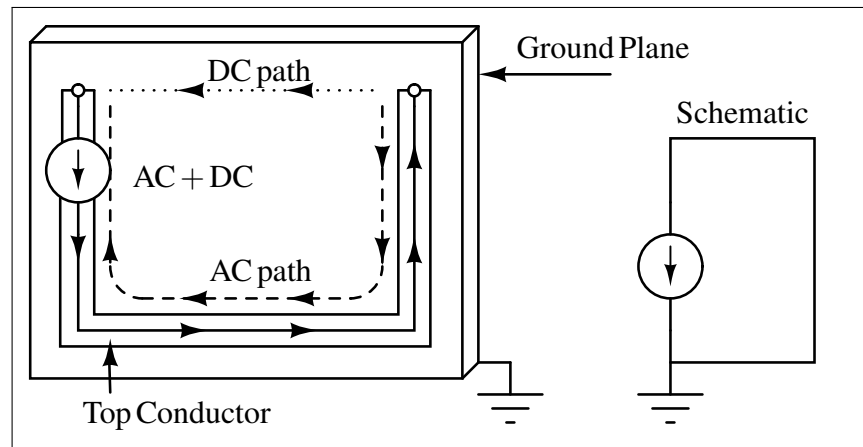


Figure 3.3: Frequency Dependant Current Paths

If the ground current flows next to or underneath the top conductor, the magnetic fields will cancel resulting in a lower inductance path. The high frequency AC path with least inductance will therefore be underneath the top layer conductor, as shown by the dashed line labelled AC path. At frequencies between DC and 1MHz the ground impedance contains resistive and inductive parts. The current will follow an arc between the DC and high frequency paths, tending toward the high frequency path as frequency increases (Brokaw and Barrow, 1989).

In a practical implementation, active components are combined on a PCB, each drawing current and requiring a ground current path. The ground plane provides a series ground scheme like that of 3.1.1 and as such ground currents need to be controlled to avoid interference between components. Current loops such as the one shown in figure 3.3 should be avoided wherever possible. A circuit within the loop will experience interference due to ground currents sharing the same path. The best option is to keep conductors on the top layer straight. This means the DC and AC ground current paths will be the same, and components can be arranged so their ground currents do not interfere with each other. Breaks in the ground plane along ground current paths should be avoided, as these force

currents to take longer paths, raising the impedance of the ground path, creating larger voltage drops in the ground plane.

Ground currents originating from power supply lines can be further controlled by using bypass capacitors. A bypass capacitor acts as a local voltage source; current will flow out of the capacitor and return through the path of least impedance to the capacitor. This limits current flow in other parts of the board, reducing the risk of interference. Bypass capacitors also help to maintain power supply voltages, particularly when high frequency currents from switching circuits or sharp transients are drawn. The power supply lines (and any PCB trace) have characteristic impedance which can be derived from the telegraphers equations. The characteristic impedance for a lossless line or at high frequencies is $Z_0 = \sqrt{L/C}$. To minimise the voltage drop due to current being drawn from the line, Z_0 should be kept small. Z_0 can be reduced by adding bypass capacitors to increase the capacitance, and keeping connections to the bypass capacitor short to reduce inductance. Bypass capacitors are a necessity in digital, high frequency analogue, and high current circuits. However, they should be used in any circuit to improve power supply distribution. $0.1\mu\text{F}$ capacitors should be used as close as possible to active components to supply high frequency currents, and $10\mu\text{F}$ capacitors throughout the circuit to maintain energy storage (Horowitz, 1989).

If analogue, digital, or high current circuits are to be combined on the same board, interference can be difficult to control. A parallel grounding scheme like that of figure 3.2 is the best option to reduce interference. This can be implemented on a PCB by separating the ground plane, providing each section with its own ground path as shown in figure 3.4. These grounds should be connected together at a single point close to the power supply.

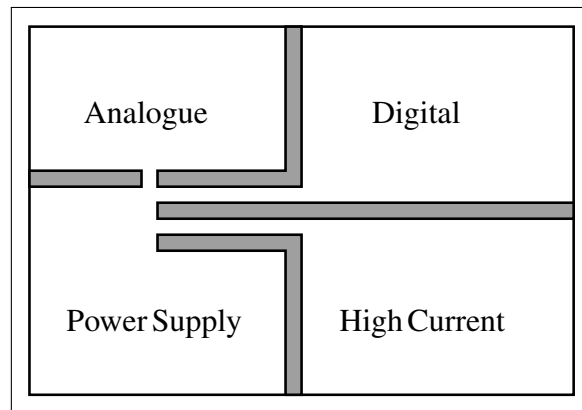


Figure 3.4: Parallel Ground Plane on PCB

3.1.2 Shielding

Shielding Cables

This section discusses the shielding of electronic cabling against interference from electric fields. An electrical model of electric field pick up by a cable is presented and used to demonstrate the effectiveness of correctly shielded cable termination.

Cables are the longest part of an electronic system, and without attention to shielding and termination they act as antennas picking up or radiating interference. Interference is coupled onto cables through interactions with electric and magnetic fields. Electric field pick up, referred to as capacitive or electric coupling, can be modelled as a capacitance between the interference source, and the conductor. Magnetic field pick up, referred to as inductive or magnetic coupling, can be modelled as a mutual inductance between interference source and cable. The mutual inductance is defined by the geometry of source and cable and the magnetic properties of the medium between them (Ott, 1988). As all experiments are to be performed away from sources of strong magnetic fields such as electric motors, only shielding against electric fields will be discussed.

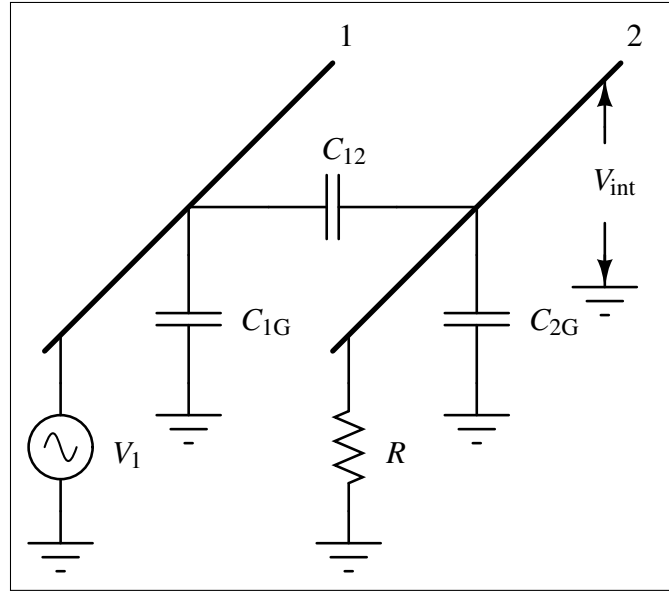


Figure 3.5: Capacitive Coupling between Unshielded Conductors

Figure 3.5 shows a representation of the capacitive coupling between two conductors. Conductor 1 represents the source of interference, having voltage, V_1 and a capacitance to ground, C_{1G} . The interference is coupled to conductor 2 through the capacitance between the conductors, C_{12} . Conductor 2 also has a capacitance to ground, C_{2G} and a resistance to ground, R . The interference voltage produced on conductor 2 is V_{int} . C_{1G} has no effect on the coupling as it is connected directly across the source V_1 . The interference voltage on conductor 2 can be expressed as follows:

$$V_{int} = \frac{j\omega [C_{12}/(C_{12} + C_{2G})]}{j\omega + 1/R(C_{12} + C_{2G})} V_1 \quad (3.3)$$

If the impedance of R is much lower than that of $C_{12} + C_{2G}$ which is true unless, R is a very high impedance node, the frequency is very high or the conductors are very close together, then (3.3) becomes:

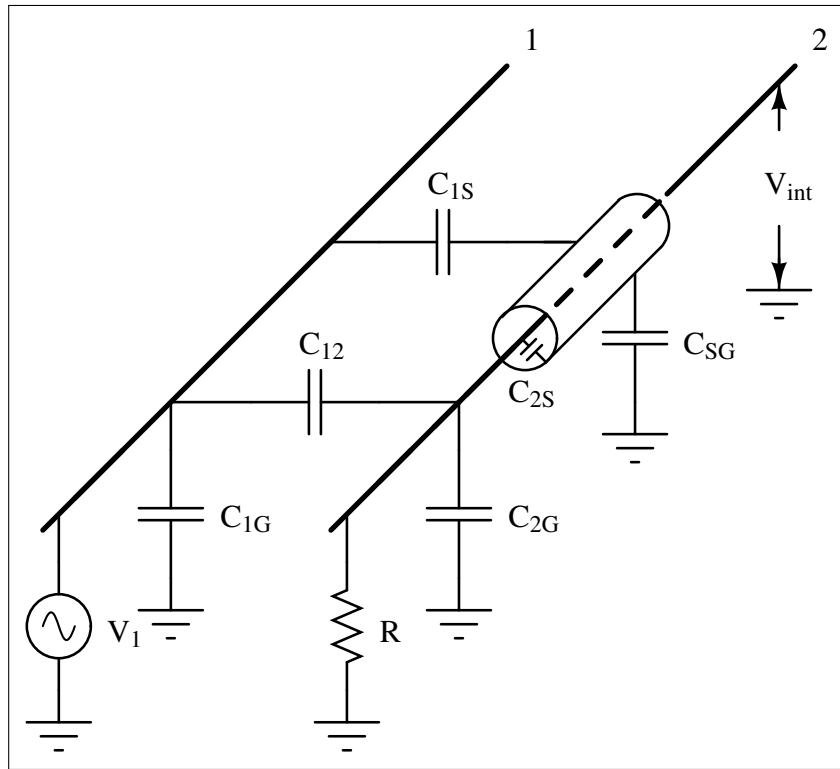


Figure 3.6: Capacitive Coupling with Shielded Conductor

$$V_{int} = j\omega RC_{12}V_1 \quad (3.4)$$

Equation (3.4) clearly shows the mechanisms of interference by capacitive coupling. To reduce interference pick up we can either reduce the capacitance, C_{12} by separating the conductors or altering their geometry, or reduce the resistance R to ground. Another possibility is to place a shield between the two conductors. Figure 3.6 shows a representation of the coupling between two conductors, with one of the conductors surrounded by a shield.

When a shielded cable is terminated there will usually be some part of the conductor which is not encased by the shield. For example many BNC connectors have a small section where the shield does not cover the conductor to allow soldering to a PCB. Additionally if a braided shield is used there will be gaps which allow capacitive coupling. In Figure 3.6 the unshielded portion has been exaggerated for clarity. C_{12} represents the coupling from the interference source to the unshielded portion, as well as any coupling due to gaps in the shield. C_{2G} is the capacitance, and R is the resistance from the unshielded portion to ground. Coupling to the shield from the interference source is represented by C_{1S} , and from the shield to ground by C_{SG} . The coupling from the shield to conductor 2 is given by C_{2S} . First we consider the coupling from the shield to conductor 2. If we substitute conductor 1 for the shield, the coupling will be the same as (3.3). For the typical case where the impedance of R is much lower than that of $C_{2S} + C_{2G}$ the voltage coupled to conductor 2 from the shield is:

$$V_{\text{int}} = j\omega RC_{2S}V_S \quad (3.5)$$

Where V_S is the voltage on the shield.

If we ground the shield, $V_S = 0$ and therefore $V_{\text{int}} = 0$. For the best results the shield should be grounded at one point only. Multiple grounds allow current to flow through the shield's resistance. This creates a non-zero voltage which will be coupled to conductor 2. If the cable is very long (greater than one-twentieth of a wavelength), multiple grounds may be necessary to maintain the voltage across the entire shield (Ott, 1988). In this work we are only concerned with low frequencies so wavelengths are very long compared to cable length (a 10kHz signal through a co-axial cable has a wavelength of 19.8km). Thus, cables should be grounded at one point only.

Provided we have a low impedance ground, the only coupling from the interference source is to the unshielded portion of conductor 2. This is the same for the

unshielded case (3.3), except that the coupling capacitance, C_{12} is greatly reduced due to the shield covering most of conductor 2.

We have covered the theory behind shielding cables, showing that to reduce interference from electric fields we should use a grounded shield, minimise the length of conductor outside of this shield, and provide a low termination resistance. The next section will discuss how to use shielding to reduce electric field interference in amplifiers.

Amplifier Shielding

This section will cover when amplifier shielding is necessary, potential problems with shielded amplifiers, and how best to implement a shielded amplifier.

When using high impedance or high gain amplifiers, electric fields coupling to the input result in signals being corrupted with interference. High impedance amplifier inputs couple electric fields at all frequencies, from static fields through to high frequency (the details of this are discussed in section 3.1.3). High gain amplifiers transform small interference signals at the input to large signals at the output. In both cases (high gain and high impedance), placing a correctly terminated shield around the amplifier will significantly reduce electric field interference from external sources. Failure to terminate the shield correctly results in feedback between the output and input of the amplifier, altering the frequency response, and potentially causing oscillation in high gain amplifiers (Ott, 1988).

Figure 3.7 shows a diagram of an amplifier with an un-terminated shield surrounding it. The capacitances, C_{inS} , C_{outS} , and C_{comS} represent the parasitic capacitive coupling to the shield from the input, output, and amplifier common respectively. The shield connects all of these parasitic capacitances, and thus there is a path from the input to the output through C_{inS} and C_{outS} . The gain of the amplifier will provide positive feedback through these capacitances, leaving oscillation as the most likely outcome. The solution is to terminate the shield to the amplifier common potential. This shorts out C_{comS} tying C_{inS} and C_{outS} to the amplifier

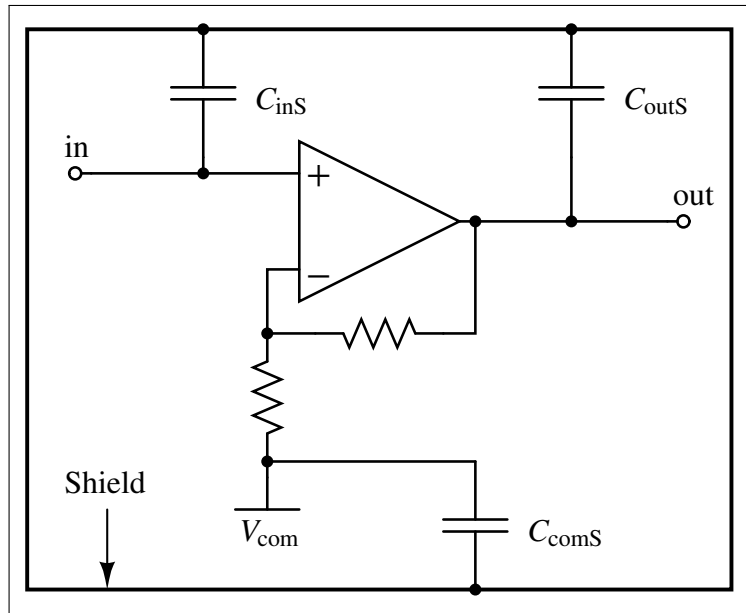


Figure 3.7: Capacitive Coupling in Shielded Amplifier

common, thus removing the connection from output to input.

In high impedance amplifiers, interference will also be coupled from sources inside the circuit, requiring further attention. The next section will cover guarding techniques to reduce this interference.

3.1.3 Guarding High Impedance Amplifiers

This section covers active guarding techniques to reduce interference in high impedance amplifiers. The interference model of (3.3) is updated for high impedance termination, highlighting the susceptibility of high impedance nodes. High impedance amplifiers are discussed, with a focus on the sources of error at the input. The mechanisms of these errors are used to explain why shielding alone is inadequate at high impedance. In light of the discussion of errors, guidelines for implement-

ing an active guard will be presented.

In section 3.1.2 it was shown that the capacitive coupling between two unshielded conductors (figure 3.5) is given by (3.3). When the impedance of R is much larger than that of $C_{12} + C_{2G}$ (3.3) becomes frequency independent and is given by:

$$V_{\text{int}} = \left(\frac{C_{12}}{C_{12} + C_{2G}} \right) V_1 \quad (3.6)$$

It can be seen from (3.6) that V_{int} is now frequency independent, thus all frequencies, will happily couple onto the high impedance node. PCB traces which run close to high impedance nodes will cause interference due to the capacitive coupling between them. Additionally, high voltage sources, such as the mains power supply, and electrostatic build up will also create interference at high impedance nodes. With the heightened susceptibility of high impedance termination it should only be used when an application demands it.

High impedance amplifiers are required when high source impedances are unavoidable. High source impedances are encountered in devices such as; pH probes, piezo-electric sensors, condenser microphones, photodiodes and non-contact bio-potential electrodes. In non-contact bio-potential electrodes the source impedance can have a magnitude of many GΩs at signal frequencies.

If source impedance is high, current flowing in the input causes a significant error voltage to occur across the source impedance, referred to as circuit loading (Horowitz, 1989). In an operational amplifier the input bias current loads the circuit. The input bias current is closely correlated to the input impedance of the operational amplifier (Pease, 1993), so an operational amplifier with low bias current will have high input impedance.

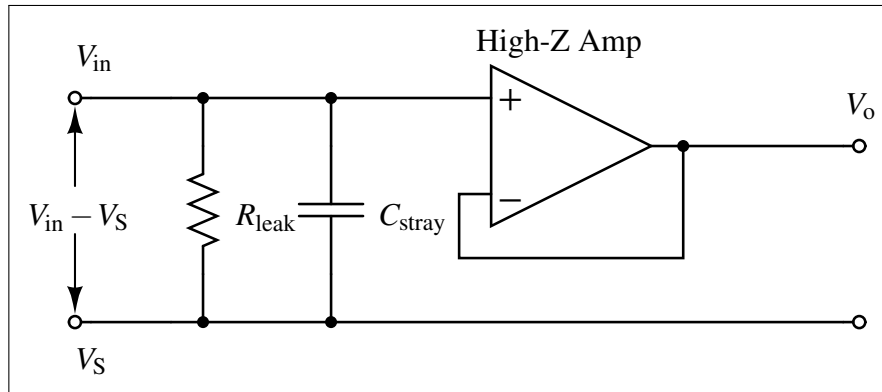


Figure 3.8: Input Problems for High Impedance Amplifiers

In addition to the input bias current, parasitic currents will flow through the finite resistance between traces on a PCB. Figure 3.8 shows a high impedance amplifier with input voltage V_{in} , and shield trace with voltage V_S . If the shield is connected to the circuit ground (for optimal interference rejection — see section 3.1.2) then the differential voltage ($V_{in} - V_S$) across the leakage resistance, R_{leak} will cause a current to flow. On a PCB R_{leak} is due to the surface and bulk resistivity of the PCB material. Increasing temperature, solder flux residue, moisture absorption, oil and dirt all conspire to lower the surface resistance of the PCB material. This increases the current in the input and thus the voltage error across any source impedance (Grohe, 2011).

In addition to the leakage current problems, the parasitic capacitance between the shield and the input trace, C_{stray} will be charged or discharged through the source impedance. The interaction between source impedance and the stray capacitance creates a large time constant, which will affect the settling time of the circuit (Grohe, 2011). The effects of the parasitic elements R_{leak} and C_{stray} can be reduced by decreasing the differential voltage, $V_{in} - V_S$. To decrease the differential voltage the input can be buffered by a voltage follower, the output of which drives a guard trace surrounding the input.

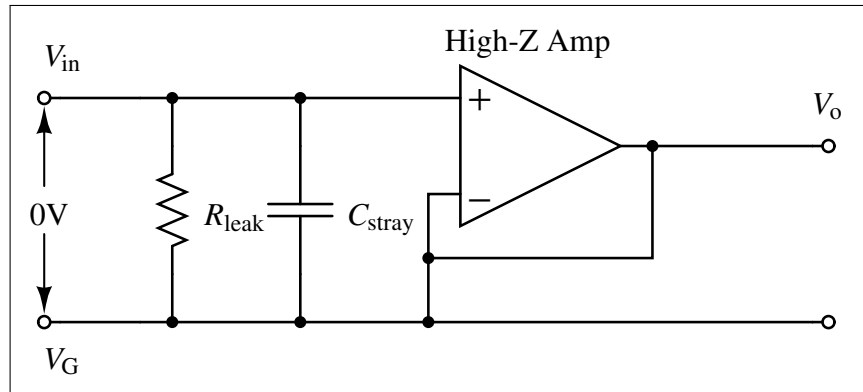


Figure 3.9: Active Guard Eliminates Input Parasitic Elements

In figure 3.9 the output of the op-amp buffer is tied to a guard trace located next to the input trace. The output voltage of the buffer will be the same as the input voltage, reducing $V_{in} - V_G$ to 0V. This configuration eliminates current flow through R_{leak} and prevents C_{stray} from charging/discharging. In reality the output voltage of the buffer will not be exactly the same as the input voltage. The op-amp's offset voltage, V_{os} will create a DC voltage across the input and guard, and the op-amp bandwidth will limit the guard's effectiveness at high frequencies. An op-amp with low offset voltage should be chosen for the guard driver; unfortunately for high impedance a FET input op-amp is usually required, these op-amps typically have offset voltages which are an order of magnitude higher than BJT input op-amps. Temperature stability of the voltage offset in FET op-amps is also worse than BJT inputs. These problems have been addressed in semiconductor fabrication and modern FET amps are available with low offset voltage ($\pm 26 \mu V$ (Texas Instruments, 2008)), and offset voltage drift characteristics ($-1.5 \mu V/^{\circ}C$ (Texas Instruments, 2008)).

Figure 3.10 shows a PCB layout for a standard, single op-amp SOIC-8 package in voltage follower configuration. The guard trace is routed all the way around

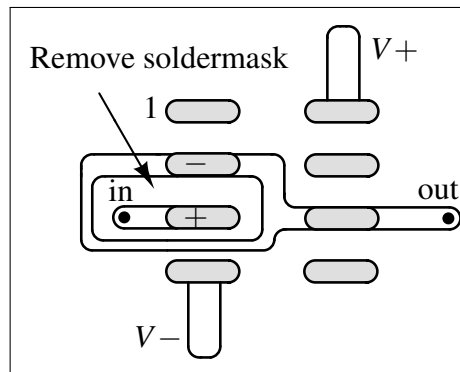


Figure 3.10: Guard Layout for Voltage Follower

the input, if a double sided PCB is used the guard ring should be implemented on both sides, and connected together through a via. The guarding on the other side of the board, prevents leakage from the bottom layer to the input via, as well as reducing the leakage through the PCB material.

Soldermask helps to prevent moisture (which reduces the resistivity) being absorbed into the PCB. However typical soldermask material has a lower surface resistivity than the board material. The soldermask should be removed from the guard ring area. After the PCB has been populated the board can be encapsulated with a high quality conformal coating to prevent moisture absorption.

In figure 3.10 pin 4 is the negative power terminal of the op-amp — it is critical that the guard comes between this pin and the input. To achieve this the guard ring must be routed between pins on the op-amp package. The package should be chosen so that whatever PCB manufacturing process is used allows traces to be routed between pins. Alternative packages are available, particularly for high input impedance op-amps which ease guard ring layout. The Burr Brown INA116 from Texas Instruments buffers the inputs on chip, providing the output on dedicated pins surrounding the inputs. This eases guarding layout, as well as providing

some extension of the guard internally. The LMP7721 from National Semiconductor (now part of Texas Instruments) comes in a SOIC-8 package, with inputs on pins 1 and 8, power on pins 4 and 5, output on pin 4, and no connection (NC) on pins 2,5 and 7. Having the power pins away from the input helps reduce leakage to the inputs, and the NC pins allow guard traces to be connected to these pins, easing the implementation of the guard ring.

3.2 Shielded Test environment

This section presents the shielded testing environment created for this research. This enclosure is used for all measurements of high impedance circuits performed.

In order to characterise the high impedance circuits developed, control over the electromagnetic environment is essential. A shielded enclosure was designed so that power supply voltages, and input and output signals could be routed to the device under test (DUT), without exposing the DUT to large interference potentials. Figure 3.11 shows a picture of the shielded enclosure.

The enclosure consists of a box with a hinged lid, and various connections to allow input and output from the DUT. Three banana sockets provide inputs for power supply voltages, with one socket directly connected to the enclosure (this should be the ground potential). A slot in the side of the enclosure was included to allow oscilloscope probes to be fed into the enclosure. When the lid is closed the slot is partially closed off, to limit the break in the shield. This slot can be patched with copper tape if the shielding is not sufficient. Signal input and output are provided through two BNC sockets, one insulated and one grounded. Whether the input or output is connected to the insulated or grounded connector should be determined based on the equipment being connected.

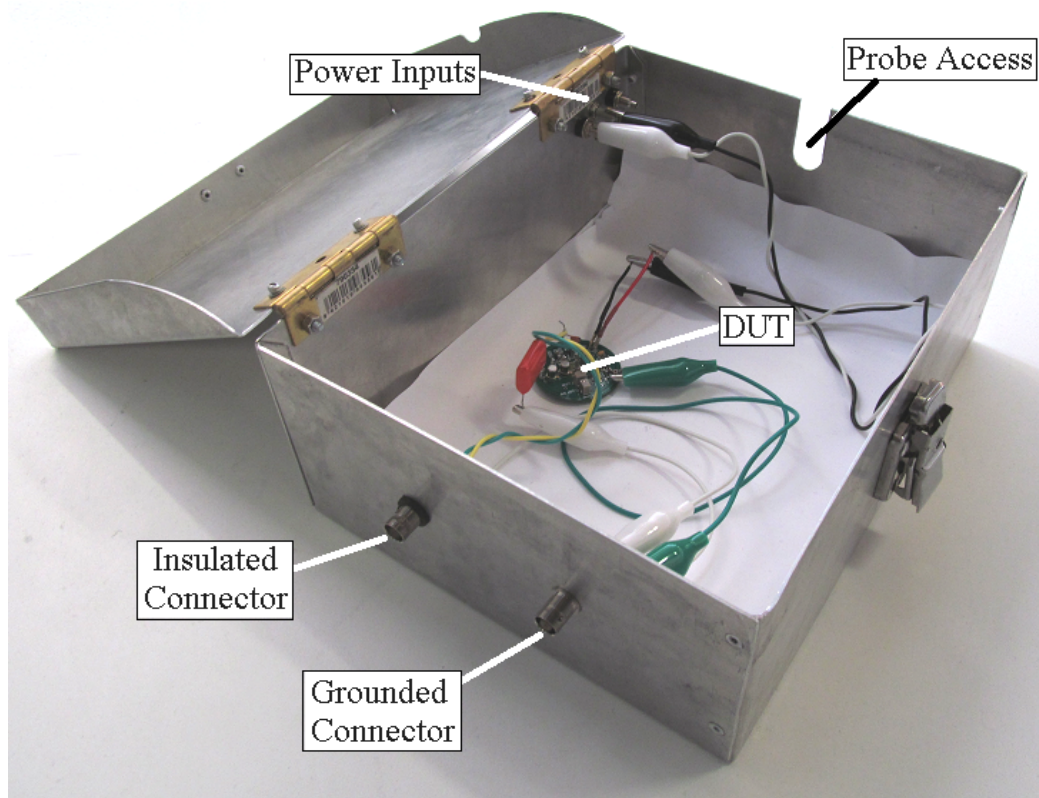


Figure 3.11: Shielded Enclosure for Circuit Testing

Chapter 4

Methodology

4.1 Input Capacitance Measurement

The aim of this experiment is to measure the input capacitance of the sensor electronics. Knowledge of the input capacitance is required for measuring the input bias current, and determining the gain required for the capacitance neutralisation circuit.

4.1.1 Hypothesis

This test exploits the low pass filter formed with a resistive source (R_S) and the capacitive component of the DUT's input impedance. The input capacitance can be measured by finding the -3 dB frequency of the filter and extracting the input capacitance:

$$C_{\text{in}} = \frac{1}{2\pi R_S f_{3\text{dB}}} \quad (4.1)$$

The input capacitance of an amplifier, particularly a FET or CMOS amplifier is mostly due to protection diodes at the input. The capacitance is therefore voltage dependant, and hence this method provides only a first order approximation of the input capacitance.

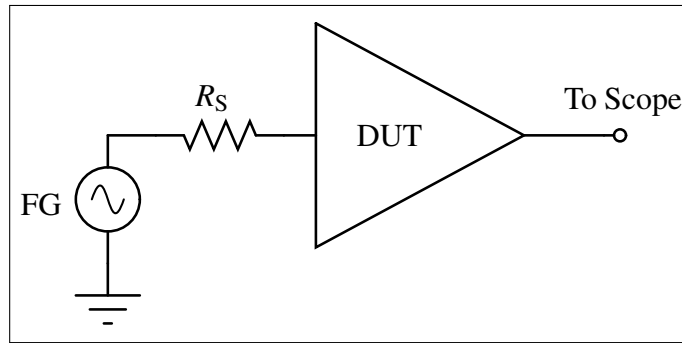


Figure 4.1: Input Capacitance Test Circuit

4.1.2 Method

The value of R_S is chosen so that the -3 dB frequency is at least 10 times smaller than the bandwidth of the DUT and the measurement device. Determining this value may require some trial and error if the magnitude of the input capacitance is not approximately known. The parasitic capacitance of the resistor may complicate the measurement if the input capacitance is low. To reduce the capacitance of the source resistor, several resistors can be soldered together in series. The capacitance of each resistor will add in series, reducing the overall capacitance.

The device under test (DUT) should be placed inside the shielded enclosure. The function generator is connected through a resistance R_S to the input of the DUT as shown in Figure 4.1. The output of the DUT is connected to an oscilloscope to view the signal.

The function generator is set to output a sine wave of 100Hz. The amplitude of the sine wave should be set to within the input voltage range of the DUT, with a DC offset to match the input bias voltage of the DUT.

The amplitude of the output is measured on the oscilloscope for the 100Hz

input signal. From this amplitude the -3 dB amplitude is calculated:

$$V_{-3\text{dB}} = V_{100\text{Hz}} \times \frac{1}{\sqrt{2}} \quad (4.2)$$

The frequency of the function generator is increased until the output reaches this amplitude. This frequency can then be used in (4.1) to calculate the input capacitance.

4.2 Input Bias Current Measurement

The aim of this experiment is to measure the input bias current of the sensor amplifier. This measurement can be used to verify the effectiveness of the input guarding scheme against leakage currents on the PCB.

4.2.1 Hypothesis

Because of the ultra-high input impedance of the input, measuring the input bias current directly is not possible. Any measurement probe at the input will load the input, resulting in an erroneous measurement. The input bias current varies with temperature and humidity, and as such these parameters need to be controlled to provide comparable results. The humidity can be controlled by using silica desiccants to remove moisture. Ambient temperature should be measured before testing. If the environment is air conditioned, testing when the air conditioning system is active is a good way to maintain a constant temperature.

As the input amplifier is a unity gain buffer, the input voltage can be determined by probing the low impedance output of the buffer, without loading the input. The input bias current can then be determined to an order of magnitude by relating the input voltage to the input current and the input capacitance.

If the input capacitance is charged from a DC source, and then that source removed, the input node will be floating, connected only through the amplifier

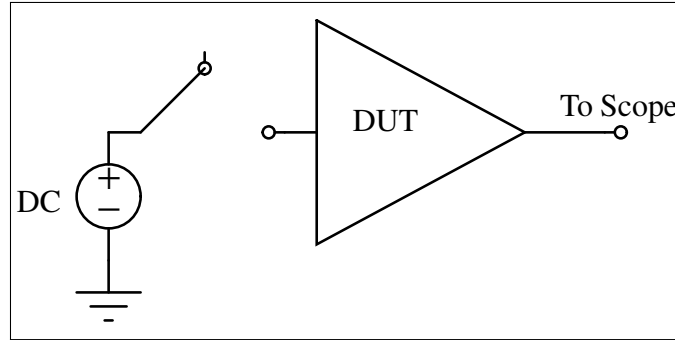


Figure 4.2: Input Bias Current Test Circuit

input impedance, and any leakage paths the rest of the circuit. The input current (bias current and leakage paths) will discharge the input capacitance of the sensor, producing a change in voltage. The input current can then be determined by measuring the rate of change of this voltage and their relationship given as:

$$I_{\text{in}} = C_{\text{in}} \frac{dV(t)}{dt} \quad (4.3)$$

Where I_{in} is the total input current, C_{in} is the input capacitance of the DUT, and $dV(t)/dt$ is the rate of change of the input voltage.

The input capacitance can be measured using the method given in Section 4.1.

If the current I_{in} is of the same order as the quoted input bias current of the DUT, then the input guarding scheme can be deemed to be effective against leakage currents on the PCB.

4.2.2 Method

The circuit of Figure 4.2 should be placed inside of the shielded enclosure, to prevent external electric fields from charging the input, and disrupting the measurement. The switch can be implemented simply by connecting a wire to the

input to close the switch and removing the wire to open the switch. The DC voltage should be set to half the supply voltage for a single supply amplifier, or ground for a dual supply. This allows the input current to charge or discharge the input, depending on its polarity.

Data acquisition is performed using an oscilloscope controlled by the LabView program shown in Figure 4.3. The oscilloscope is selected from the VISA resource name drop down menu. The acquisition channel should be set to the oscilloscope channel which the test jig is connected to, and the probe attenuation to the appropriate setting (1x for direct cable connection, 10x for connection through high impedance probe). The voltage resolution of the measurement is set by the V/Div parameter (lower V/Div gives higher resolution). The Initial Reference parameter should be set to the value of the DC source. This parameter sets the initial voltage offset of the oscilloscope. The input capacitance of the DUT can be entered into the Input Capacitance parameter, which along with the integration time, calculates an estimate of the bias current while the program is run. The integration time parameter sets the time over which the rate of change of the voltage is measured. The program samples the output voltage at time intervals given by the input variable Sample Period (ms). The Period Too Small indicator will light if the sample period is too small to complete the measurement (around 1000ms is a good place to start). The program measures the DC voltage at intervals set by the Sample Period variable. The voltage is then plotted vs time on the display to provide feedback to the user. The data is saved to a comma separated file by turning on the Save Data button. This data can then be used in MATLAB to extract the rate of change of the input voltage and calculate the input current.

The DC voltage is connected to the DUT to charge the input capacitance. This should be left for a few minutes to ensure the input is fully charged. The program should then be run, the wire connecting the DC source to the input removed, and the lid of the shielded enclosure secured. The test should be run until a clear linear slope is seen on the program display (around 300 seconds should be sufficient).

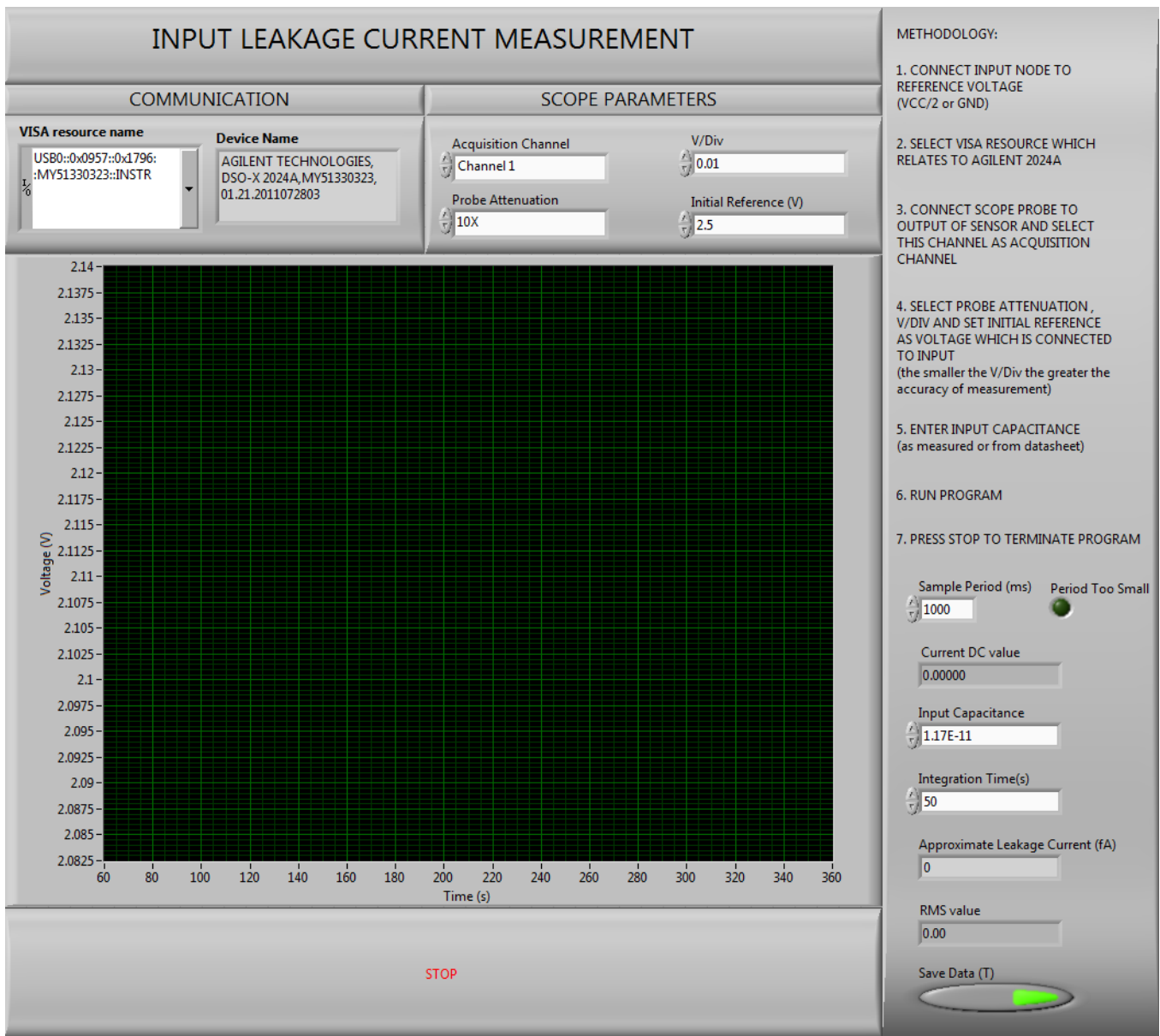


Figure 4.3: Lab View Program for measuring input bias current

The data should be analysed in MATLAB extracting dV/dt and calculating the leakage current using (4.3). Figure 4.4 gives an example of the data obtained from this test.

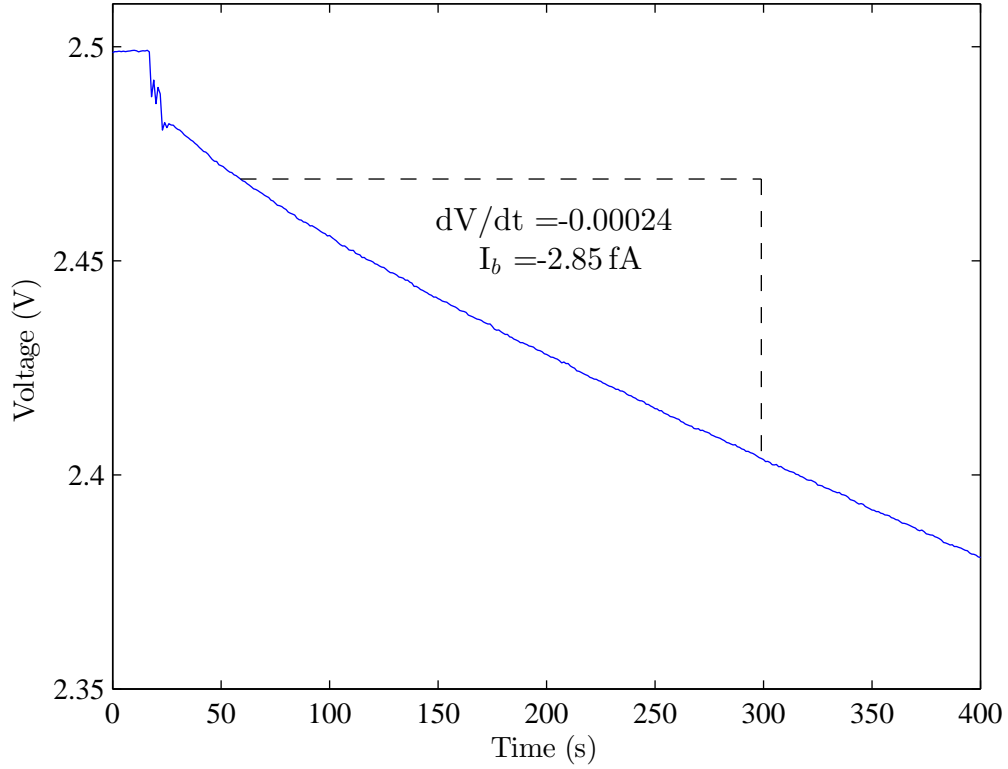


Figure 4.4: MATLAB analysis of bias current measurement

4.3 Transfer Function Measurements

The aim of this method is to characterise the transfer function of circuits used in this research. The transfer function provides knowledge of the phase and gain of the circuit over frequency. This can be used to specify the bandwidth, gain accuracy, and derive the input impedance of the circuit.

4.3.1 Hypothesis

The transfer function given by (6.3) defines the input to output relationship of a circuit or system. By measuring the amplitude of the input and output voltages,

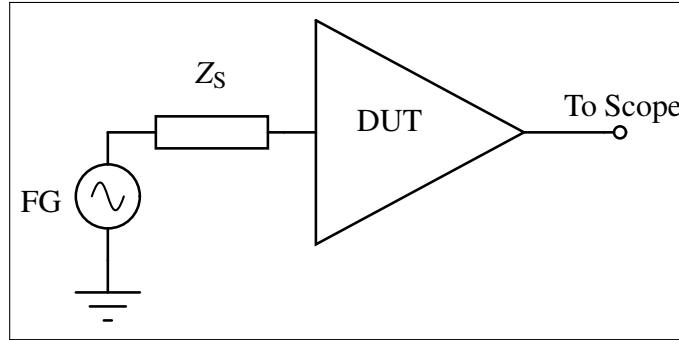


Figure 4.5: Transfer Function Test Circuit

and the phase difference between them over a range of input frequencies the frequency response of the circuit can be quantified.

$$T(j\omega) = \frac{V_{\text{out}}(j\omega)}{V_{\text{in}}(j\omega)} \quad (4.4)$$

where $T(j\omega)$ is the transfer function, $V_{\text{out}}(j\omega)$ is the complex output voltage, and $V_{\text{in}}(j\omega)$ is the complex input voltage.

The transfer function defines the bandwidth and gain of the circuit, as well as revealing any resonances in the response. The input impedance of the circuit can also be estimated by fitting a model to the response. The derivation of the input impedance from the transfer function is given in Section 7.4.

4.3.2 Method

The circuit shown in Figure 4.5 should be placed inside the shielded enclosure, or simply connected as shown if the DUT is already housed in a shielded enclosure. Z_S should be a capacitor with high parallel resistance (typically the higher the rated voltage the higher the parallel resistance — capacitors rated to 1 kV were

used in this research) for AC coupled tests. Z_S can be omitted for DC coupled tests. The transfer function can then be measured using the LabView program shown in figure 4.6.

The function generator and oscilloscope are selected from the VISA communication panel. The program automatically detects which instrument is which, so the only requirement is that both the function generator and the oscilloscope are selected. The function generator panel is used to setup the function generator output. The oscilloscope panel sets up the data acquisition for the input channel and the output channel. AC coupling should only be used if the response is measured above 10Hz, as AC coupling introduces a high pass filter with a cut off frequency of 1 Hz. The frequency sweep panel sets up the frequency range of the test. The spacing of the frequency sweep can be set to linear: where Step Size/No. Points defines the size of the frequency steps, or logarithmic: where Step Size/No. Points defines the number of data points to be measured. The measurement settling time panel controls the settling time between measurements. Initial settling defines the time between the initial application of the input signal and the first measurement. This should be set to greater than the settling time of the circuit to ensure the initial measurements are taken under steady state operation. Settling defines the time between measurements, and can be set much lower, as the input voltage is not changed between measurements. Min.Meas.Time sets the minimum acquisition time of the program, this should be used when higher frequency measurements are taken, as the program may run faster than the hardware can keep up with. The data acquisition panel sets the acquisition type (normal, hi-resolution, averaging, or peak detect), the number of averages performed (for averaging acquisition type) and the number of full cycles over which the measurement is taken. User feedback is provided through the active measurement panel, which displays the most recent measurements, and the graph which plots the transfer function as the program runs. The data is saved when the save data button is pressed. This button turns bright green when saving is selected.

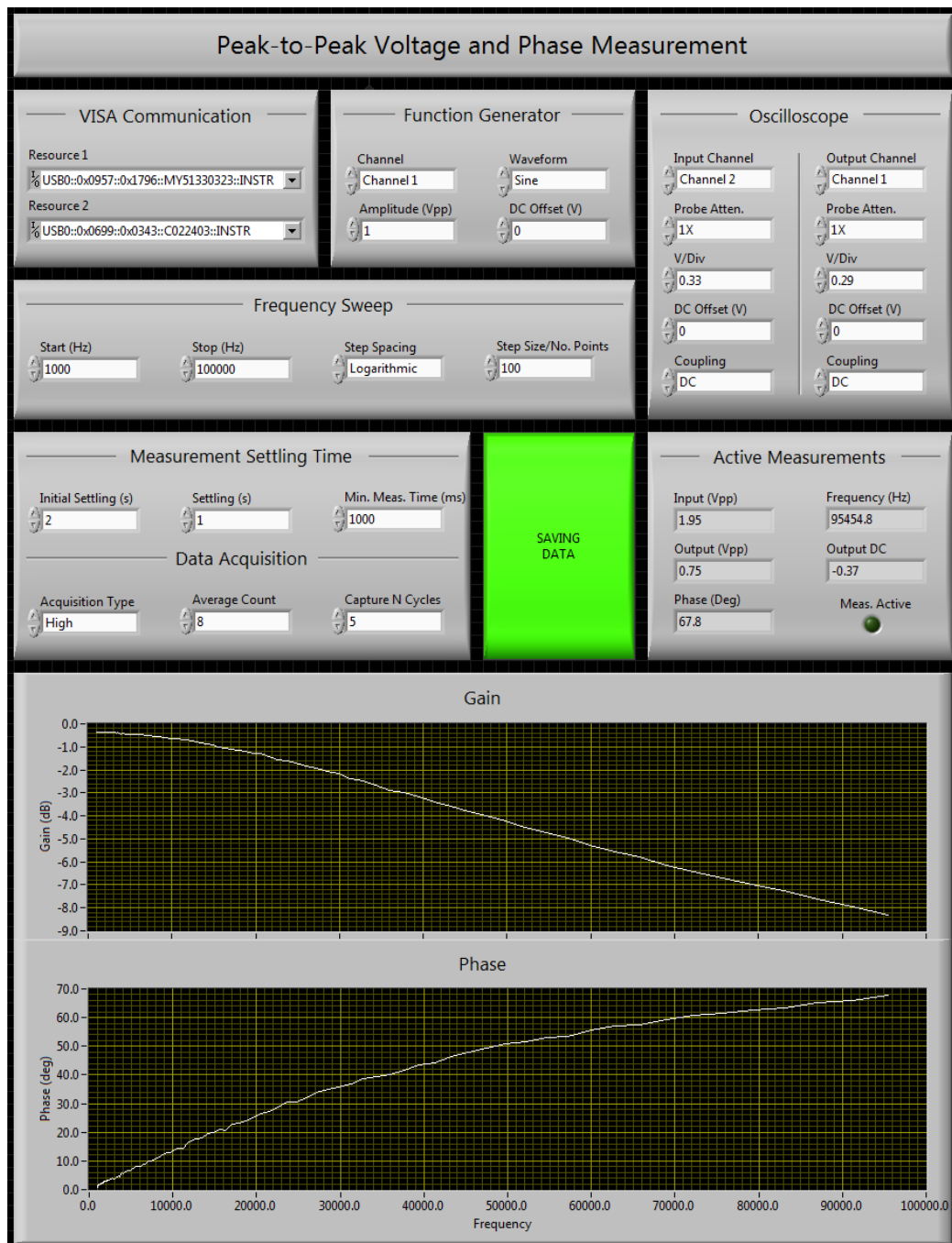


Figure 4.6: Lab View Program for measuring Circuit Transfer Function

The oscilloscope trigger must be setup manually as different circuits may require different triggering methods. In this research the trigger output of the function generator (a $5\text{ V}_{\text{p-p}}$ square wave) was connected to the external trigger input of the oscilloscope. The trigger was set to Normal (only triggers on a event) rather than Auto (automatically re-triggers) so that when averaging signals, re-triggering occurs in phase with the previous measurement.

The input frequency, input p-p voltage, output p-p voltage, and phase from input to output are saved in a comma separated txt file. This data can easily be imported into MATLAB for further analysis and to create figures.

4.4 Noise Measurements

The aim of this experiment is to characterise the input voltage noise spectral density of circuits used in this research. This measurement defines the lower limit of input signals which can be resolved. It also identifies small resonances in the system which can illuminate non-ideal circuit function.

4.4.1 Hypothesis

The measurement of noise requires a measurement device which has lower noise than the DUT. For measuring low noise devices this can be difficult to obtain. A way to improve this situation is to amplify the output of the DUT with a low noise amplifier, prior to measuring the noise. The amplification factor can be removed from the measured spectrum to obtain the input noise of the DUT.

The voltage noise spectral density is measured in units of $V_{\text{RMS}}/\sqrt{\text{Hz}}$. If the noise is white, the voltage noise spectral density can be transformed to a total RMS noise by multiplying by the square root of the bandwidth. Semiconductor junctions introduce flicker noise or $1/f$ noise which increases as frequency decreases. The corner frequency of the noise is the point where the $1/f$ noise becomes greater

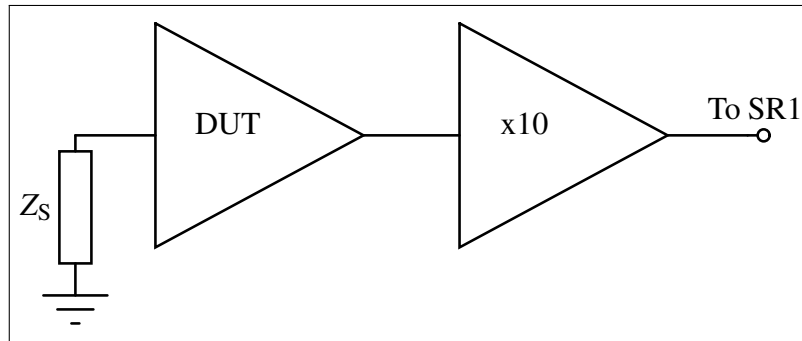


Figure 4.7: Noise Measurement Circuit

than the white noise. This is important when characterising noise, particularly in low frequency systems as below this frequency noise contributions become significant.

4.4.2 Method

The circuit in Figure 4.7 shows the setup for performing noise measurements. The source impedance Z_S can be altered to mimic the conditions observed under normal operation. For DC coupled circuits Z_S should be shorted out. For characterising the non-contact sensors, Z_S should be set to a capacitance, as this represents the input under normal operating conditions. The DUT should be placed in the shielded enclosure, the x10 pre-amplifier should have very low noise characteristics. The output of the pre-amplifier is connected to the SR1 audio analyser to measure the noise spectrum.

The FFT analyser of the SR1 should be used to capture the input signals, and configured as follows:

- High Resolution Converter – $F_s = 128\text{ kHz}$
- Averaging – 100 (Fixed)

- Resolution – 32k (131seconds)
- Window – Hanning
- DC correction – none

The bandwidth can be set between 97.655Hz and 25kHz. The bandwidth should be set so that the 1/f corner frequency can be observed. A graph display should be opened on the SR1 to allow the measurements to be viewed as they happen. The power spectrum of the input channel should be added to the graph, and the units changed to $V/\sqrt{\text{Hz}}$. Before beginning the measurement the averaging should be cleared. Once the measurement is complete the data can be exported as a comma separated text file. This file can then be imported to MATLAB for analysis. The power spectrum data should be divided by the gain of the pre-amplifier to give the input voltage noise spectral density.

4.5 Gain vs Distance Characterisation

The aim of this experiment is to measure the gain of the non-contact sensors as a function of the distance away from the source. This measurement shows how the sensor responds to fluctuations in the distance between the sensor and the body.

4.5.1 Hypothesis

The reduction of gain as the non-contact sensor is moved further away from the source is due to the capacitance between the sensor and the source interacting with the input capacitance of the sensor. The mechanics of this gain reduction are given in Section 6.5. Before applying capacitance neutralisation feedback the input capacitance can be measured using the method in Section 4.1. After applying capacitance neutralisation this method requires very high source resistances, which introduce unacceptable noise levels to the measurement. Measuring the gain vs distance before applying capacitance neutralisation can be used to derive

the capacitance from the source to the sensor input. After applying the capacitance neutralisation the gain vs distance can be measured again. Using the source capacitance previously derived to estimate the input capacitance, the effectiveness of the capacitance neutralisation feedback can be quantified.

4.5.2 Method

Figure 4.8 shows the experimental setup for measuring the gain vs distance response of the sensor. The input voltage from a function generator is applied to the plate, simulating a body surface potential. The sensor is attached to by the clamp to a micrometer controlled Z-axis positioning device. The distance can be controlled and measured using the micrometer. The input and output voltage of the sensor are measured using the SR1 audio analyser for each distance step.

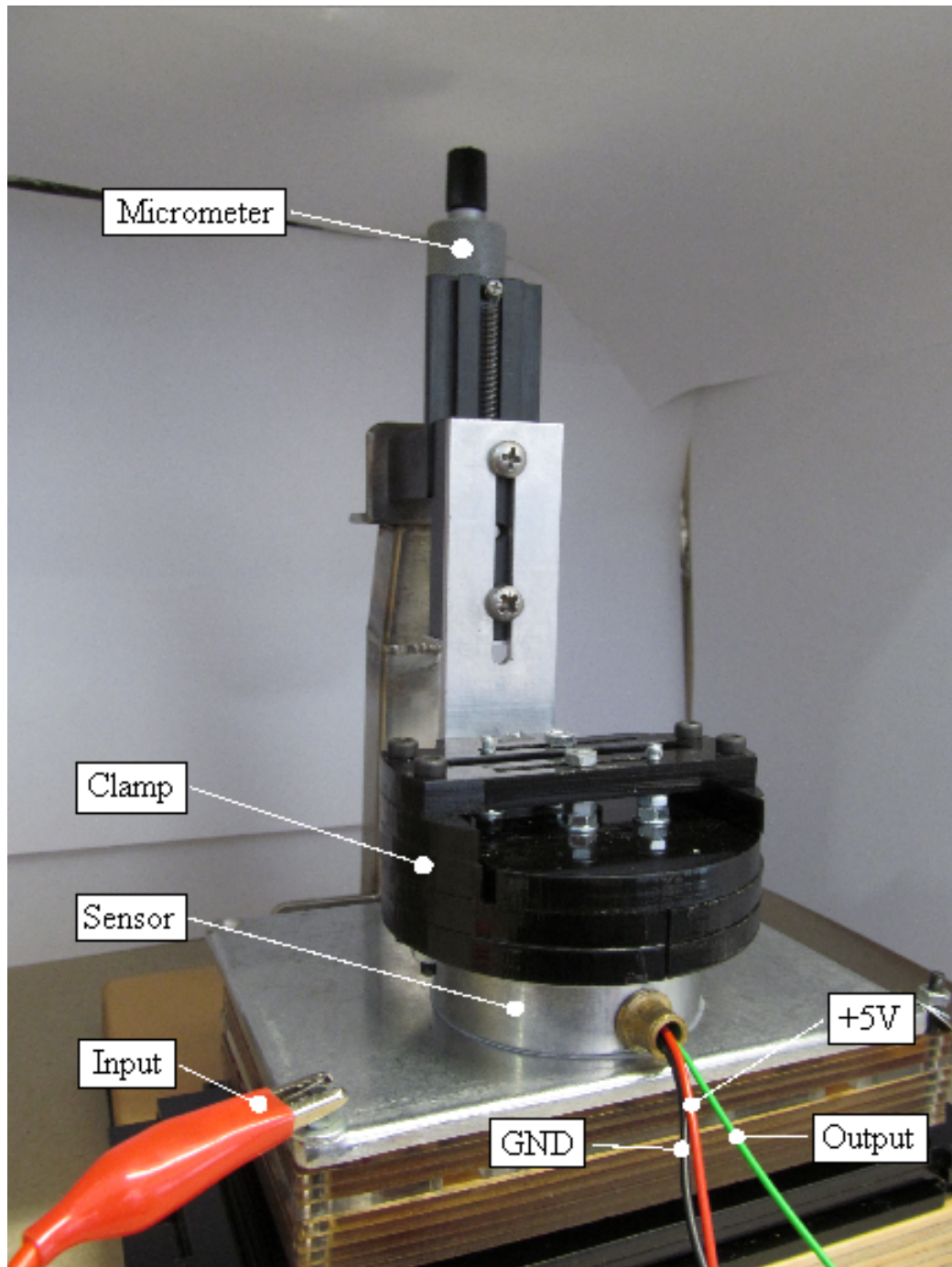


Figure 4.8: Experimental Setup for Gain vs Distance Characterisation

Chapter 5

Differential Amplification System

This chapter presents the design and evaluation of a system for acquiring signals from capacitive bio-potential sensors. Requirements for the system will be outlined and justified with reference to the bio-potential recording environment. These will be translated into specifications for the system design and construction. Characterisation of the system's performance is presented, and evaluated with respect to the specifications. Problems discovered in the original design are discussed, and the implemented solutions are presented. Measurements of the common mode rejection, frequency response, and noise of system are presented to show the system performance.

5.1 Requirements

This section presents the general requirements for a system to acquire signals from capacitive bio-potential sensors. Discussion of the bio-potential recording environment identifies the signal processing blocks needed, and the critical requirements of each block. In the following section these requirements are used to form quantitative specifications, informing system design.

The signals of interest in this work come from the difference in potential be-

tween two points on the human body, such as across the heart in two lead ECG recording. The differential signal between two bio-potential sensors shows the propagation of the bio-potentials, which can be used to aid diagnosis of pathological function in the patient (see section 2.3 for details of clinical electrophysiology). The amplitudes of bio-potentials are typically very small compared with sources of interference in the environment (see section 3.1 for more detail on interference), thus an amplifier is needed which rejects the interference and amplifies the differential signal. Fortunately the distance between two points on the human body is very small compared to the wavelength of low frequency electromagnetic waves. This means that low frequency interference will be at approximately the same potential, or common, to all sensors attached to the patient. This common mode signal can be removed by using a differential amplifier with high common mode rejection (CMR). In ECoG measurement the stimulation source is also a source of interference. To measure ECoG across the entire range of human hearing would require signal frequencies up to 20kHz. Unfortunately CMR is frequency dependent, being very good at low frequencies ($<100\text{Hz}$), but decreasing rapidly with increasing frequency. This puts a limit on the range of frequencies which can be used in ECoG, as the decreased CMR at higher frequencies results in higher levels of interference.

The amplitude of bio-potentials ranges from $10\mu\text{V}$ for EEG to 10mV for EMG (Webster, 1999). In order to analyse these signals, amplification is essential. To view the signal on an oscilloscope, the signal needs to be amplified above the internal noise of the oscilloscope and connecting cables. For digital conversion, amplification is required to match the input range of the ADC, maximising the resolution. The internal noise of the amplifier and passive components needs to be kept much lower than the expected input signal level to maintain signal to noise ratio.

Due to the low frequency of some bio-potential signals, long time base settings are used on digital storage oscilloscopes (DSO) to view the signals. At these

settings many DSOs will lower their sampling frequency, so to prevent aliasing low pass filtering at the output is required.

Capacitive bio-potential sensors require a DC power supply to operate. This should be integrated into the system and supplied through the connection to the capacitive sensor. Despite the excellent power supply rejection (PSR) of modern op-amps, power supply ripples will still affect the signal output. The small amplitude of bio-potential signals requires the consideration of interference from the power supply.

From the foregoing discussion the building blocks needed to create the system can be identified. The following bullet points identify these blocks, and their general requirements.

- Instrumentation Amplifier
 - High CMR is needed to eliminate common mode interference.
 - The CMR vs frequency needs to be taken into account, especially for ECoG measurements.
- Gain Amplifier
 - Amplification is necessary for viewing and analysing signals.
 - Amplifier noise should be kept well below signal amplitudes.
- Data Acquisition
 - Bandwidth limiting should be used to avoid aliasing upon digitisation.
- Power Supply
 - An integrated low noise power supply for powering capacitive sensors.

The following section will develop the system architecture, presenting a block diagram, specifying the performance required of each block, and detailing the design process.

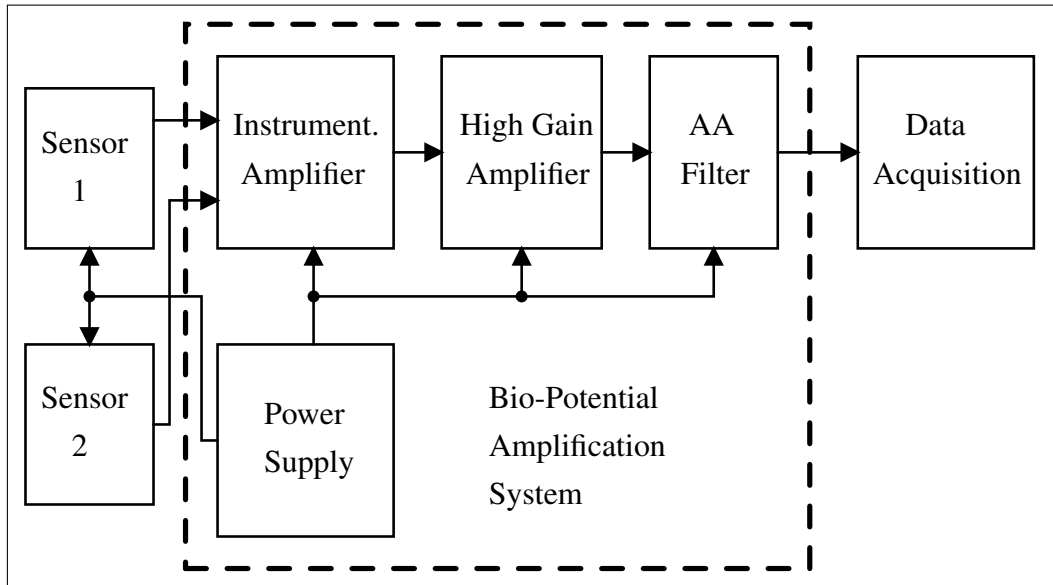


Figure 5.1: Block Diagram of Bio-Potential Measurement System

5.2 Design and Evaluation

This section presents the design and evaluation of the bio-potential amplification system. A block diagram is presented, showing the system elements and their connections to each other. The design of each block will be presented separately, covering design specifications, component selection, and circuit design. Problems and solutions discovered are addressed for each block, and relevant performance metrics are presented. System construction is presented including the design of PCBs and an enclosure for the system.

5.2.1 System Overview

The system block diagram of figure 5.1 was developed using the requirements identified in section 5.1. The block diagram incorporates the capacitive bio-potential sensors (Sensor 1 and Sensor 2), the bio-potential amplifier (elements

inside the dashed box), and the data acquisition device (oscilloscope or other digitisation device). The following sections present the design of the bio-potential amplifier: the instrumentation amplifier, high gain amplifier, anti-aliasing filter and the power supply.

5.2.2 Instrumentation Amplifier

This section details the design of the instrumentation amplifier of the bio-potential amplification system. The critical performance characteristics of the instrumentation amplifier are identified, and used to select electronic components. The output characteristics of this stage; gain, bandwidth, and impedance are defined to inform the design of subsequent stages. Power supply demands are estimated for inclusion in the total power budget for the bio-potential amplification system.

In the bio-potential recording environment the common mode interference is several orders of magnitude larger than the signals of interest. The reduction of this interference is critical to obtaining high quality bio-potential signals. The CMRR of the instrumentation amplifier (see section 2.5.4 for discussion of CMRR), defines how much of the common mode signal will be rejected, thus the CMRR is the critical parameter for this stage. A specification for the minimum CMRR can be reached by defining the largest source of interference at the input, and the amount of this interference which is tolerable at the output.

The largest source of common mode interference comes from the mains power supply, typically 1V at 50Hz (Winter and Webster, 1983). Assuming the source impedances are well matched, the common mode input impedance is high, and allowing for $10\mu\text{V}$ of interference; the minimum CMRR can be calculated using a simplified version of (2.1):

$$\begin{aligned}
\text{CMRR}_{\min} &= \frac{V_{cm}}{v_{int}} \\
&= 1\text{V}/10\mu\text{V} \\
&= 10 \times 10^6 \\
&= 100\text{dB}
\end{aligned} \tag{5.1}$$

As any mismatch in source impedance will further degrade the CMRR, it is beneficial to specify CMRR of higher than 100dB. The CMRR will also degrade with frequency as capacitance starts to dominate the common mode input impedance. The CMRR of most instrumentation amplifiers begins to degrade at about 100Hz-1kHz (Pallas-Areny and Webster, 1991) dropping 20dB/decade thereafter. For ECoG measurements this limits the stimulation source rejection at higher frequencies, resulting in a higher signal to interference ratio.

From these considerations the specification for the instrumentation amplifier is given as:

- CMRR > 100dB at 50Hz

And providing this specification is met the amplifier should

- Maintain high CMRR to at least 4kHz (Masood et al., 2012)

The noise of the amplifier should also be taken into consideration. The output of the capacitive sensors will be at low impedance, thus current noise is not a critical factor in this stage. The voltage noise is critical to obtaining high quality, low level signals. Voltage noise spectral density is typically quoted at 1kHz, but many bio-potentials have energy below this frequency. Thus attention should be paid to the low frequency noise performance, opting for amplifiers with a low $1/f$ corner frequency.

Most analogue semiconductor manufacturers offer integrated circuit (IC) instrumentation amplifiers with precisely matched integrated feedback resistors.

This precise matching allows very high common mode rejection to be achieved without using expensive, high precision, discrete resistors. The integration of these resistors also provides better thermal coupling between resistors than a discrete implementation, reducing errors due to temperature drift. Integrated instrumentation amplifiers typically allow gain to be set with a single external resistor, where the tolerance of this component only affects the gain of the circuit, not the CMRR. IC pins for the gain setting resistor are typically positioned next to each other, simplifying PCB layout by enabling short traces to the resistor, which minimises parasitic impedances. For these reasons an integrated instrumentation amplifier was chosen to be the basis of this stage.

The instrumentation amplifiers considered were the AD620, AD8221AR, and INA128. All these amplifiers when operated with a gain of 10 meet the CMRR specification at 50Hz (5.1) and have $1/f$ voltage noise corner frequencies below 100Hz. The AD620 and INA128's CMRR begin to decrease above 200Hz, operated with a gain of 10 the CMRR at 10kHz = 80 and 70dB respectively (Analog Devices, 2011a) (Texas Instruments, 2005). The AD8221AR instrumentation amplifier has the highest CMRR with frequency of all currently available amplifiers. Operated with a gain of 10 the AD8221AR has a minimum CMRR of 90dB at 10kHz, low voltage noise ($10.5nV/\sqrt{Hz}$) and a $1/f$ noise corner frequency of 10Hz (Analog Devices, 2011b), making the AD8221AR an excellent choice for the basis of the instrumentation amplifier design.

A potential problem arises when an instrumentation amplifier is operated in an environment with strong high frequency signals. Due to the reduced CMRR, high frequency signals will be transformed into common mode signals. The high frequency common mode signal can then be rectified by the base emitter junction of the input stage of the amplifier. This rectification causes a DC offset that will vary in proportion to the strength of the high frequency field, potentially causing measurement errors (Kester, 2009). The energy of high frequency signals can be reduced (and thus the potential for rectification reduced) by implementing a pas-

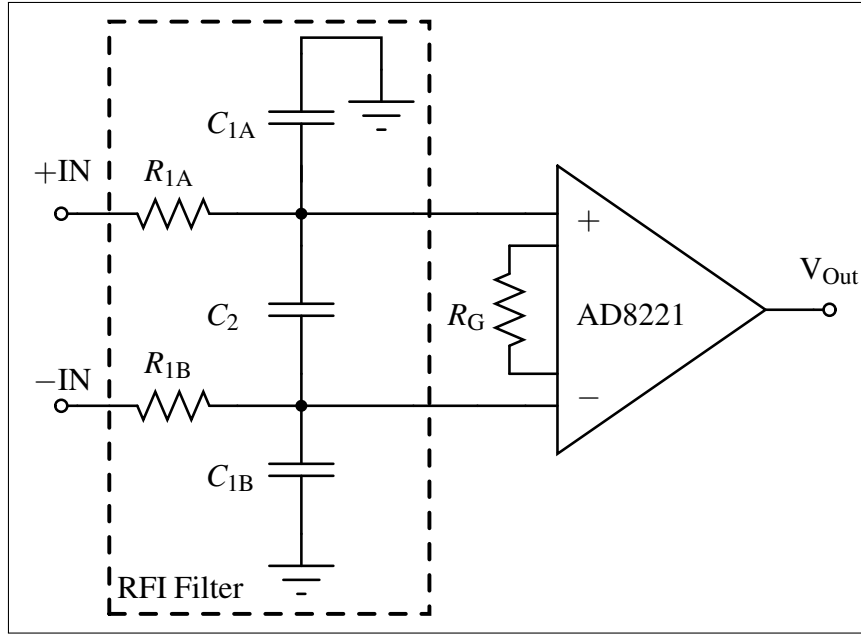


Figure 5.2: Instrumentation Amplifier with Radio Frequency Interference Filter

sive differential filter at the input to the instrumentation amplifier (Kitchin et al., 2003).

Figure 5.2 shows the schematic diagram of the instrumentation amplifier stage. The RFI filter (inside the dashed box) has a differential bandwidth, $BW_{diff} = 1/(2\pi R_1(2C_2 + C_1))$ and a common mode bandwidth, $BW_{cm} = 1/2\pi R_1 C_1$. The common mode bandwidth should be kept below 10% of the unity gain bandwidth of the AD8221AR to sufficiently attenuate high frequency signals before they enter the instrumentation amplifier. The filter will reduce the CMRR due to mismatch between $R_{1A} \times C_{1A}$ and $R_{1B} \times C_{1B}$. The effect on CMRR can be reduced by making C_2 at least one order of magnitude higher than C_{1A} and C_{1B} . Unfortunately, maintaining a signal bandwidth of 20kHz (for ECochG) and setting C_2 at least one order of magnitude higher than C_{1A} and C_{1B} is impossible. This means the CMRR will be reduced by implementing this filter.

Provided contiguous shielding is used between the capacitive sensors and the enclosure, radio frequency interference may not be a problem. Performance should be tested without populating C_2 , C_{1A} , and C_{1B} , and fitting 0Ω jumper resistors in place of R_{1A} and R_{1B} . If high frequency rectification is deemed to be a problem then the filter can be implemented. C_2 , C_{1A} , and C_{1B} should be high-Q, low-loss components, with $\pm 2\%$ tolerance. Good choices are either mica or film capacitors. R_{1A} and R_{1B} should be metal film resistors with $\pm 0.1\%$ tolerance.

The gain of the AD8221AR is set by the single resistor R_G as shown in figure 5.2. The gain is calculated by the following equation:

$$G = \left(\frac{49.4k}{R_G} \right) + 1 \quad (5.2)$$

A gain of 10 can be set by solving for R_G , giving a resistor value of $5.489k\Omega$ for a gain of 10. $5.489k\Omega$ is not a readily available value, a $5.49k\Omega$ resistor with a $\pm 0.1\%$ tolerance should be used giving a maximum gain error of $\pm 0.09\%$.

Bypass capacitors (not shown in figure 5.2) should be applied from both the positive and negative supply lines to ground. These capacitors provide supply voltage stability, and filter high frequency interference on the power supply lines. $100nF$ ceramic capacitors should be positioned as close to the AD8221AR as possible to provide fast power supply currents to the amplifier. $10\mu F$ electrolytic capacitors should be placed in parallel with the $100nF$ capacitors, to provide low frequency currents. The position of the $10\mu F$ capacitors is not as critical as the $100nF$ capacitors, however keeping them close to the AD8221AR is preferable.

The instrumentation amplifier stage has theoretical gain of $9.998 \pm 0.009V/V$ giving a maximum gain error from $10V/V$ of 0.09% . The bandwidth without input filter is $562kHz$ (Analog Devices, 2011b). This will change to the differential

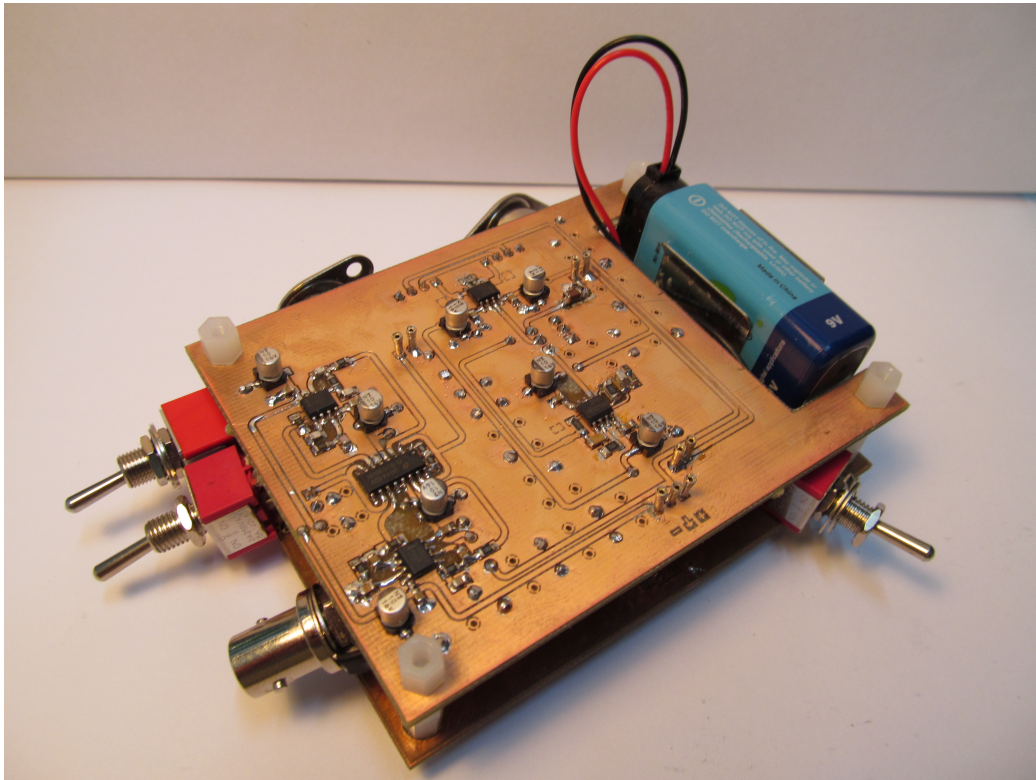


Figure 5.3: Differential Amplifier and Filters

bandwidth of the filter if it is implemented. The output impedance is not stated in the AD8221AR datasheet, but is likely to be low ($< 100\Omega$) since the output stage of the instrumentation amplifier is an operational amplifier. The AD8221AR can be operated with a power supply voltage from $\pm 2.3 - \pm 18\text{V}$ and has maximum power dissipation of 200mW. If operated from a $\pm 12\text{V}$ supply the maximum output current with a $10\text{k}\Omega$ load will be 1.08mA, the quiescent current is 0.9mA, and the output short circuit current is 18mA.

The instrumentation amplifier was built onto a PCB (along with the anti-aliasing filters – see Section 5.2.3) as shown in Figure 5.3, and its output checked for DC offsets due to RFI. No significant offsets were discovered, so the input differential filter was left out. The amplifier was integrated into the final system and the CMRR was measured.

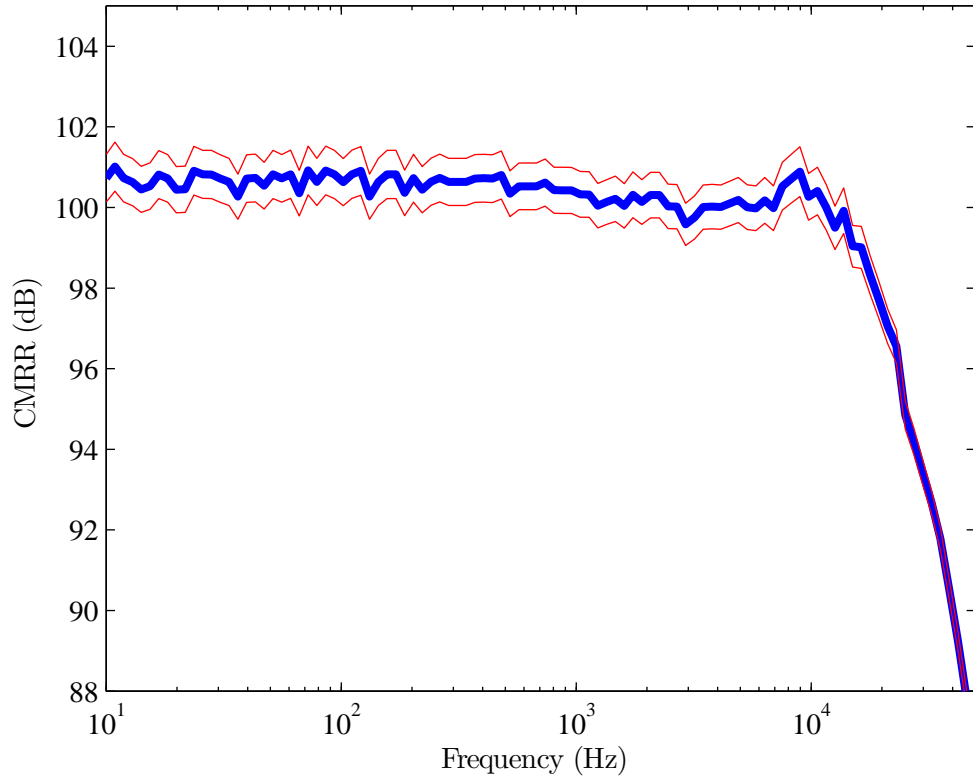


Figure 5.4: CMRR for bio-potential amplification system

Figure 5.4 shows the measured CMRR of the system. The blue trace is the experimental data, and the red traces show the bounds of the measurement error calculated using the method defined in ISO (1995). It can be seen that the system achieves a CMRR of greater than 100dB up to a frequency of 10kHz. This exceeds the specification set out in (5.1).

5.2.3 Anti-Aliasing Filters

This section details the design of anti-aliasing (AA) filters to prevent aliasing upon digitisation.

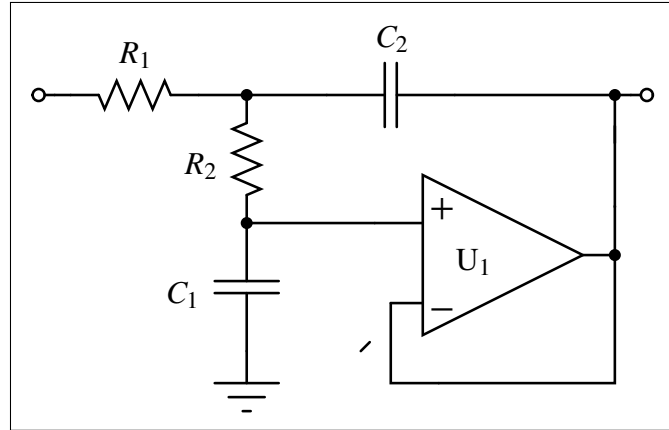


Figure 5.5: Anti-Aliasing filters: 2nd Order Salen Key low pass filter stage. Two stages are cascaded together to create 4th order Bessel filters

The DSO-X 2024A oscilloscope adjusts its sample rate according to the horizontal time setting. For 1s/Div the sample rate is 1.25 kHz, and at 10ms/Div it is 125 kHz, thus some filtering prior to acquisition is required to minimise the effects of aliasing. Two 4th order bessel filters with cut off frequencies of 500Hz, and 50kHz were designed to provide AA filters for long time periods, and short time periods respectively.

Figure 5.5 shows the 2nd order salen key topology used to build the filters. Each filter combines two of these stages with component values determining the filter response and cut off frequency. The TL072 low noise dual op amp was used for U_1 . The 500Hz filter was implemented with the following component values:

Stage 1:

$$R1 = 2.32\text{k}\Omega$$

$$R3 = 2.32\text{k}\Omega$$

$$C1 = 100\text{nF}$$

$$C2 = 100\text{nF}$$

Stage 2:

$$R1 = 3.24\text{k}\Omega$$

$$R3 = 3.24\text{k}\Omega$$

$$C1 = 100\text{nF}$$

$$C2 = 39\text{nF}$$

The 50kHz filter was implemented with the following component values:

Stage 1:

$$R1 = 2.32\text{k}\Omega$$

$$R3 = 2.32\text{k}\Omega$$

$$C1 = 1\text{nF}$$

$$C2 = 1\text{nF}$$

Stage 2:

$$R1 = 3.24\text{k}\Omega$$

$$R3 = 3.24\text{k}\Omega$$

$$C1 = 1\text{nF}$$

$$C2 = 390\text{pF}$$

Switching between these filters was accomplished using the DG444DY analog switch. A switch on the front panel selects the DG444DY configuration by controlling the voltage at the logic control pins for each switch. This allowed the

Table 5.1: Maximum amplitude and frequency range of bio-potentials (AD Instruments, 2009; Masood et al., 2012)

Bio-Potential	Amplitude (max)	f_{low} (Hz)	f_{high} (Hz)
ECG	10-20mV	0.3	200-1k
EEG	200-500 μV	0.1	200
EOG	200-500 μV	0.1	100
EMG	100mV	0.3	2k
ECochG	1 μV	20	20k

signal path to be altered without running the signals out to a switch on the front panel, preventing the possibility of picking up interference signals.

The power consumption of the DG444DY is very low at 22nW. The TL072 has a short circuit current of 60mA, and a quiescent current of 2.5mA. Considering only two op amps can be on at the same time, whilst the other two are in a quiescent state the total supply current under a short circuit event is 125mA.

5.2.4 High Gain Amplifier

This section details the design of the high gain amplifier stage. The gain and bandwidth required is specified based on the amplitude and frequency range of the bio-potential signals to be measured. Maximum gain error is defined based on suggested errors for bio-potential amplifiers and used to specify component tolerances.

Table 5.1 shows the amplitude and frequency range of common bio-potential signals. In order to obtain recordings of these small amplitude signals, low noise, low error, and high gain amplification is a necessity. Due to the varying amplitude between different bio-potentials, a range of amplification settings will be required.

The American Heart Association (AHA) suggest a minimum amplitude error

when acquiring ECG for data analysis of $\pm 2\%$ or $10\mu\text{V}$ (whichever is greater), and for visual display $\pm 5\%$ or $\pm 25\mu\text{V}$ (whichever is greater) Bailey et al. (1990). Considering the recommended errors, the quantisation error of the data acquisition device and the error of the amplification, a specification for minimum gain error can be reached. Expressing these errors as $\pm\%$ of amplitude the minimum acceptable gain can be calculated from (5.3)

$$A_{\text{error}} = \text{Error}_{\text{min}} - Q_{\text{err}} \quad (5.3)$$

where A_{error} = Minimum acceptable gain error, $\text{Error}_{\text{min}}$ = AHA recommended amplitude error, and Q_{err} = Quantisation error of data acquisition device.

The quantisation error in $\pm\%$ of fullscale voltage can be calculated using (5.4)

$$Q_{\text{err}} = \pm \frac{1}{2(2^M - 1)} \times 100 \quad (5.4)$$

where Q_{err} = Quantisation error of data acquisition device, and M = resolution of data acquisition device in bits.

The Agilent DSO-X 2024A has a Normal acquisition setting with 8bit resolution, and a High Resolution setting with 12bit resolution (Agilent Technologies, 2013b), giving $Q_{\text{err}} = \pm 0.2\%$ for Normal acquisition, and $Q_{\text{err}} = \pm 0.012\%$ for High Resolution acquisition. Using the error from the 8bit ADC, and the AHA recommended minimum amplitude error, the minimum acceptable gain error is:

$$\begin{aligned} A_{\text{error}} &= \pm 2\% - \pm 0.2\% \\ &= \pm 1.8\% \end{aligned} \quad (5.5)$$

Using a non-inverting amplifier the gain error is approximately the sum of the resistor errors in percentages. Using $\pm 1\%$ resistors will give an error of $\approx \pm 2\%$,

greater than our minimum error specification. On top of the tolerance error; temperature co-efficients, component aging, and PCB parasitics will conspire to increase the gain error. To satisfy the minimum gain error, $\pm 0.1\%$ resistors, with low temperature co-efficients should be used, giving a gain error of $\approx \pm 0.2\%$

In order to achieve the stated quantisation error, the bio-potential signal needs to span the full range of the data acquisition device. The DSO-X 2024A has a minimum fullscale voltage of 32 mV (Agilent Technologies, 2013b), therefore to utilise the full range of the oscilloscope, pre-amplification is needed for all bio-potentials apart from the EMG. (5.6) defines the gain required to scale bio-potential signals to the fullscale voltage.

$$G_{\min} = \frac{V_{fs}}{V_{bp}} \quad (5.6)$$

where G_{\min} = gain to scale signals to the minimum fullscale voltage, V_{fs} = fullscale voltage and V_{bp} = amplitude of bio-potential

The gain from the instrumentation stage is 20 dB. This should be sufficient gain to view EMG signals. ECG signals will require further amplification, a gain of 40 dB will bring the ECG amplitude up to 100-200 mV, sufficient for viewing on an oscilloscope. EEG and EOG signals require even more amplification, a gain of 60 dB will give a peak amplitude of 500 mV. These gains can be achieved by creating a 20 dB gain stage, and a 40 dB gain stage, and connecting them through a multipole switch to give gains of 20 dB (single stage), 40 dB (single stage), and 60 dB (cascaded 40 dB — 20 dB).

Figure 5.6 shows the circuit diagram of a single gain stage. R_{in} for limiting the input impedance to the amplifier, reducing capacitive coupling to the input. R_1 and R_2 set the amplifier gain of $1 + \frac{R_2}{R_1}$. The offset nulling circuitry of R_{Trim} , R_3 , and C_1 is a variation of a design from Horowitz (1989). R_{Trim} is a 50 k Ω , 25 turn, trimming potentiometer for adjusting the input voltage to the nulling network. R_3

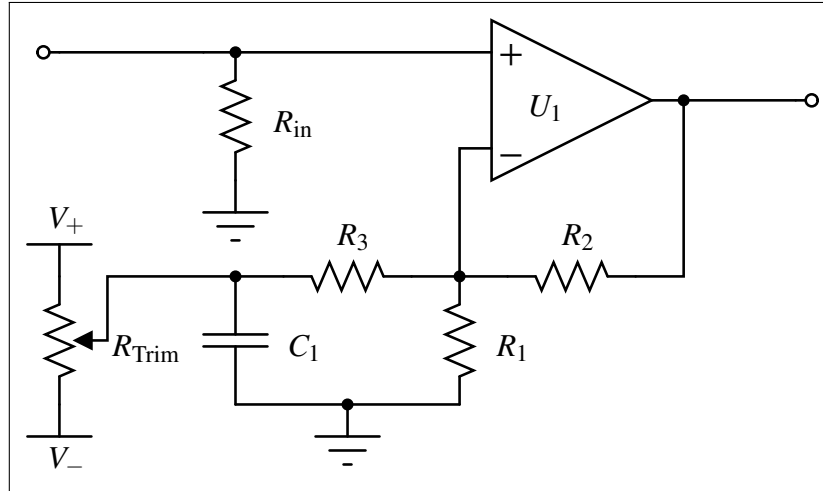


Figure 5.6: High Gain Stage where V_+ is the positive supply voltage, V_- is the negative supply voltage and U_1 is the AD8067 FET op amp from Analog Devices

attenuates the input voltage and couples the trim voltage to the inverting input. C_1 filters the trim voltage to remove any high frequency interference which maybe present on the power supply lines. The AD8067 op amp was chosen for U_1 as this part was already in the inventory, and was deemed to have suitable specifications. The AD8067 has a gain bandwidth product of 540MHz, $6.6\text{nV}/\sqrt{\text{Hz}}$ voltage noise spectral density and voltage offset of 1 mV maximum. Despite being a FET input amplifier the AD8067 has low offset voltage drift ($1\mu\text{V}/^\circ\text{C}$ typical) and the bias current variation is 25 pA from -40 to 85°C (Analog Devices, 2012).

To keep RMS noise to a minimum, the bandwidth of the gain stage should be kept as small as possible. To achieve this a 2nd order low pass bessel filter was implemented between the instrumentation amplifier and the gain amplifiers. The cut off frequency of the filter was set to 100kHz to ensure a flat response across signal frequencies.

The AD8067 has an output current of 26mA, giving a total output current for

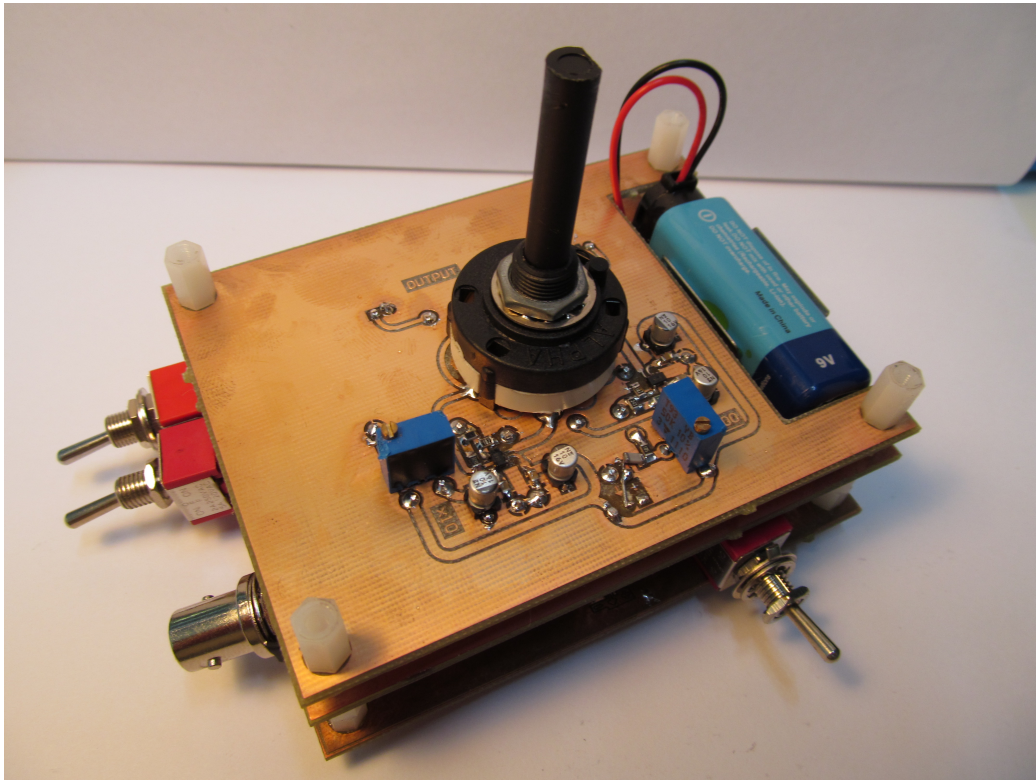


Figure 5.7: High Gain Stage

this stage of 52 mA.

The circuit was built onto a PCB and its performance was measured. The gain amplifier was initially found to be oscillating, even with the input shorted. These oscillations were discovered to originate from the long trace connecting the bandwidth limiting filter to the input of the gain amplifier. The oscillations were removed by placing a single pole RC lowpass filter directly at the input to the high gain stage.

The high gain stage was integrated into the system as shown in Figure 5.7, and the frequency response of the each gain settings were measured giving the results in Figure 5.8. The high frequency roll off is due to the anti-aliasing filters discussed in the following section. Other than this high frequency attenuation, the

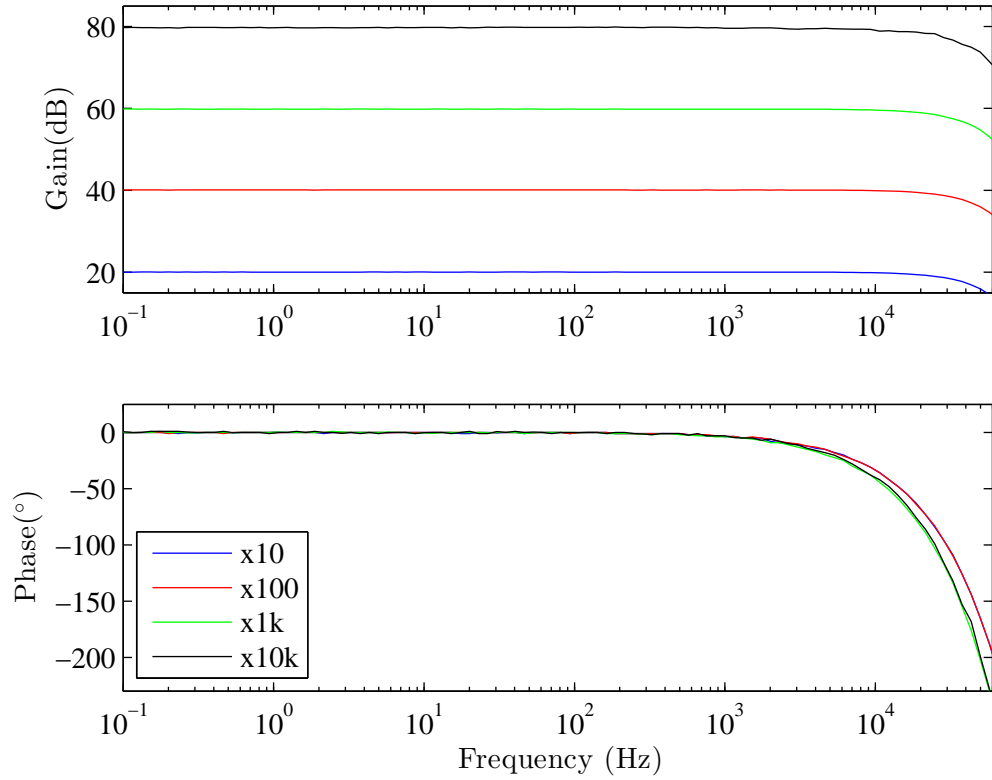


Figure 5.8: Frequency response of amplifier at different gain settings

Table 5.2: Summary of system gain accuracy

Gain (dB)	AVG Gain (V/V)	Flatness – 1 kHz ($\pm\%$)	Flatness – 20 kHz ($\pm\%$)
20	10.02	0.12	3.5
40	100.6	0.06	3.4
60	975	0.17	4.6
80	9583	1.73	7.2

gain and phase are very flat across the passband. The average gain and passband flatness for 1 kHz and 20 kHz are given in Table 5.2.

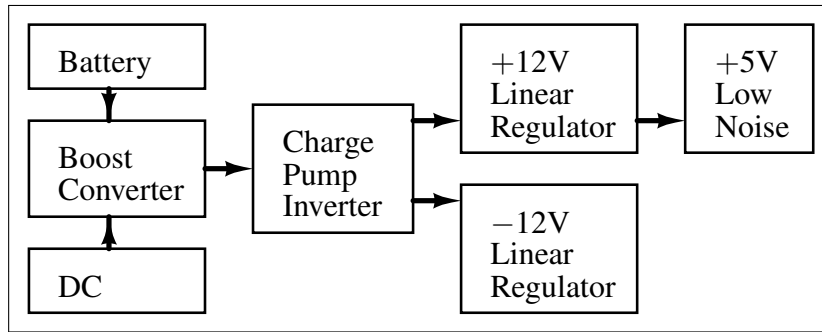


Figure 5.9: Block diagram of system power supply

The maximum acceptable gain error was defined as $\pm 1.8\%$. All the gain settings, except 80dB are below this error over the 1kHz passband. However none of the gains achieve this specification over the 20kHz passband, due to attenuation by the 50kHz anti-aliasing filter. Future revisions could increase the cut off frequency of this filter or apply a higher Q filter, to prevent passband attenuation. If the frequency is increased care should be taken when digitising that the sample rate is sufficiently high to reduce the effects of aliasing.

5.2.5 Power Supply

This section presents the design of the power supply for the differential amplifier, and non-contact bio-potential sensors.

Adding the power supply currents from all the stages the maximum current (with the outputs of all sub circuits shorted) is 195mA. The actual current which will be drawn will be significantly less than this, so a 9V battery supply should be sufficient, although some provision for external DC power should be made.

To provide sufficient headroom for the amplifier circuitry a $\pm 12V$ power sup-

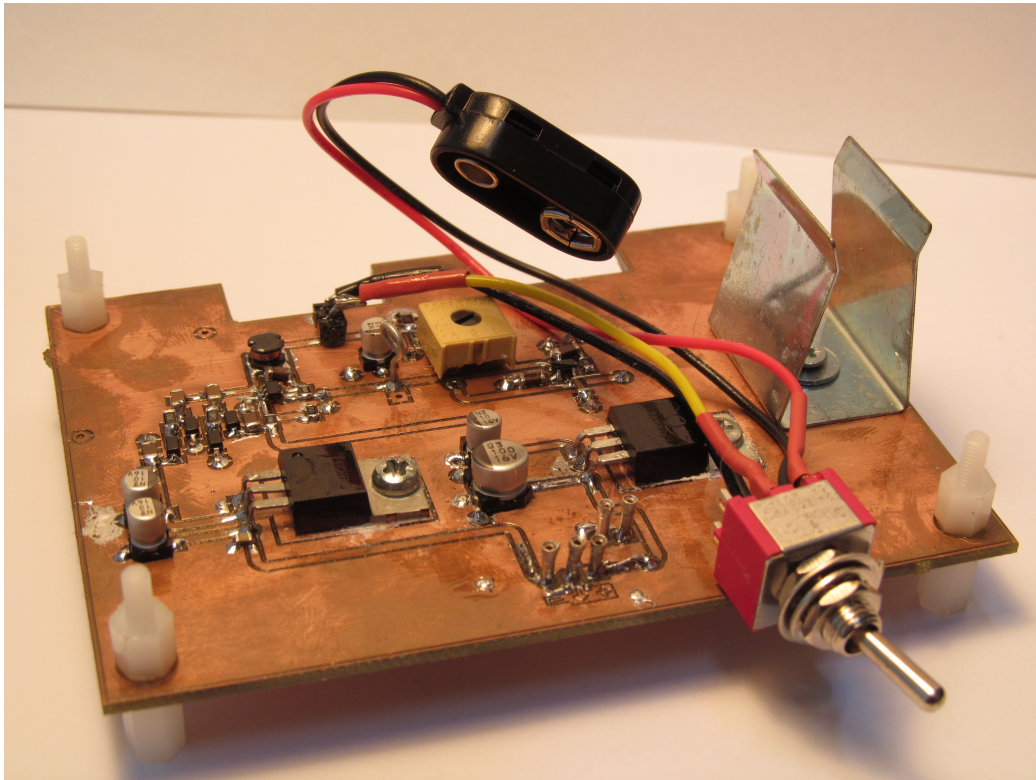


Figure 5.10: Differential Amplifier Power distribution circuit

ply was chosen. To generate these voltages from a single 9V battery a combination of a boost converter and a charge pump inverter was used, with linear regulators applied to the output of the charge pump inverter to reduce any ripple from the switching power stage. A low noise 5V supply was derived from the 12V regulator to provide power to the sensors. Figure 5.9 shows a block diagram of the proposed power supply.

The LMR62014 boost converter was used to increase the voltage from the 9V battery/DC supply to 15V. The 15V was feed into the charge pump inverter to generate $\pm 15V$ outputs. The positive supply was feed into a 7812 linear regulator, and the negative to a 7912 linear regulator to generate the $\pm 12V$ supply rails for the amplifier circuitry. The positive 12V was fed to the LT1461 low noise 5V reference, to provide power to the non-contact sensors. Figure C.5 shows the

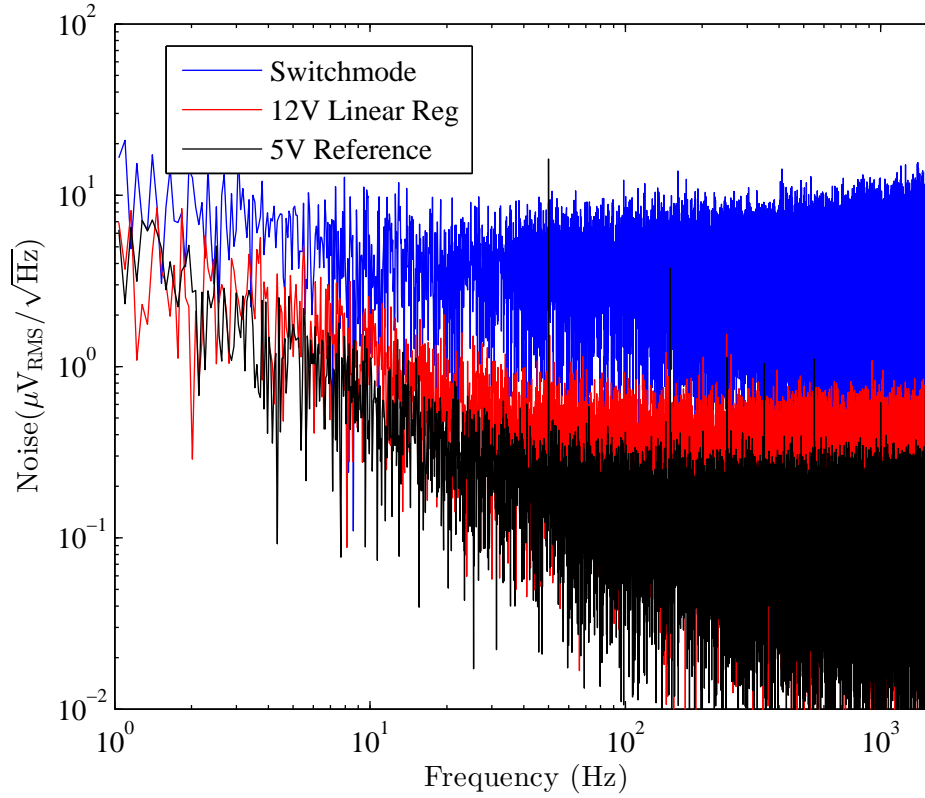


Figure 5.11: Voltage noise spectral density of power supply outputs

schematic diagrams of these power supply circuits.

The power supply was built on a PCB as shown in Figure 5.10. The output noise spectral density was measured for the output of the charge pump inverter, the 12V regulator, and the low noise 5V supply. Figure 5.11 shows these measurements. It can be seen that the noise becomes increasingly smaller at each stage of regulation.

Electromagnetic interference from the switching power supply was preempted and provisions made for adding a shield to encase the circuit. Interference at the switching frequency was found to be present at the output of the amplifier, and

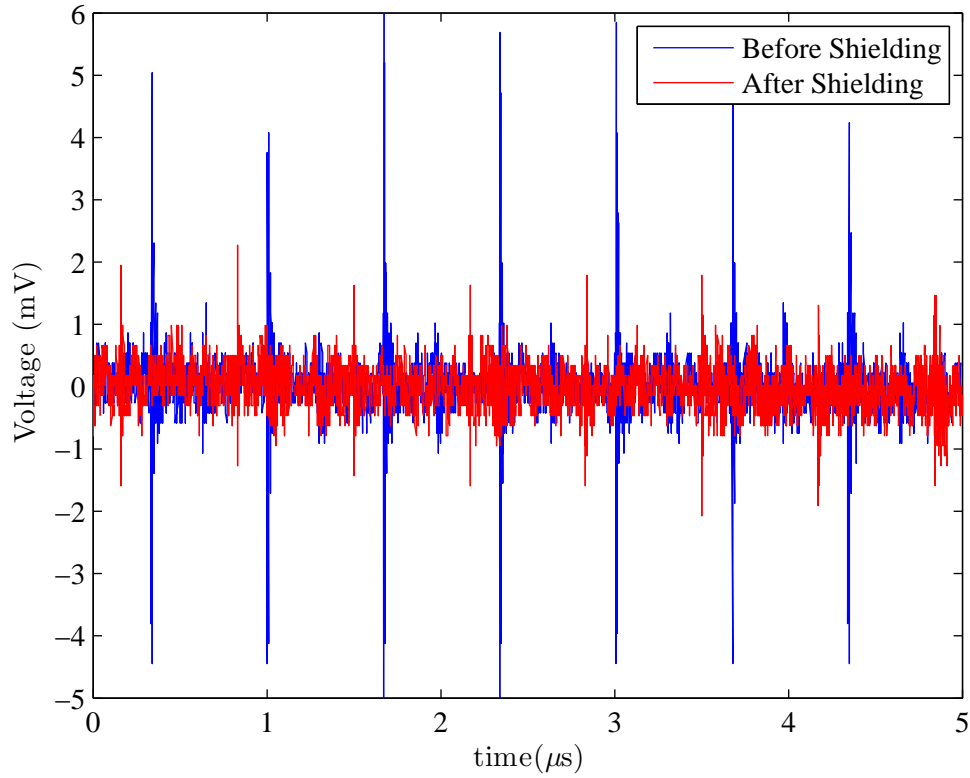


Figure 5.12: Power supply interference at the output before and after shielding of switchmode power supply

thus the shield was implemented. Figure 5.12 shows the comparison of this interference before and after applying the shield. It can be seen that applying the shield significantly reduces the level of interference at the output.

5.2.6 Enclosure Design and System Integration

A custom enclosure for the differential amplifier was built from an aluminium instrument rack case. The front and back panels were made from laser cut acrylic and coated with nickel on the inside, to provide shielding from EMI. Figure 5.13

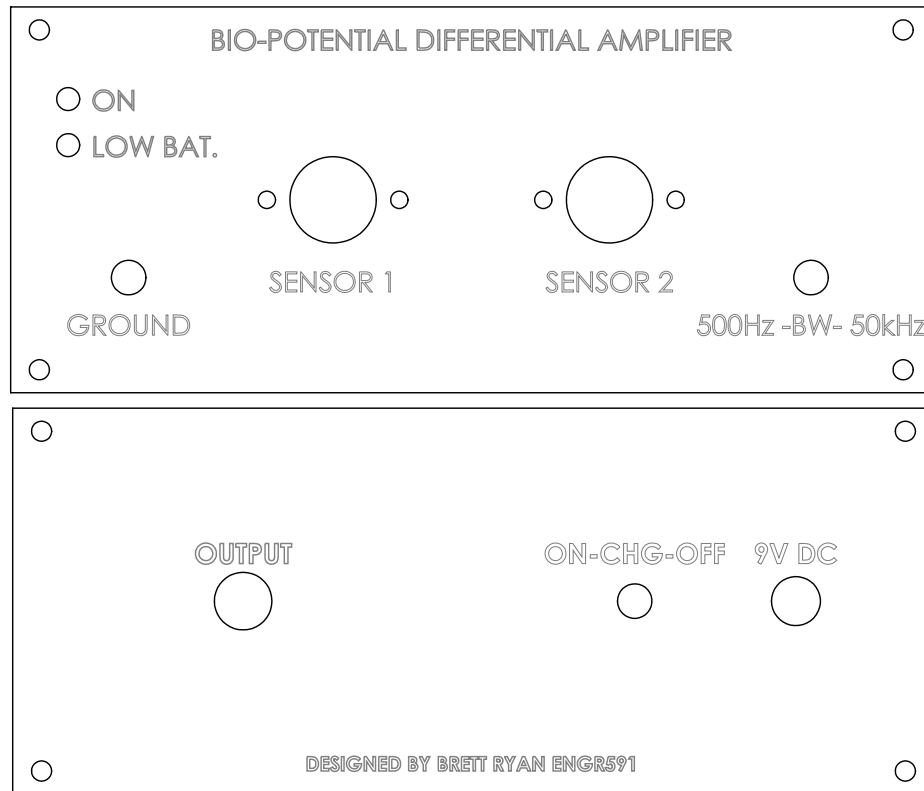


Figure 5.13: Amplifier enclosure panels designed in Solidworks. The front panel is shown at the top, and the back panel at the bottom

shows the front and back panel designs. Figure 5.14 shows the completed amplifier enclosure, with the non-contact sensors (developed in Chapter 6) connected to the inputs.

The input voltage noise spectral density of the differential amplifier was measured for each gain setting. These results are presented in Figure 5.15. The theoretical noise was calculated from simple noise models of the op amps used throughout the circuit. Each op amp has a $1/f$ noise, and a white noise component. The experimental data matches very well with the predictions. This shows that

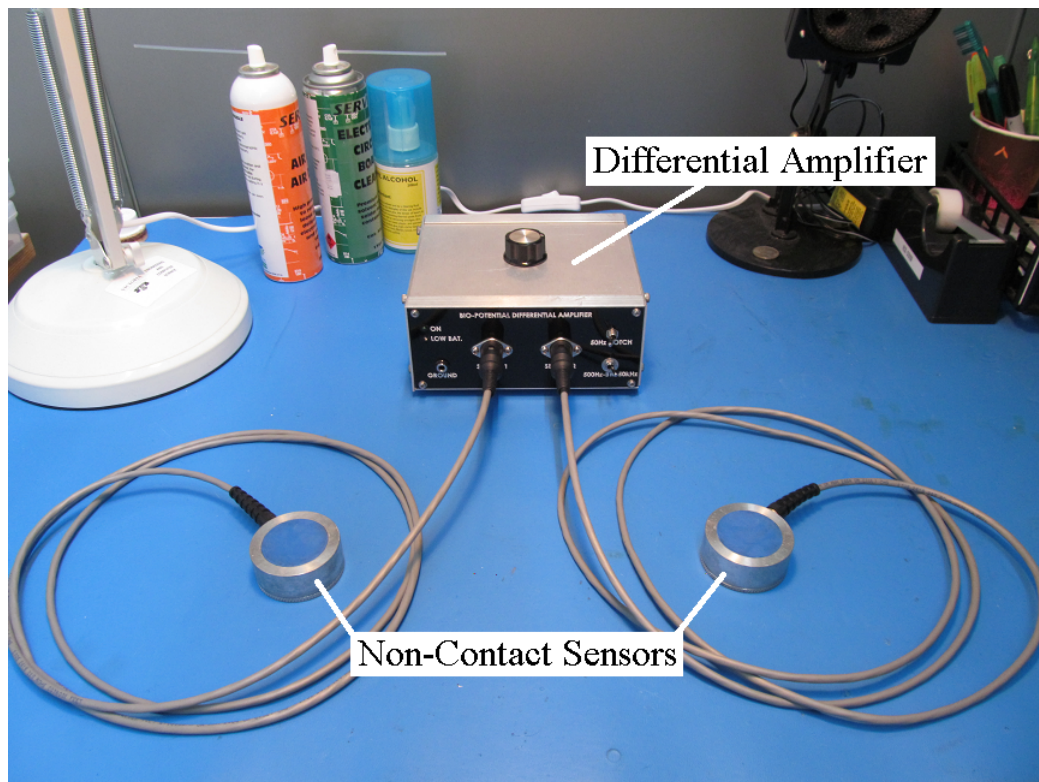


Figure 5.14: Completed differential amplifier with non-contact sensors connected to the inputs.

there is no excess noise being added to the circuit by poor PCB layout, and the thermal noise from passive components is minimal.

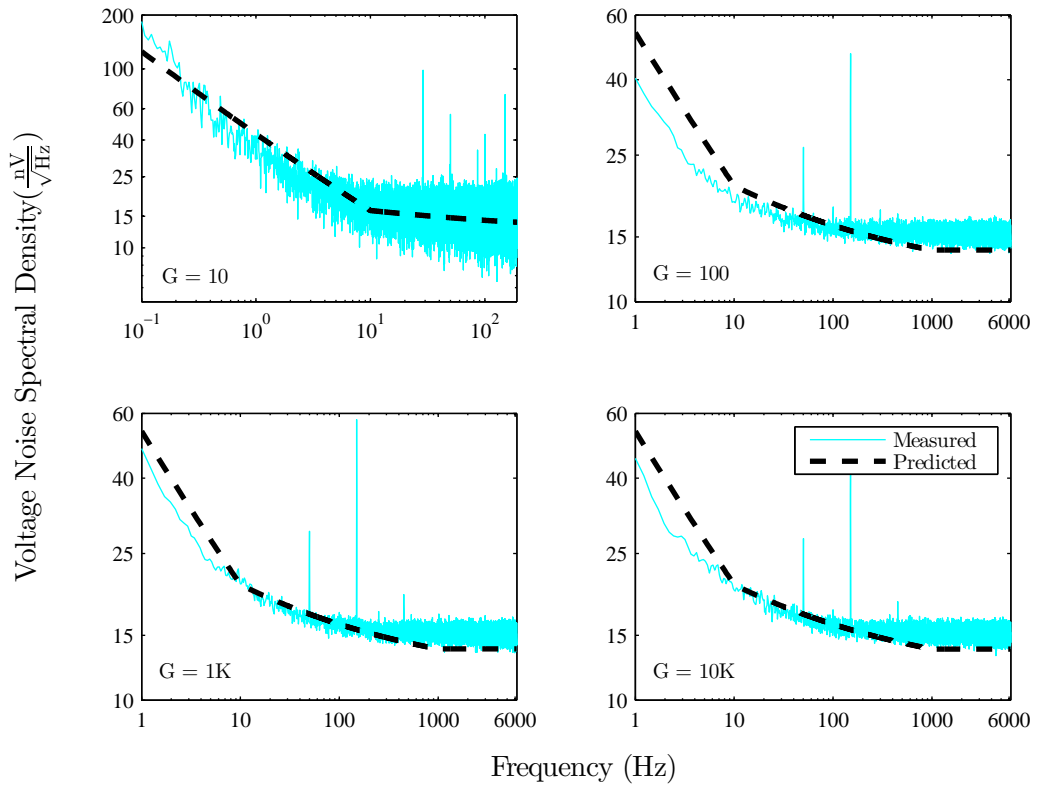


Figure 5.15: Input voltage noise spectral density of differential amplifier for different gains. The theoretical noise is plotted as a dashed line over the experimental data.

Chapter 6

Sensor Design

This section presents the design and evaluation of the capacitive bio-potential sensors. The design development is presented in three sections representing the separate problems to be solved; electrode plate, high impedance biasing, and input capacitance neutralisation.

6.1 Overview

The capacitive bio-potential sensor is required to sense the electric potential present at the surface of the body, without making ohmic contact to the skin. Bio-potentials originate from electrochemical reactions inside cells. These potentials travel through tissue, and skin to the exterior of the body, and on out into the environment where the sensor measures the electric potential. This path between the cell and the sensor can be modelled as an electrical circuit. The body represents a resistance; the stratum corneum layer of the skin, a parallel capacitor and resistor; and the gap between the skin and sensor, a capacitance (Chi et al., 2010a). All these elements add in series, creating a very large impedance between the source of potential and the sensor input. For a sense of the magnitude of this impedance, considering only the capacitance between the skin and the sensor input (typically 10pF) gives an impedance of magnitude $\approx 1\text{G}\Omega$ at 10Hz (Spinelli and Haberman, 2010). This large source impedance imposes most of the constraints for the sensor design.

The source capacitance and the input resistance of the sensor will form a high pass filter, limiting the low frequency response. With a 1pF source capacitance, to achieve a response down to 0.1Hz requires an input impedance of $\approx 1.6T\Omega$. Only ultra-low leakage FET input op amps achieve input impedances of the order of $T\Omega$ s, thus the sensor requires an amplifier of this type to achieve the low frequency response. As the source impedance is capacitive, a DC current path to the input is required to avoid the input bias current of the amplifier charging the input, and thereby saturating the sensor. The impedance of this bias network adds in parallel with the amplifier's input impedance, thus the bias network is also required to be of the order of $T\Omega$ s to achieve the low frequency response.

Input transients from power switching and static discharge will cause the sensor output to shift from its DC bias point, which after amplification could easily saturate the output signal, resulting in the loss of bio-potential information. The source capacitance and input resistance form time constants in the tens of seconds, which means the signal could remain in saturation for an unacceptably long period of time. If the sensor is saturated for long periods of time, the bio-potentials cannot be monitored. Furthermore when first applying the sensors, static charges create a large transient which can saturate the sensors. Thus verifying sensor positioning could be a long and frustrating process.

The capacitive component of the sensor's input impedance will be of the same order as the source capacitance, forming a capacitive divider at the input. This capacitive divider will severely attenuate the signal at all frequencies (if $C_s = C_{in}$ the source will be attenuated by -6dB at the input). Furthermore the source capacitance will change as the distance between skin and electrode changes, resulting in fluctuating attenuation. This fluctuating attenuation transduces mechanical actions into electrical signals, adding interference to the bio-potential signal.

Considering the previous discussion the design problems to be solved in ca-

capacitive bio-potential sensors are defined as follows:

1. High Impedance Input Biasing — to maintain low frequency response
2. Low Settling Time — to limit time in saturation due to input transients
3. Low Input Capacitance — to limit attenuation and mechanical interference

Problems 3 and 1 relate to signal fidelity, and problem 2 relates to the usability of the sensors. In addition to the primary problems (1 - 3) the following design problems also need to be solved:

4. Low Noise Biasing — to keep noise levels below the small input signals
5. High Source Capacitance — to decrease mechanical coupling and maintain low frequency response
6. Directional Sensing — to limit interference from external electric fields
7. Low Power Operation — to increase battery power time and allow use of low noise precision voltage references

Problem 7 will be considered when making component selections, problem 3 is addressed in section 6.5, problems 1, 2 and 4 will be addressed in section 6.4, and problems 5 and 6 in section 6.3. The following section presents the design of the amplifier circuitry of the sensor.

6.2 Amplifier Design

The topology of the sensor is based on the non-contact sensors outlined by (Clippingdale et al., 1994), and (Prance et al., 2000). Figure 6.1 shows a block diagram of the sensor topology. The sensor consists of an insulated electrode, and an electrometer grade (bias current < 1 pA) amplifier; with input biasing and capacitance neutralisation circuitry. The design of the insulated electrode is covered in section 6.3, the input biasing circuitry in section 6.4, and the capacitance neutralisation in

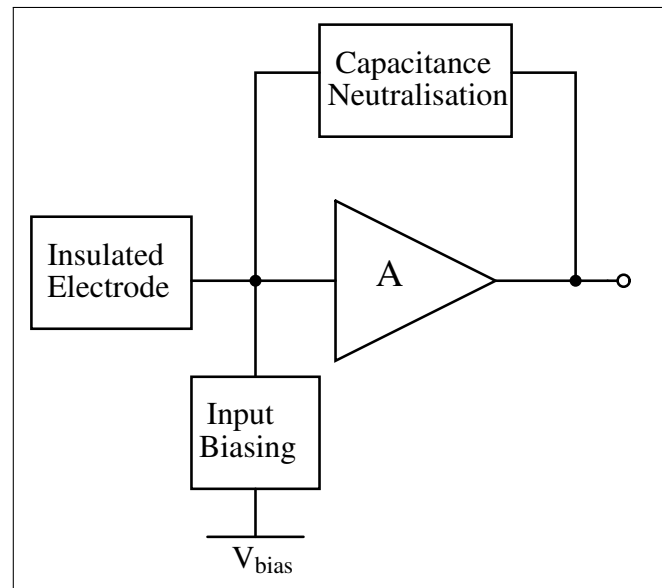


Figure 6.1: Block Diagram of Sensor System

section 6.5. This section covers the selection of the sensor amplifier, and the gain of the sensor. Critical amplifier specifications, and power supply requirements are used to select an appropriate amplifier to form the basis of the non-contact sensor.

The amplifier must have a very low input bias current, and very high input impedance to avoid loading errors due to the high impedance of the insulated electrode. A high CMRR ($>90\text{dB}$) is beneficial to reject common interference potentials. Input current noise will flow through the large source impedance, thus to keep the total noise low, low input current noise is essential. In order to maintain very low bias currents, on board guarding to minimise leakage current paths is essential. The amplifier IC pinout should be arranged so that the input pins are far away from power supply pins, and have sufficient space around them to implement a guard ring.

The two amplifiers which best match these specifications are the Burr Brown

R_G	1		16	R_G
Guard–	2		15	NC
V_{-IN}	3		14	NC
Guard–	4		13	V_+
Guard+	5	INA116	12	NC
V_{+IN}	6		11	V_O
Guard+	7		10	NC
V_-	8		9	Ref

Figure 6.2: Pinout of INA116 showing on chip guard pins surrounding the inputs. The pins labeled Guard– are driven from a unity gain buffer with V_{-IN} as the input. The Guard+ pins are driven from a unity gain buffer with V_{+IN} as the input

INA116 (now from Texas Instruments), and the National Semiconductor LMP7721 (also now from Texas Instruments). The INA116 claims a typical input bias current of 3 fA, and ± 25 fA max, input current noise at 1 kHz of $0.1 fA/\sqrt{Hz}$, CMRR of 89 dB at a gain of 1, and most attractively an on chip guarding scheme (Texas Instruments, 1995). The on chip guarding scheme consists of integrated input buffer amplifiers which drive dedicated guard pins either side of both inputs (see figure 6.2 for the INA116 pinout). This allows easy implementation of a guarding around the inputs, as well as providing some guarding internal to the IC, further reducing leakage currents.

The LMP7721 claims a typical bias current of 3 fA, and ± 20 fA max, input current noise at 1 kHz of $10 fA/\sqrt{Hz}$, CMRR of 100 dB at a gain of 1, and comes in an 8 pin SOIC package with the inputs and power supply pins located at opposite ends of the package (Texas Instruments, 2008).

When attempting to measure small potentials with large source impedances the input current noise provides a significant contribution to the total input noise of the amplifier. The INA116 has input current noise which is 100 times smaller

than the LMP7721, however the voltage noise of the INA116 ($200\text{ nV}/\sqrt{\text{Hz}}$) is much higher than that of the LMP7721 ($6.5\text{ nV}/\sqrt{\text{Hz}}$). For a 10pF source capacitance, at frequencies $>800\text{Hz}$, the LMP7721 will have lower total input noise than the INA116. While most bio-potentials exist below 800Hz, for ECoG measurements the bandwidth is over the entire audio range, making higher frequency noise performance essential to acquiring high fidelity signals.

The sensor must be implemented on a very small PCB, thus the size of the amplifier footprint is an important consideration when making a selection. The LMP7721 comes in an 8 pin SOIC package and the INA116 in the significantly larger 16 pin SOIC.

The INA116 operates from a dual power supply of $\pm 4.5\text{ V} - \pm 18\text{ V}$, whereas the LMP7721 can operate from a single supply of $1.8\text{ V} - 6\text{ V}$. The lower voltage, and single supply operation of the LMP7721 simplifies power supply generation and distribution. Power supply generation is simplified because a single, low noise, $+5\text{ V}$ reference voltage can be used to power the sensor. Distribution is simplified because only a positive supply voltage and ground wire need to be connected to the sensor to provide power.

Despite the better input current noise specifications of the INA116, the smaller size, lower power operation, better high frequency noise performance, guard friendly IC package, and ultra low input bias current of the LMP7721 make it an excellent choice for implementing a non-contact bio-potential sensor.

The input amplifiers in non-contact sensor designs are often configured to amplify the input signal. Chi and Cauwenberghs (2009) include a gain of 11 at the input amplifier to improve the signal to noise ratio of the sensor. Clippingdale et al. (1994) keep the input amplifier gain at unity, with a subsequent gain of 11 to drive the cables which connect the sensors to the acquisition device. Providing gain at the sensor has the primary benefit of increased signal to noise ratio,

however there are some negative effects produced by increasing the gain. As was mentioned in section 6.1, fluctuations in source capacitance create voltage fluctuations at the input to the sensor. As these fluctuations are specific to individual sensors, they will not be rejected by differential amplification. Thus increasing the gain of the sensor results in higher levels of interference in the differential bio-potential signal, possibly negating any signal to noise improvements. For this reason the amplifier was configured as a unity gain buffer. Implementing the sensor amplifier as a unity gain buffer, rather than a non-inverting amplifier with gain, also removes the gain dependence on external resistors. This means matching the gain of pairs of sensors does not rely on precise components, reducing the CMRR degradation at the differential amplifier.

This section has defined the non-contact bio-potential sensor topology. Centered around a unity gain buffer with high input impedance, implemented with the LMP7721 op amp, the sensor takes its input from an insulated electrode. Input bias stability is provided through a high impedance biasing network, and input capacitance is reduced through capacitance neutralisation circuitry. The sensor is powered by a +5V, low noise, voltage reference (see section 5.2.5 for details of the power supply design). The following section details the design of the insulated electrode.

6.3 Electrode Design

This section describes the design of the sensor's electrode. Theoretical models, informed by physical constraints are used to investigate the performance of capacitive sensor electrodes. The theoretical response, and consideration of the intended applications are then used to make decisions about the design of the electrode. Guarding and shielding techniques to add directionality are discussed, and the electrode design presented.

The source impedance of the sensor can be thought of as a parallel plate ca-

pacitor. The sensor electrode forms one of the plates, the insulating material forms the dielectric, and the body of the patient forms the other plate. The capacitance of this configuration (provided the dimensions of the plates are larger than the distance between them) can be approximated using the model of a parallel plate capacitor:

$$C = \epsilon_r \epsilon_0 \frac{A}{d} \quad (6.1)$$

where C is the source capacitance, ϵ_r is the relative permittivity of the insulating material, ϵ_0 is the permittivity of free space, A is the Area of the electrode, and d is the distance between the electrode and the body. At distances much greater than the electrode dimensions the source capacitance approaches a minimum. This minimum is defined by the self capacitance of the electrode which for a circular disc is given by:

$$C_{\text{self}} = 8\epsilon_r \epsilon_0 r \quad (6.2)$$

where r is the radius of the circular electrode.

From (6.1) the parameters which can be altered are; the dielectric between the electrode and the body, the area of the electrode plate, and the distance between the body and the electrode plate. Early work on capacitive bio-potential sensors focused on creating electrodes with a high permittivity insulation layer to increase the source capacitance (see Section 2.4). These high source capacitances reduced the input impedance requirements to maintain low frequency response. Unfortunately these high permittivity electrodes all suffer from a critical flaw; if the sensor becomes detached from the skin, or the patient moves, reducing the surface area in contact with the skin, the coupling capacitance is severely reduced. The source capacitance model now becomes a series combination of parallel plate capacitors, one of which has air as the dielectric. With the relative permittivity of air being 1, and the capacitances combining in series, the increased capacitance from using a high permittivity material is quickly eroded as sensor to body separation increases.

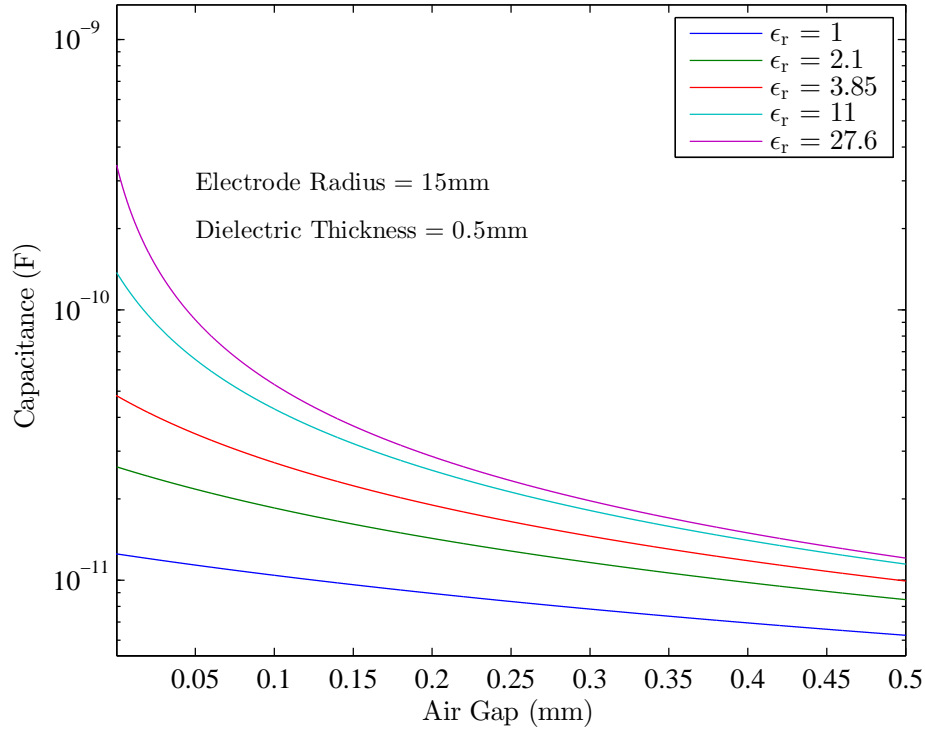


Figure 6.3: One capacitance is formed between the electrode plate and the edge of the insulation, with ϵ_r of 1 for air, 2.1 for teflon, 3.85 for paper, 11 for silicone, and 27.6 for anodised tantalum. The other capacitance is formed between the edge of the sensor and the body, with air as dielectric and distance plotted on y-axis.

Figure 6.3 uses the model of a series combination of parallel plate capacitors to show how the capacitance decreases as the sensor is moved away from the body. ϵ_r is the relative permittivity of the dielectric for various insulating materials. The dielectric thickness is set to 0.5mm (smaller thicknesses will give larger capacitances whilst in contact with the skin, but these require precise manufacturing equipment to be realised). With the electrode in direct contact with the skin, the capacitance ranges from 0.3 nF for anodised tantalum, to 12.5 pF for an air gap. As the air gap is increased the capacitances start to converge. With a 0.5 mm gap the range drops to 12 pF for anodised tantalum to 6 pF for an air gap. This shows

that high permittivity insulation is only beneficial when the sensor is in close contact with the skin.

The resistivity of the insulating material should be high to avoid making ohmic contact to the body, as well as minimising leakage currents which could flow through the insulation to the input. Silicone has a high resistivity, is easily applied to the electrode plate, and is chemically stable with salt water. Because of this silicone was decided upon for the insulating layer of the electrode. This layer will increase the body to electrode coupling capacitance when the sensor is in close proximity to the skin.

A simple metal disk electrode will have a capacitance to sources directly in front and behind of the electrode. In addition there will be capacitance to sources which are not directly in front or behind the plate. These capacitances are due to the sensing field extending around the edges of the plate, known as fringing effects (LION Precision, 2006). To create an electrode which only senses electric potentials directly in front of it, the electrode must be guarded against extraneous electric potentials. The guard potential is driven to match the potential at the electrode, so that no current can flow between the guard and the electrode input. The guard should cover the back of the electrode to prevent coupling to sources behind the electrode, and surround the front of the electrode to limit fringing effects.

In addition to guarding shielding was also included on the electrode to further reduce interference at the sensor input. The shielding on the electrode is made around the outside edge so that a connection can be made to the sensor enclosure, providing the sensor with contiguous shielding. Figure 6.4 shows the electrode design with and without the silicone insulating material, and Figure 6.5 shows the back of the electrode.

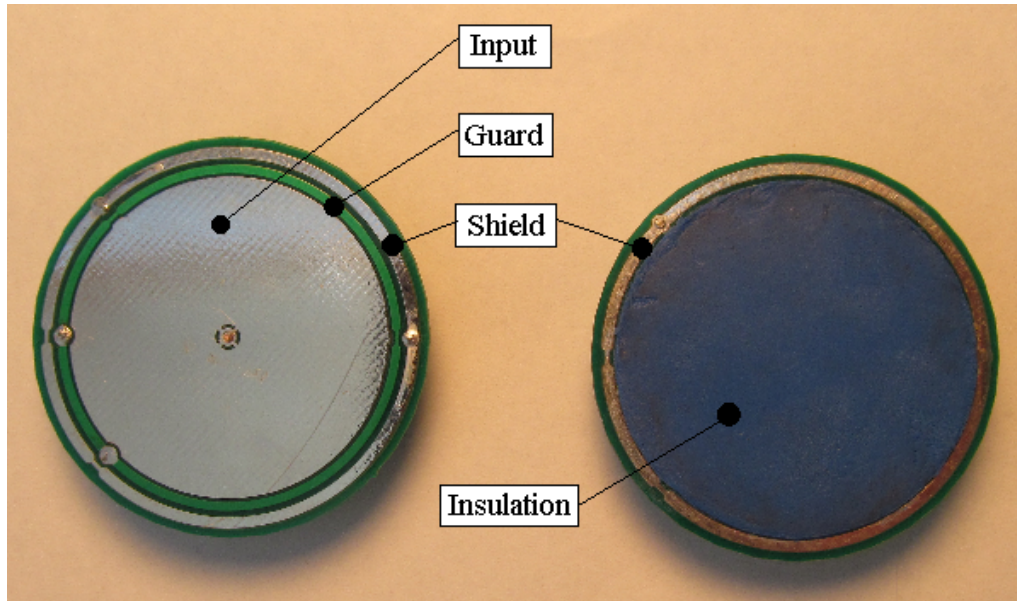


Figure 6.4: Final Insulated electrode design: The electrode on the left has no silicone insulation, showing the shield, guard and input traces. The electrode on the right has been insulated, with the shield left exposed for connection to the sensor enclosure.

6.4 High Impedance Biasing

This section presents the design of ultra high impedance input biasing networks. Several topologies are investigated and their high impedance operation verified through circuit analysis, simulation and prototype testing.

6.4.1 Overview

Many high impedance biasing schemes have been realised, using bootstrapped resistors (Lanyi and Pisani, 2002), back to back low leakage diodes (Lopez and Richardson, 1969), anti-parallel diodes (Chi et al., 2009), and even a scheme with no explicit biasing element (Prance et al., 2000). Apart from the bootstrapped anti-parallel diodes, these schemes have no mechanism to quickly return the input

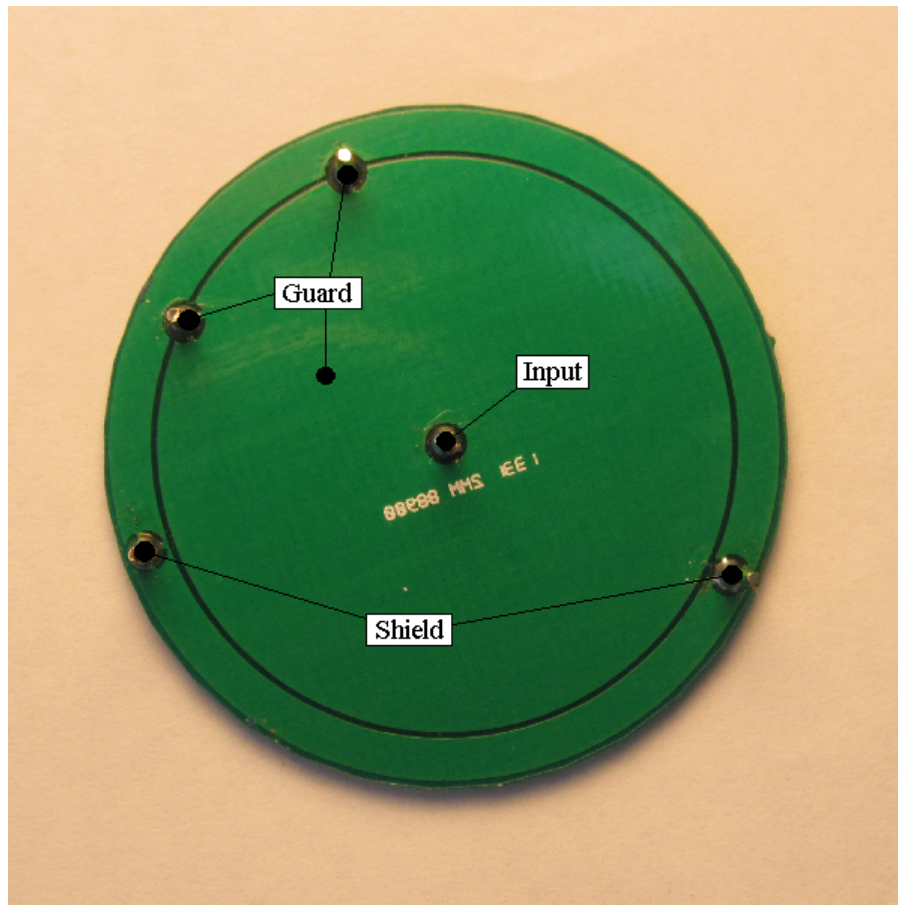


Figure 6.5: Final Insulated electrode design: Back side of electrode showing how the guard covers the sensing plate.

to its bias level after an input transient event. A scheme to quickly return the input to its bias voltage was presented by Sullivan et al. (2007), but the low frequency response (down to $\approx 1\text{Hz}$) achieved by this scheme is unacceptable for obtaining EEG or ECG measurements. The following sections present the development of an input biasing topology which can provide the ultra high impedance necessary for low frequency operation, whilst minimising the time taken for the sensor to recover after input transient events.

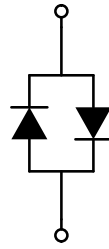


Figure 6.6: Anti-Parallel Diodes

6.4.2 Input Biasing with Anti-Parallel Diodes

This section explores the use of anti-parallel diodes as a high impedance input biasing element.

A pair of diodes connected in parallel, with the anode of one diode connected to the cathode of the other, and vice versa, are known as anti-parallel diodes (see figure 6.6). Using anti-parallel diodes as a biasing element is attractive for two reasons. The first being that provided the diodes are both biased in their cut off regions, and they have ultra low-leakage currents ($< 1\text{pA}$), the diodes will present a very high resistance ($> 50\text{G}\Omega$). This high resistance can replace conventional resistors which above $50\text{G}\Omega$ s are very expensive ($> \$100$), have wide tolerance ranges, are sensitive to temperature and humidity, and must be handled with extreme care as oils from the skin degrade the insulation, reducing the resistance (Grohe, 2011). The second attraction is that as the voltage across the diodes increases, the diode current increases approximately exponentially, lowering the effective input resistance. This means that input transient events, which shift the DC potential at the input away from the bias voltage, will reduce the input resistance, and thus the settling time of the circuit. As the input voltage nears the bias voltage the conduction will reduce, returning the anti-parallel diodes to a high impedance state.

For the anti-parallel diodes to function as a high impedance device, both diodes must be operated in their off state. In this state the conduction of the diodes is gov-

erned by their reverse leakage current. The lower this leakage current, the higher the effective impedance of the diodes. At the time of writing the diode with the lowest leakage current available is the PAD1 from Linear Integrated Systems with a specified leakage current of 1 pA (Linear Integrated Systems, 2001). The capacitance of the diode is also important, as this adds to the total input capacitance, which increases the attenuation at the input. The PAD1 has a very low capacitance of < 0.8 pF. To create the anti-parallel diode, two PAD1 diodes are required, thus the total capacitance is double that of a single PAD1 device. The PAD1 comes in a TO-72 circular metal can package with a diameter of 5.55mm, including two of these diodes on the small PCB will put strain on the board layout. Another low leakage diode is the BAV199 from NXP semiconductors. The BAV199 is a series connected pair of diodes, meaning a single device can be used to create the anti-parallel diodes. The BAV199 comes in the compact SOT-23 surface mount package minimising the PCB footprint. The leakage current of the BAV199 is 3 pA and the capacitance is 2 pF (NXP Semiconductors, 2001). Whilst the PAD1 out performs the BAV199 in all the critical aspects, the BAV199 was chosen as it is more easily incorporated into a PCB, and inexpensive at \$0.38 per diode pair, compared to \$8.30 for a pair of PAD1 diodes.

The exponential current to voltage relationship of the anti-parallel diodes can be further exploited by applying an active bias voltage across the anti-parallel diodes. If the voltage across the diodes can be controlled, then so can the input impedance. The active bias voltage should set a high impedance state for the desired signal frequencies, and a low impedance state for frequencies below 0.1Hz. This can be achieved by using an inverting low pass filter connected from the output of the buffer amplifier to one end of the anti-parallel diodes (E.Deuss, pers. comm.).

Figure 6.7 shows the active biasing topology. C_S is the source impedance from the body to the electrode, D_1 is the BAV199 configured as an anti-parallel diode, U_1 is the LMP7721 op amp configured as a unity gain buffer, U_2 , C_1 , R_2 , and R_1

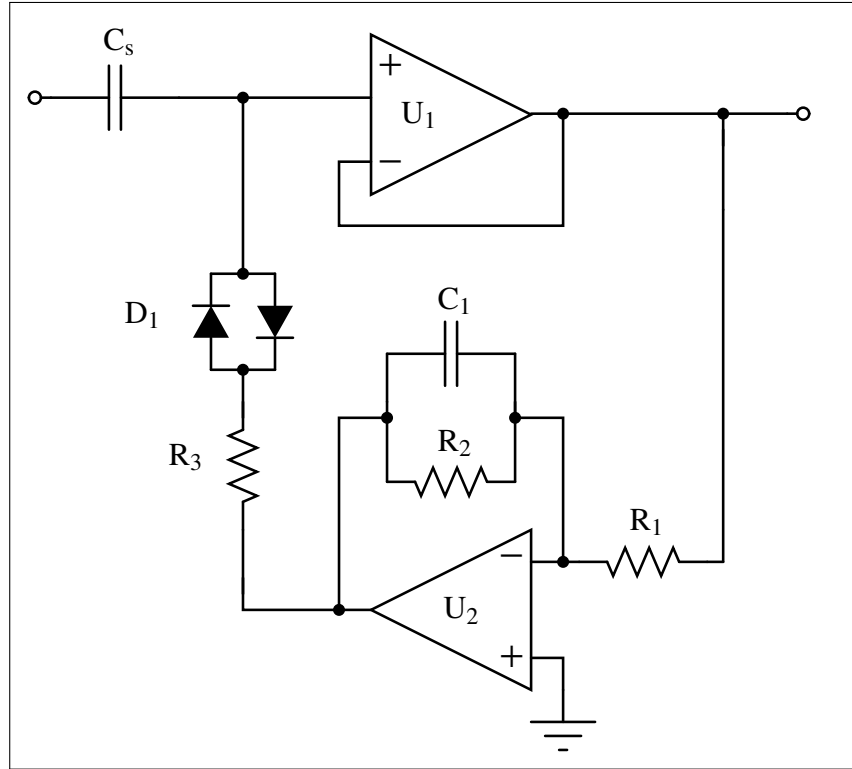


Figure 6.7: Anti-Parallel Diode Active Biasing Circuit. U_1 is the LMP7721 high impedance buffer amplifier, and U_2 is the LMP7715, a general purpose op amp configured as an inverting low pass filter. Ground is the circuit reference voltage, in this case $V_{CC}/2 = 2.5\text{ V}$

form the inverting low pass filter, and R_3 can be used to increase the biasing resistance. The ground symbol is used to represent the circuit reference voltage, which for this single supply circuit is $V_{CC}/2$. The inverting low pass filter responds to low frequency voltages at the input, adjusting the voltage across D_1 and R_3 . If the input rises above $V_{CC}/2$ by 0.1 V , the inverting low pass filter (with a gain of -1) outputs a voltage $V_{CC}/2 - 0.1\text{ V}$. As the input approaches the desired bias level of $V_{CC}/2$, so too does the output of the inverting low pass filter. This drives the voltage across D_1 and R_3 towards 0 V , returning the diodes to a low conduc-

tion state. R_3 can be altered to give higher impedance if necessary, however large resistances will exhibit a voltage drop across them, increasing the voltage drop across the diodes, which will lower their effective impedance.

The inverting low pass filter should be configured so that the cut off frequency is approximately one tenth of the desired low frequency response of the sensor. This ensures that the active bias will not attenuate signal frequencies. For f_L of 0.1Hz, the cut off frequency of the inverting low pass filter should be set to around 0.01Hz. The cut off frequency of the inverting low pass filter is given by:

$$f_c = \frac{1}{2\pi R_2 C_1}$$

C_1 was set to 100uF and R_2 to 100k Ω to give a cut off frequency of 0.016Hz. R_1 can be varied to alter the gain ($G_{invLPF} = R_2/R_1$), with higher gains applying a more aggressive bias control, whilst reducing circuit stability.

The frequency response and settling time of the circuit was simulated using Altium designer's SPICE simulation tool (For details of the spice simulation setup see appendix A). The input capacitance of the LMP7721 is not included in its SPICE model, so in these simulations a capacitance of 10pF was added between the amplifier input and the negative supply rail. R_1 was varied to alter the gain of the inverting low pass filter. Figure 6.8 shows the simulated frequency response for gains of -10 , -2 , and -1 . The gain rolls off at frequencies below the cut off of the inverting low pass filter. This shows that the cut off frequency of the high pass filter formed by C_s and the input resistance is below that of the inverting low pass filter, thus the input resistance must be $> 0.9T\Omega$. It also shows that the active biasing scheme is reducing the impedance below the cut off frequency of the inverting low pass filter. The passband gain is -7.5 dB which corresponds to the attenuation from the capacitive divider formed by C_s and the input capacitance. It can be seen that as the gain of the active bias circuit is increased, the stop band attenuation becomes steeper, the phase margin is reduced, and the gain begins to peak at the resonant frequency of the inverting low pass filter. Increasing the gain

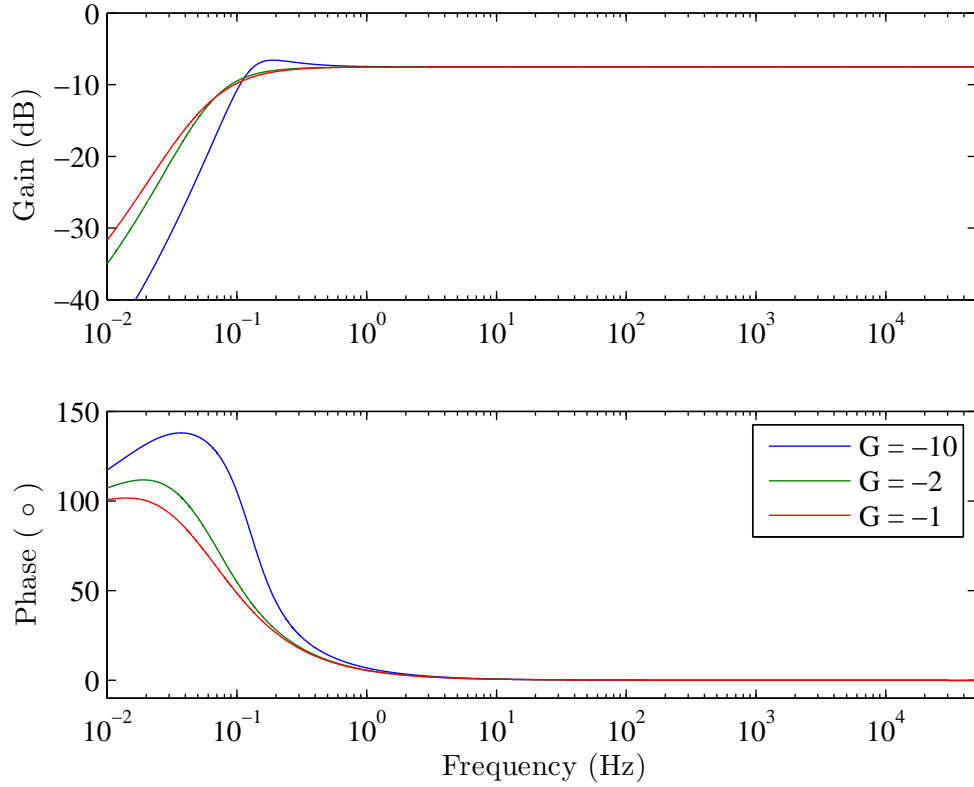


Figure 6.8: Simulated frequency response of anti-parallel diode biasing circuit in figure 6.7.

further would result in oscillations at the resonant frequency of the circuit. In order to illuminate the effect of the active bias gain on the settling time of the circuit, the step response of the circuit needs to be investigated.

Figure 6.9 shows the simulated response of the circuit to a 100 mV input step, at gains of -10, -2 and -1, as well as with a fixed bias. The fixed bias is achieved by simply connecting R_3 to the desired bias level. The horizontal dashed lines are used to illustrate when the output has settled to within 5%. From this response it can be seen that the active bias scheme should decrease the settling time for gains of -2 and -1, but overshoot or ringing becomes a problem with higher gain.

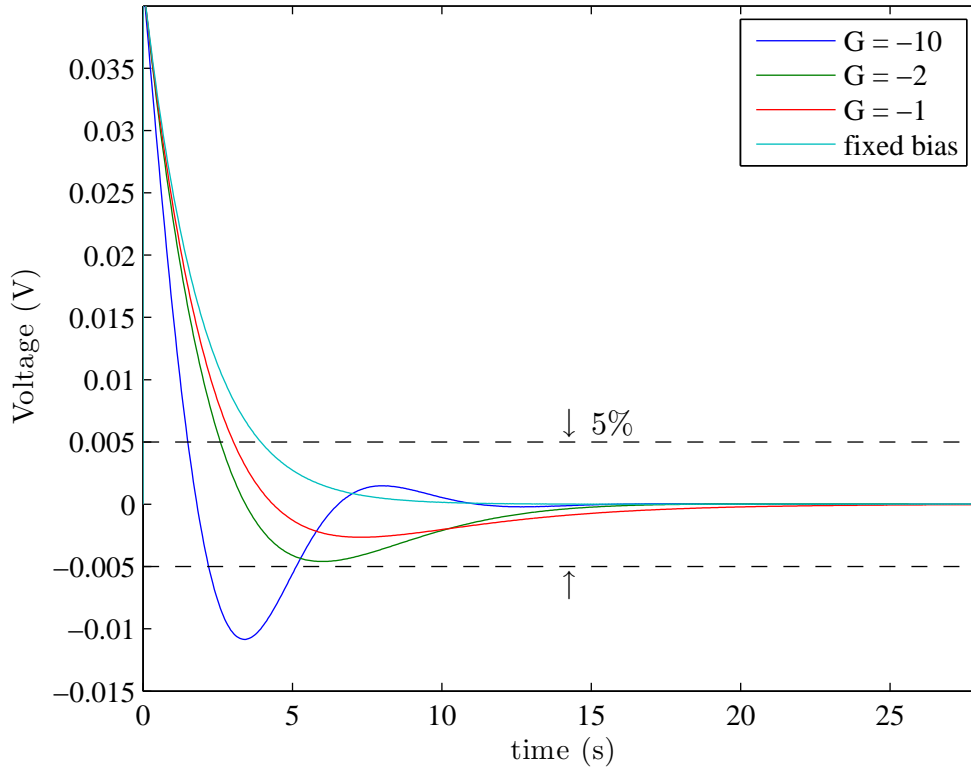


Figure 6.9: Simulated response of circuit in figure 6.7 to a 100mV step for gains of -2, and -1. The fixed bias response removes the LPF, attaching R_3 directly to the circuit reference.

The circuit was incorporated into version 1 of the non-contact sensor shown in figure 6.10. This sensor includes a capacitance neutralisation circuit covered in section 6.5, however the following measurements were all made without connecting the capacitance neutralisation circuitry.

Figure 6.11 shows the measured response of the circuit to a 100mV step input. The shape of the responses match that of the simulated response from figure 6.9, however the circuit does not settle to the bias voltage as in the simulation. This

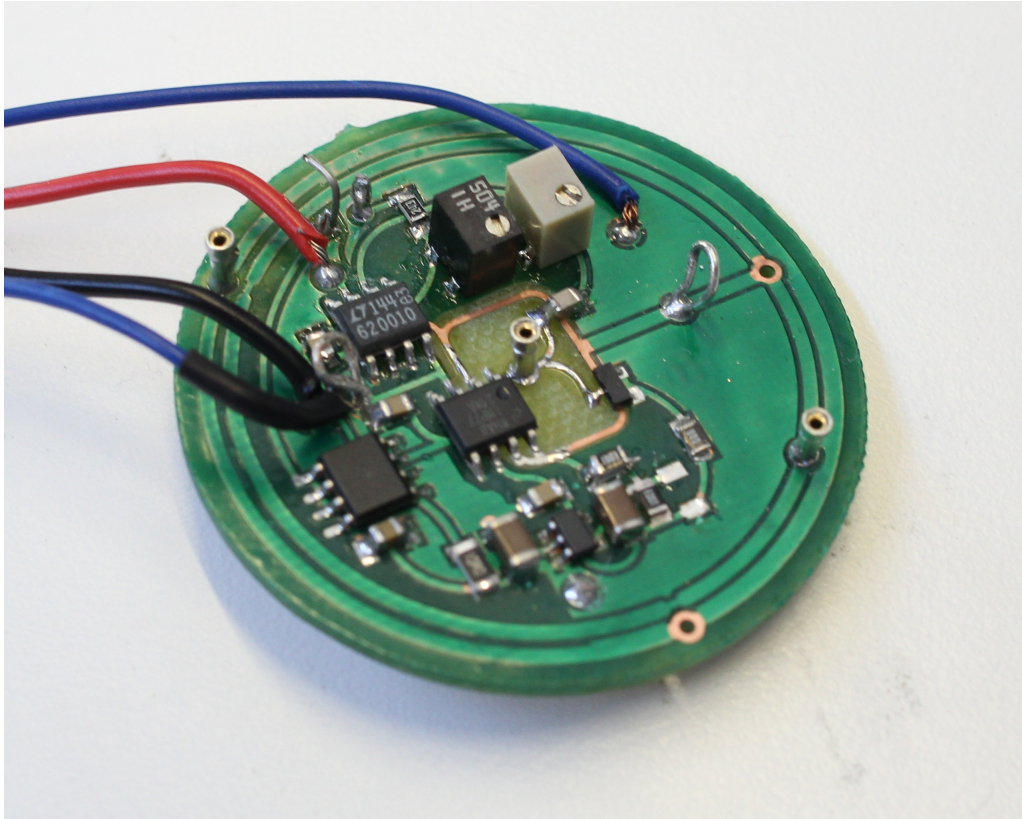


Figure 6.10: Version 1 of the non-contact sensor. This circuit incorporates the active bias circuitry of figure 6.7, and the capacitance neutralisation circuit covered in section 6.5.

means there is some voltage across the diodes, which will increase their conduction. The active bias configuration appears to lower this voltage, which means that in addition to faster settling times, the active bias also increases the DC input impedance under normal operating conditions.

Figure 6.12 shows the simulated and experimentally measured frequency response of the circuit in figure 6.7. It can be seen that the measured response follows a similar response curve to the simulation, but the passband is severely attenuated. The SPICE model used for the BAV199 sets a fixed value for the junc-

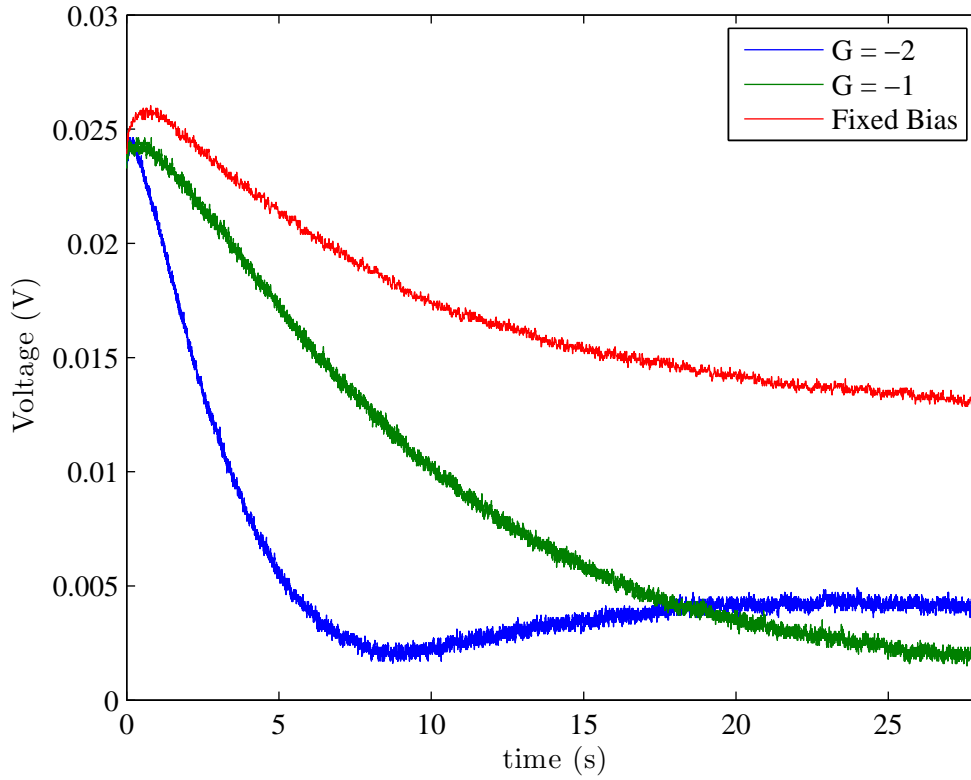


Figure 6.11: Measured response of circuit in figure 6.7 to a 100mV step for gains of -2, and -1. The fixed bias response removes the LPF, attaching R_3 directly to the circuit reference.

tion capacitance of the device. In reality there is a relationship between the voltage across the diode and the junction capacitance, with lower voltages yielding lower capacitances. The active bias scheme allows signal frequencies to appear across the diodes, which will increase the capacitance, lowering the AC input impedance. The AC impedance can be raised by using an old technique called bootstrapping, where feedback is applied from the output to the biasing element, raising the effective AC input impedance (Towers, 1968). The following section investigates bootstrapping the biasing element to raise AC impedance.

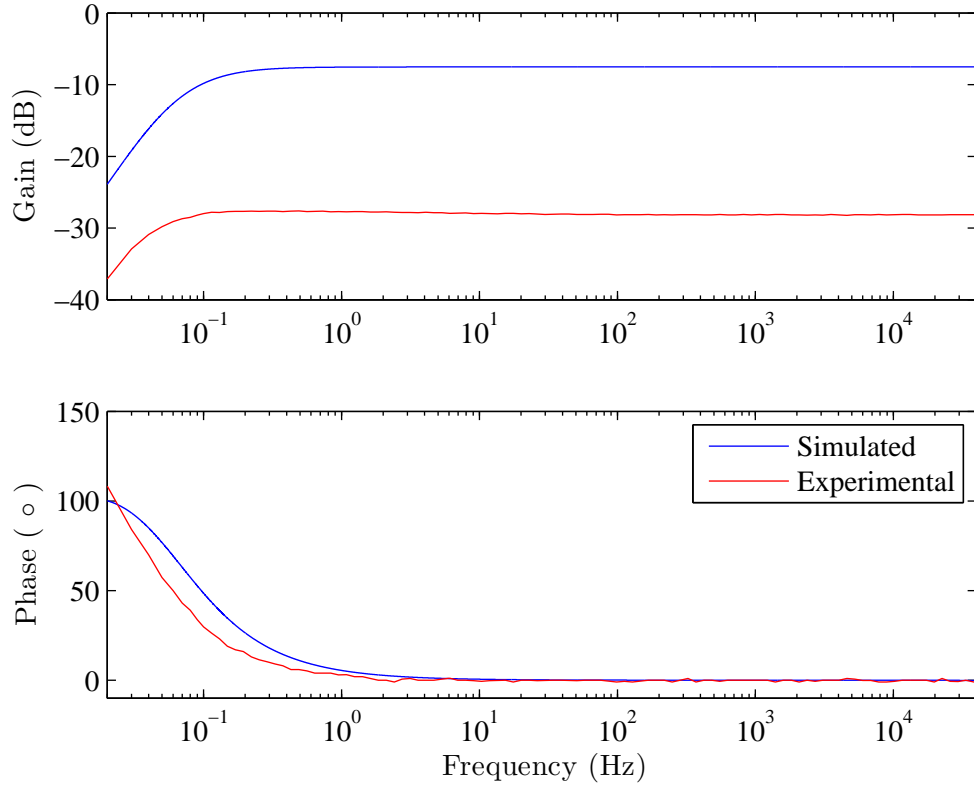


Figure 6.12: Simulated and measured frequency response of circuit in figure 6.7 with $C_s = 10\text{pF}$.

6.4.3 Bootstrapping

The previous section identified that the anti-parallel diodes were exhibiting a capacitance greater than that expected from the component specifications, and the circuit simulations. This excess capacitance caused a large attenuation of the input signal, across all frequencies. The excess capacitance was attributed to signal frequencies appearing across the diodes, raising the junction capacitance. The diode SPICE model did not take account of this dependence and so the effect was not seen in the simulations. This section uses breadboard circuit prototyping to investigate bootstrapping techniques to reduce the capacitance of the anti-parallel

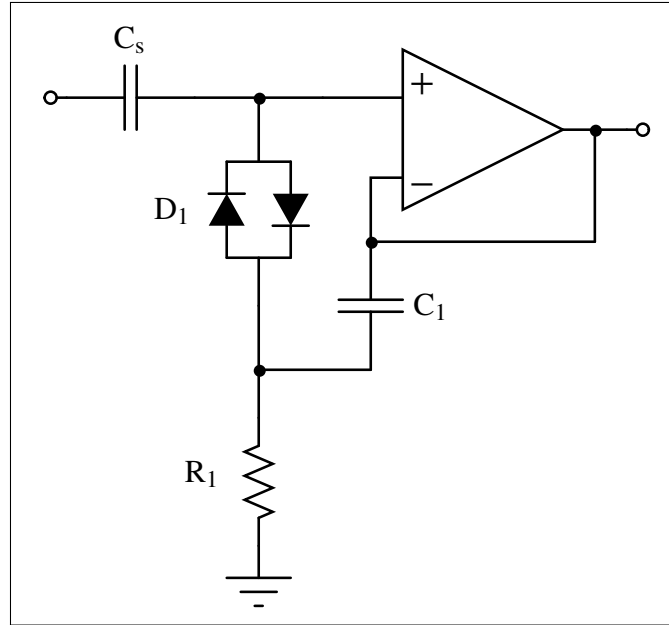


Figure 6.13: Bootstrapping with static DC bias

diodes.

Bootstrapping is often used to increase the input impedance of BJT amplifiers from $k\Omega$ s to $M\Omega$ s. The same techniques can be applied with FET amplifiers to achieve input impedances $> 1\text{ T}\Omega$ (Towers, 1968). By AC coupling the output of a unity gain buffer to the input biasing element, the effective impedance of the biasing element is raised by a factor equal to the open loop gain of the buffer amplifier (Kitchin and Counts, 1986).

Bootstrapping was applied to a non-contact sensor design by Chi et al. (2009) in a scheme similar to that shown in figure 6.13. The anti-parallel diodes are bootstrapped for frequencies above $1/2\pi R_1 C_1$, masking the diode's capacitance and increasing the effective input impedance at these frequencies.

The capacitance, C_1 used to couple the AC signal to the biasing element must be large enough to present negligible impedance at signal frequencies. Kitchen and Counts (1986) suggest using a capacitance which is larger than $1/f_L R_1$ where f_L is the lowest signal frequency. Setting R_1 to $10\text{M}\Omega$ and f_L to 0.1Hz the bootstrap capacitor should be $> 1\mu\text{F}$. The circuit of figure 6.13 was prototyped on a breadboard and its frequency response was measured. C_1 was set to $3.3\mu\text{F}$ and R_1 to $10\text{M}\Omega$. A 330pF source capacitance was used to couple input signals to the circuit, reducing any attenuation by the circuit's input capacitance. It was found that the circuit exhibited a pronounced resonance at the low frequency cut off. This resonance could cause stability problems with the sensor. To reduce the resonance a resistor was added in series with the capacitor in the bootstrap path, and the frequency response measured. Figure 6.14 shows the results of these tests. The legend entries show the component values of the bootstrap circuit. It can be seen that adding the resistor in the bootstrap path damps the resonance of the circuit, without severely altering the bandwidth, or passband gain of the circuit.

The bootstrap circuit comprising a resistor in series with a capacitor was combined with the active biasing scheme of section 6.4.2 to produce the circuit of 6.15. This design attempts to reduce the settling time, with the active biasing scheme, whilst maintaining high input impedance across signal frequencies by bootstrapping the input biasing element.

The circuit in Figure 6.15 was prototyped on a breadboard, along with the circuit of figure 6.7 to evaluate the function of the bootstrapping circuit. The inverting low pass filters of both circuits were set to a gain of -1, and the cut off frequencies set at 0.016Hz . R_4 , R_3 and C_2 of the circuit in 6.15 were set to $100\text{k}\Omega$, $10\text{M}\Omega$, and $100\mu\text{F}$ respectively. R_3 of the circuit in 6.7 was set to 0Ω . The frequency response of both circuits with a 30pF source capacitance was measured. These results are shown in Figure 6.16. The circuit without bootstrapping is heavily attenuated at all frequencies, showing the excess capacitance seen in Section 6.4.2. The bootstrapped circuit exhibits only minor attenuation, of around

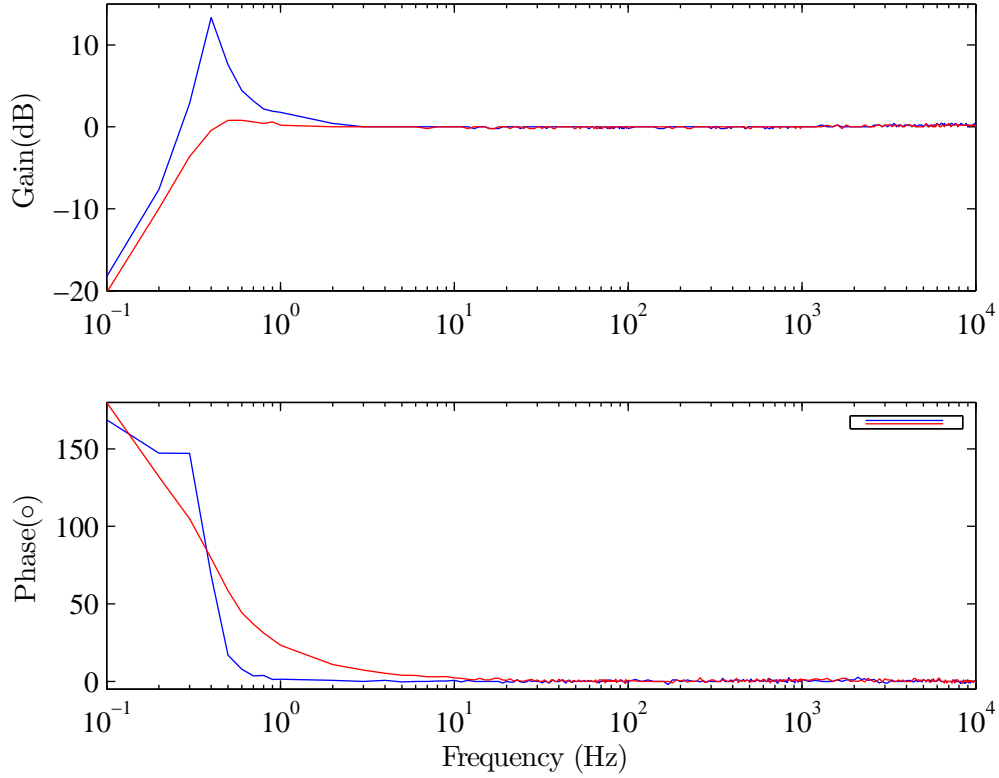


Figure 6.14: Breadboard prototype testing: Comparison of the frequency response between a purely capacitive bootstrap and a series capacitor and resistor bootstrap. Zb shows the values of the bootstrap circuit components.

the magnitude expected by the interaction of the source capacitance and the amplifier input capacitance. This shows that bootstrapping the diodes has masked the diode capacitance, raising the impedance at signal frequencies.

In order to better understand the circuit operation a simplified mathematical model of the circuit was developed. Using ideal op-amp models the circuit was broken into 5 sub circuits; the source impedance (C_s), the diode biasing element (D_1), the bootstrap path (C_2 and R_4), the inverting low pass filter (U_2, C_1, R_2 , and R_1), and the bias coupling resistor (R_3). The anti-parallel diodes were modeled

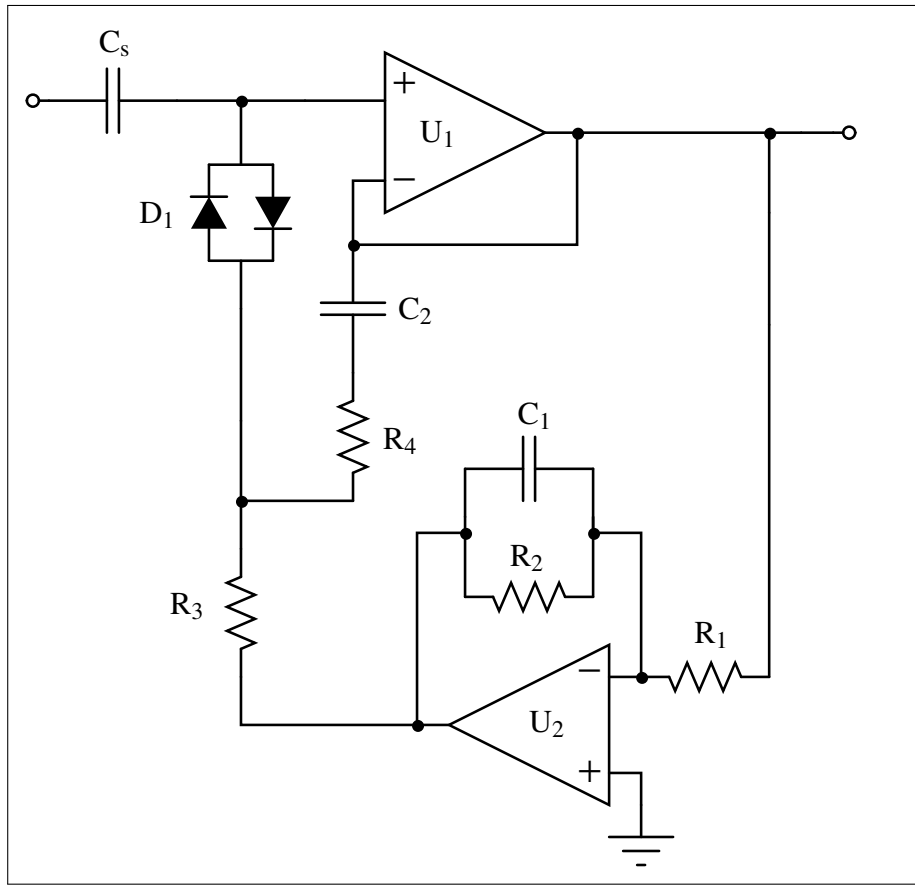


Figure 6.15: Anti-Parallel Diode Biasing with bootstrapping to raise AC impedance.

as a resistor (R_d) in parallel with a capacitor (C_d), representing the junction capacitance, and the effective resistance of the diodes. This model does not take into account the voltage dependency of these properties of the diode, however the model can still be used to gain insight to the effects of varying component values. The transfer function was derived using Kirchoff's laws, working in the laplace

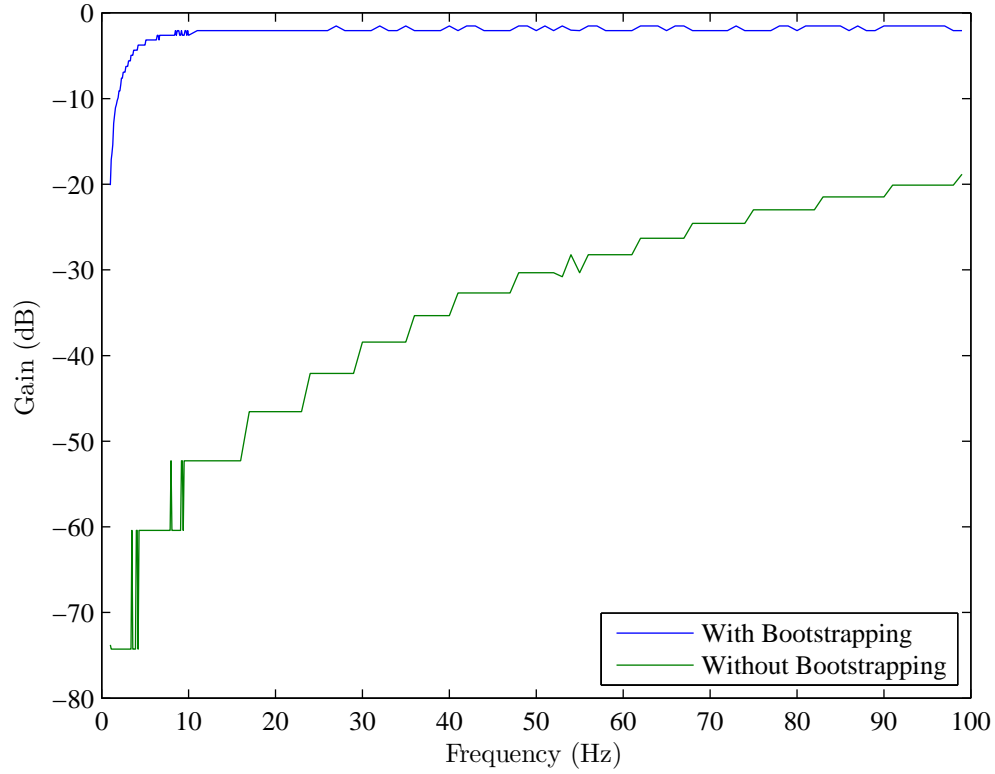


Figure 6.16: Breadboard prototype testing: Comparison of the gain vs frequency between the circuits in Figure 6.7 (Without Bootstrapping), and Figure 6.15 (with bootstrapping).

domain and is given by:

$$T(s) = \frac{\frac{D(s)}{A(s)} + \frac{D(s)B(s)}{A(s)} + D(s)R_3}{1 + C(s) + \frac{D(s)}{A(s)} + \frac{D(s)B(s)}{A(s)} + D(s)R_3} \quad (6.3)$$

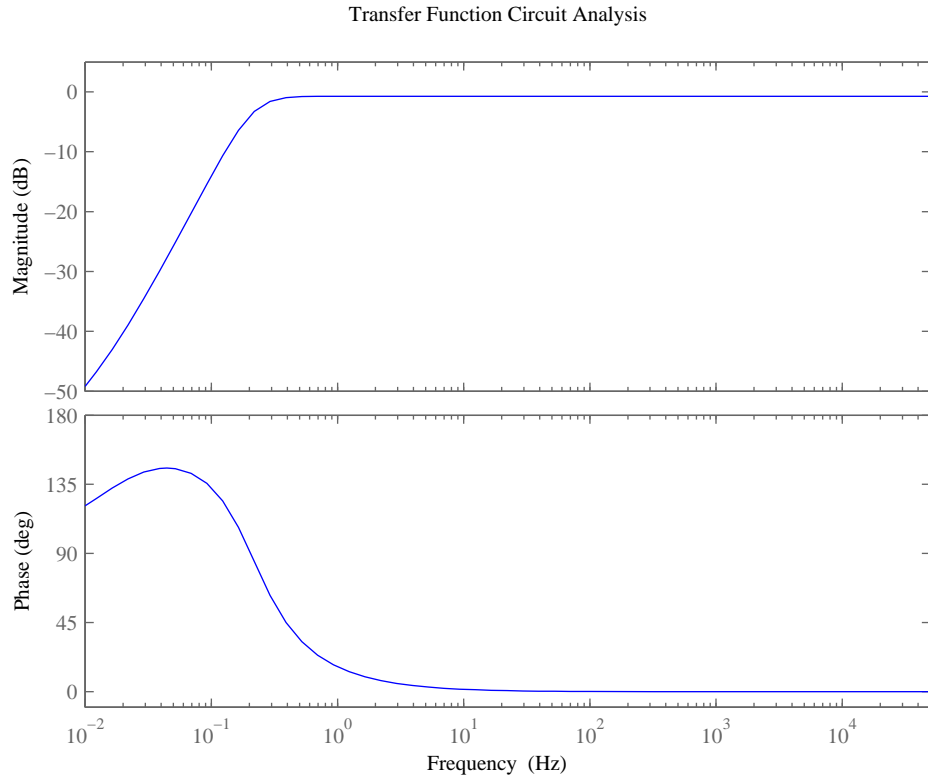


Figure 6.17: MATLAB simulation of transfer function from (6.3)

where:

$$A(s) = \frac{sR_d C_d + 1}{R_d}$$

$$B(s) = \frac{sC_2 R_3}{1 + sC_2 R_4}$$

$$C(s) = \frac{R_2/R_1}{sC_1 R_2 + 1}$$

$$D(s) = sC_s$$

The transfer function of (6.3) was evaluated in MATLAB to explore the effect of component values on the circuit behaviour. The desired frequency response was

achieved with R_1 and $R_3 = 10\text{k}\Omega$, R_2 and $R_4 = 100\text{k}\Omega$, and C_1 and $C_2 = 100\text{uF}$. Figure 6.17 shows the bode plot obtained using these values.

By applying bootstrapping techniques the attenuation observed in Section 6.4.2 has been eliminated. Breadboard prototype circuits suggest that the active biasing scheme of Section 6.4.2 can be used with input bootstrapping to create a high impedance biasing network. The following section explores the use of an alternative biasing element to the anti-parallel diodes, in an attempt to create a more versatile biasing element.

6.4.4 Exotic Biasing Networks

The anti-parallel diode biasing element used in the previous sections has been shown to work very well for high impedance input biasing. However, there is a desire to develop an alternative biasing element, which can provide more control over the input impedance. This section develops a biasing element based on low leakage JFET transistors.

Sullivan et al. (2007) used bipolar junction transistors (BJTs) to bias the amplifier of their non-contact bio-potential sensor. The BJTs are connected to both the inverting and non-inverting inputs of the sensor amplifier. Their base emitter voltage is controlled, so that when the input voltage is outside of the common mode range of the amplifier the transistors are turned on, returning the inputs to the bias level quickly, and avoiding saturation of the sensor. The low frequency response ($\approx 1\text{Hz}$) achieved by this scheme is unacceptable. This is most likely due to the high leakage currents of BJTs. To improve the frequency response low leakage transistors could be used instead of BJTs.

The lowest leakage, discrete transistor found was the 2N4117A N-channel JFET from Linear Integrated Systems. The 2N4117A has a gate leakage current of $< 1\text{pA}$, and drain source channel symmetry (Linear Integrated Systems, 2012). Since the channel is symmetric, the drain-source current will flow equally well in

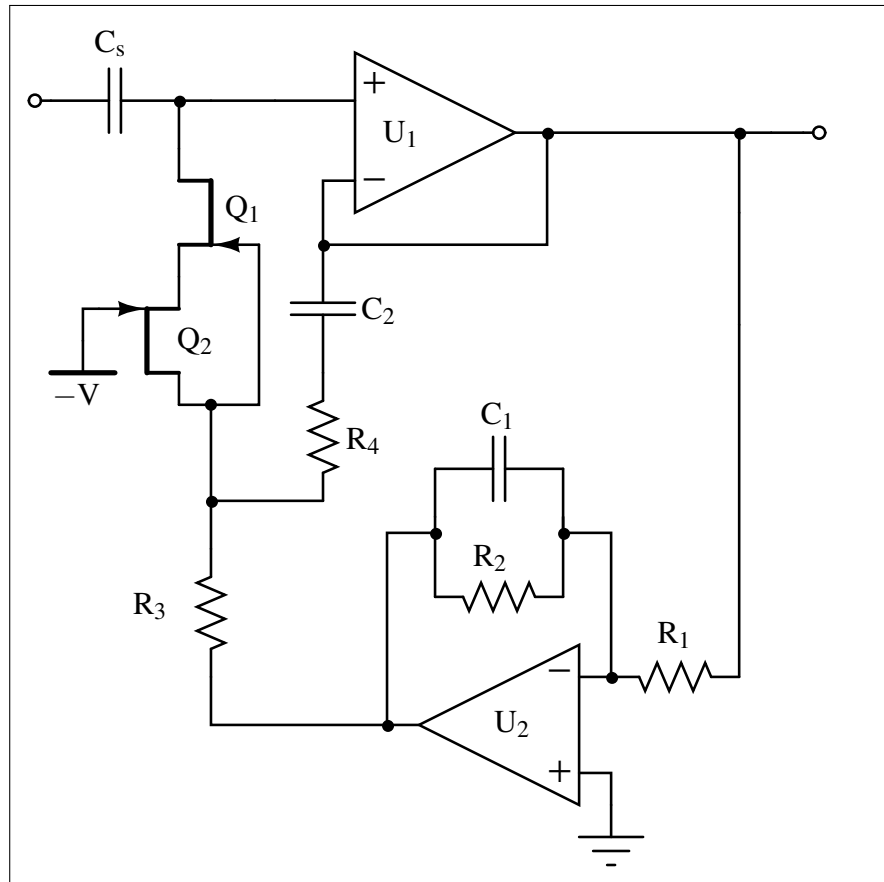


Figure 6.18: JFET current Source Biasing with AC feedback

both directions. The direction of the current can be altered by changing the polarity of the drain-source voltage. The 2N4117A was used to create a biasing element which allows more control over its impedance than the anti-parallel diodes.

The design of the JFET biasing element began with the idea of implementing a voltage controlled current source. It was thought that the current source could be set to a low leakage state under normal operation, and the current raised to counteract input transient events. A design for a JFET based current source is given in (Williams, 2005). This design consists of a single JFET with a resistor

connected between the gate and the source. The higher the value of the resistance, the lower the drain current of the JFET. Williams (2005) states that the accuracy of this configuration is poor, however it is suitable for situations where accuracy is not important, such as amplifier biasing. This circuit was elaborated on by adding a voltage controlled resistor (VCR) to set the current. A VCR can be made using a single JFET, where the drain and source form the two legs of the resistor and the gate voltage can be used to alter the resistance. The resistance decreases as the gate voltage is increased, and the drain-source voltage is fixed. The resistance also decreases as the drain source voltage increases. If the gate is fixed at a low voltage, Then the drain source voltage will control the current, making this element compatible with the design from Section 6.4.3. Figure 6.18 shows the JFET biasing element replacing the anti-parallel diodes of Figure 6.15. This configuration was the final iteration of the high impedance biasing network. Results for this circuit are given in Chapter 7.

6.5 Input Capacitance Neutralisation

This section presents an input capacitance neutralisation circuit to reduce mechanical coupling to the input.

Figure 6.19 shows a diagram of the capacitances involved at the input to the sensor. C_s is proportional to $1/d$, where d is the distance between the body and the electrode, as shown in equation (6.1). Small changes in distance will cause relatively large changes in C_s . Thus distance fluctuations are transduced to electrical signals by:

$$V_2 = V_1 \left(\frac{1}{1 + \frac{C_{in}}{C_s}} \right) \quad (6.4)$$

where V_2 is the voltage at the amplifier input, V_1 is the voltage at the body surface, C_{in} is the input capacitance of the sensor, and C_s is the distance dependent body to electrode capacitance. Even if C_s remains fixed, there will still be attenuation

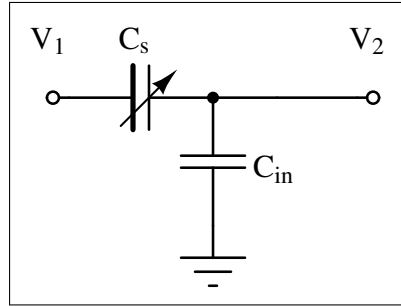


Figure 6.19: Capacitive Voltage Divider

at the input, which will degrade the signal to noise ratio.

From (6.4) it can be seen that the extent to which the signal is attenuated can be minimised if the source capacitance is much larger than the input capacitance. The source capacitance can vary between 1-100 pF (see figure 6.3), and the input capacitance of the sensor is around 10 pF. This means the input can be attenuated by as much as -20 dB. In order to reduce this attenuation the input capacitance must be reduced. The following section presents a solution to this problem in the form of an input capacitance neutralisation circuit.

6.5.1 Capacitance Neutralisation Circuits

Miller's theorem states that an impedance between two nodes can be replaced with two equivalent impedances connected between each node and ground as shown in figure 6.20 (Sedra and Smith, 2004). If these impedances are capacitive, then they can be related by the following equations:

$$C_a = C_x \left(1 - \frac{V_2}{V_1}\right) \quad (6.5)$$

$$C_b = C_x \left(1 - \frac{V_1}{V_2}\right) \quad (6.6)$$

If a gain element is included between the two nodes, as in figure 6.21 then $\frac{V_2}{V_1}$ is

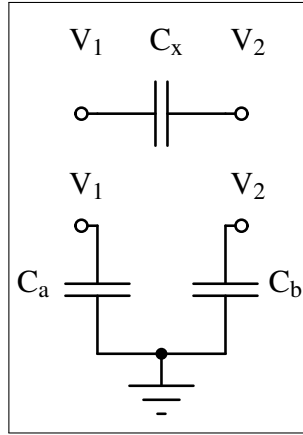


Figure 6.20: Miller Equivalent Circuit

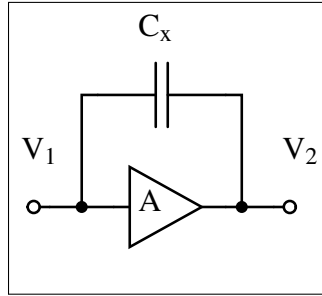


Figure 6.21: Adding a Gain element

equal to the gain and (6.5) becomes:

$$C_a = C_x(1 - A) \quad (6.7)$$

If the gain is greater than 1, C_a will be negative, and can be used to reduce the total capacitance from V_1 to ground. The optimal gain for neutralising the input capacitance can be obtained by setting C_{in} to $-C_a$, and substituting into (6.7) to give:

$$A = \frac{C_{in}}{C_x} + 1 \quad (6.8)$$

At this gain the input capacitance will be zero, and there will be no attenuation at the input. This gain must be maintained over all signal frequencies, for optimal

operation. The low pass response of a compensated op amp could cause attenuation, or if the op amp is not rated to drive capacitive loads it may increase the gain near the gain bandwidth frequency. If the gain increases the input capacitance will become negative, introducing gain at the input according to (6.4). If this happens the circuit is in danger of becoming unstable. Whilst stability is ensured if $C_{in} + C_s < 0$, the gain peaking causes distortion, and if the gain peaks are sufficiently sharp, low level oscillations will occur. To minimise the risk of these problems the op amp used should have a very wide bandwidth, giving low phase shift at signal frequencies, and be rated to drive capacitive loads.

The phase response of the capacitance neutralisation circuit could be improved by using a phase compensation circuit consisting of two operational amplifiers as described in (Soliman, 1979). This configuration relies on precision matched resistors and the amount of phase compensation is dependent on the gain. Thus creating a variable gain stage which provides adequate phase response would be difficult. It was decided to use a single op amp with a high bandwidth to simplify the design of this stage.

Figure 6.22 shows the circuit used to achieve capacitance neutralisation. The potentiometers allow the gain to be precisely tuned. R_{cor} should be 10 times greater than R_{fin} , giving a coarse and fine adjustment of the gain. C_n should be set to keep the gain low ($A < 4$), and U_3 should have a very high bandwidth to ensure the capacitance neutralisation is effective over the entire signal bandwidth.

The LT6200-10 op amp was chosen for U_3 because of its high gain bandwidth product of 1.6GHz. This configuration was implemented in version 1 of the non-contact sensor (figure 6.10). The input capacitance of the sensor was measured to be around 12pF, thus C_n was set to 4.7pF to give an optimum gain of ≈ 3.5 . This circuit had trouble with the diodes exhibiting excess capacitance as discussed in Section 6.4.2. The capacitance neutralisation circuit was not able to compensate for this, and so determining its operation effectiveness was not possible. How-

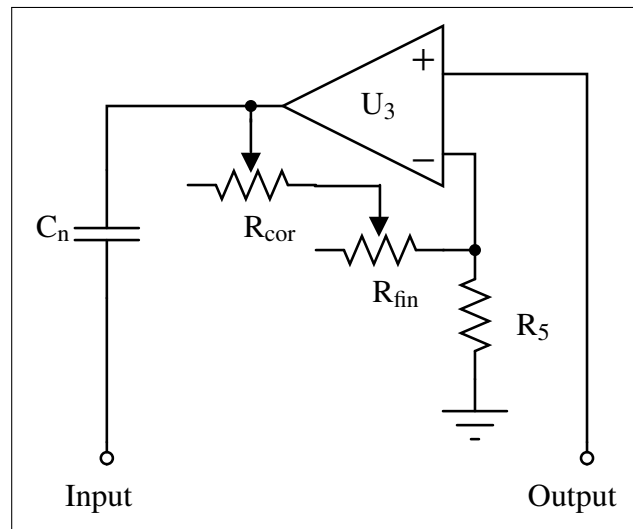


Figure 6.22: Capacitance neutralisation feedback connects between the input and output of the sensor. R_{cor} should be 10 times greater than R_{fin} to facilitate precise tuning.

ever it was noticed that the LT6200-10 was introducing small oscillations into the circuit. Upon closer inspection of the datasheet, it was found that this op amp exhibits gain peaking with any capacitive load, and requires snubbing resistors to damp the response. It was also drawing around 20mA from the power supply, which is too high for operation from a low current 5V reference. For the next iteration U_3 was changed to the LTC6252H56 op amp, which has lower power consumption, and a lower gain bandwidth product of 720MHz. This IC was included in the final version of the sensor, the results are presented in Chapter 7.

6.6 Integration

This section presents the problems, and solutions found when integrating the high impedance biasing circuit of Section 6.4.4 with the capacitance neutralisation circuit of Section 6.5.

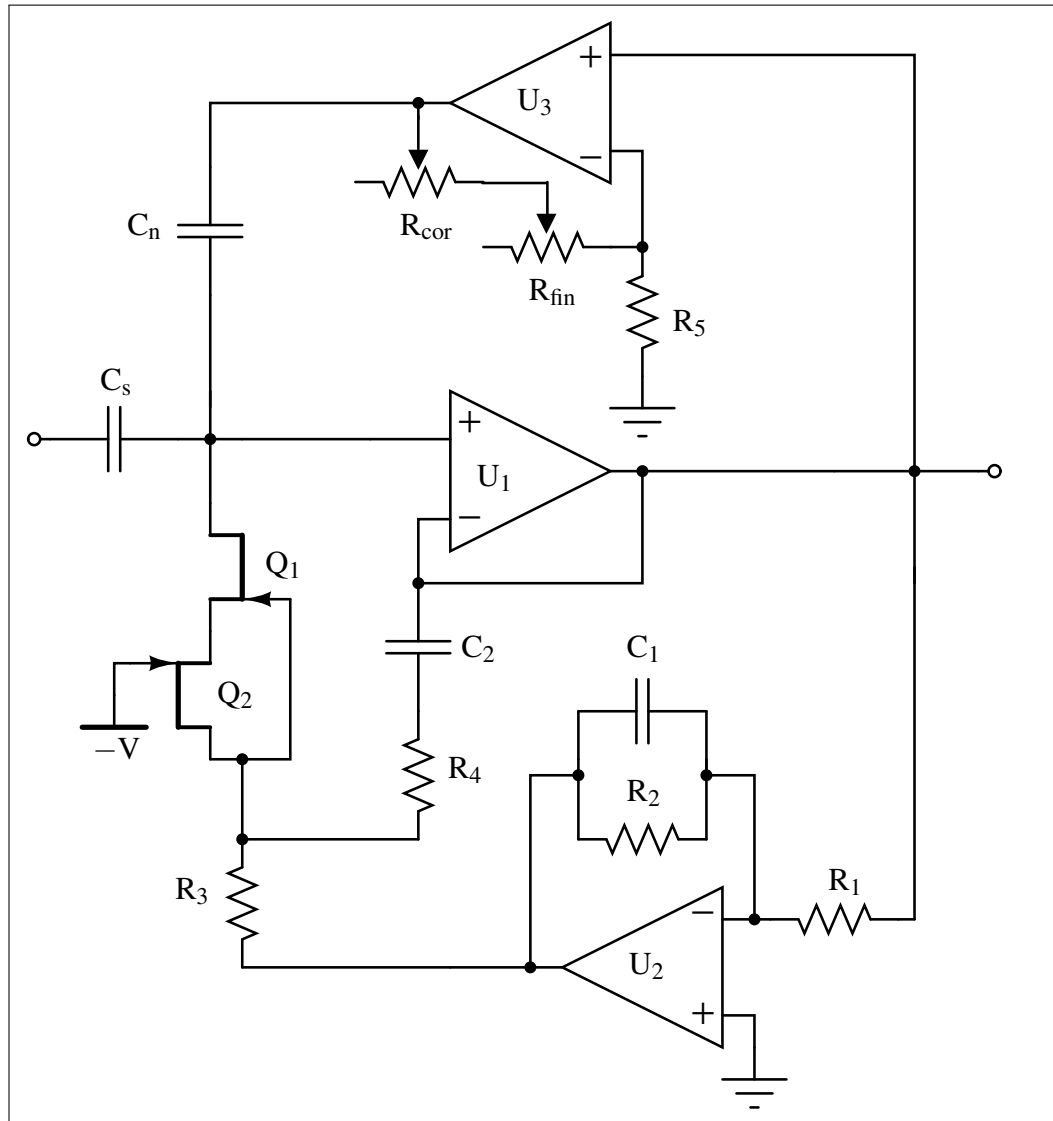


Figure 6.23: Final circuit design incorporating active bias scheme and capacitance neutralisation circuit.

Figure 6.23 shows the circuit diagram of the final sensor, and Figure 6.24 shows the completed printed circuit board of the sensor. Note that the component labels on the PCB overlay do not match with the circuit diagram.

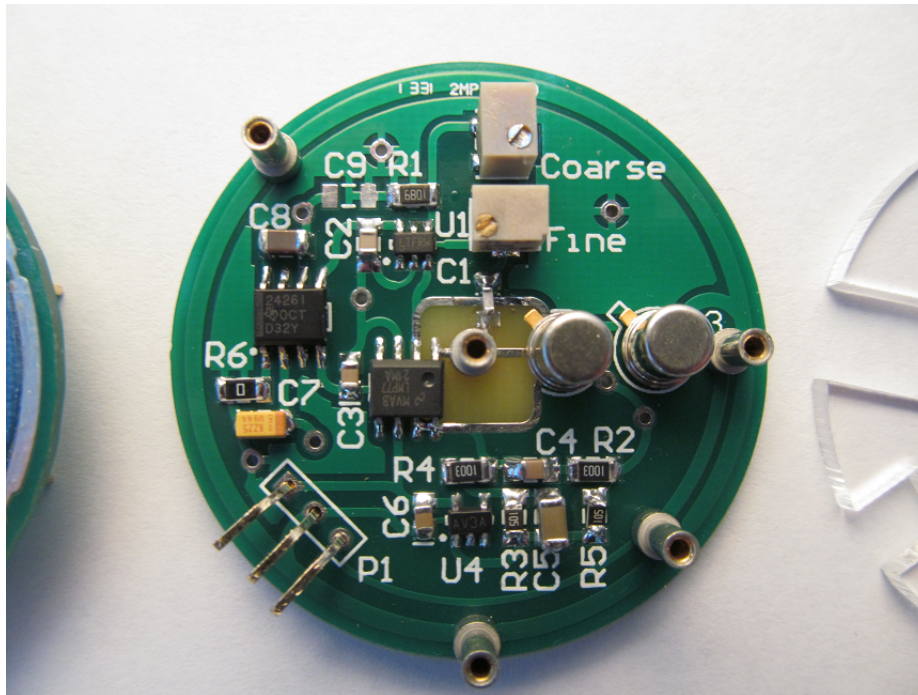


Figure 6.24: Populated PCB of the Final sensor

The capacitance neutralisation circuit requires precise tuning to achieve low input capacitance, whilst maintaining sensor stability. A tuning method has been written to define the calibration routine. This method is given in Appendix B.

The TLE2426CP "rail splitter" IC was used to generate the bias voltage of +2.5V from the +5V supply rail. This IC consists of a precision voltage divider, and a buffer amplifier to produce a low impedance output voltage equal to $1/2$ the input voltage. A noise reduction (NR) capacitor can be added externally, to reduce the RMS noise at the output.

When measuring the spectral noise density of the sensor, a resonant peak was discovered. The origin of this resonance was traced to the NR capacitor of the TLE2426CLP. The voltage noise spectral density plots of figure 6.25 document

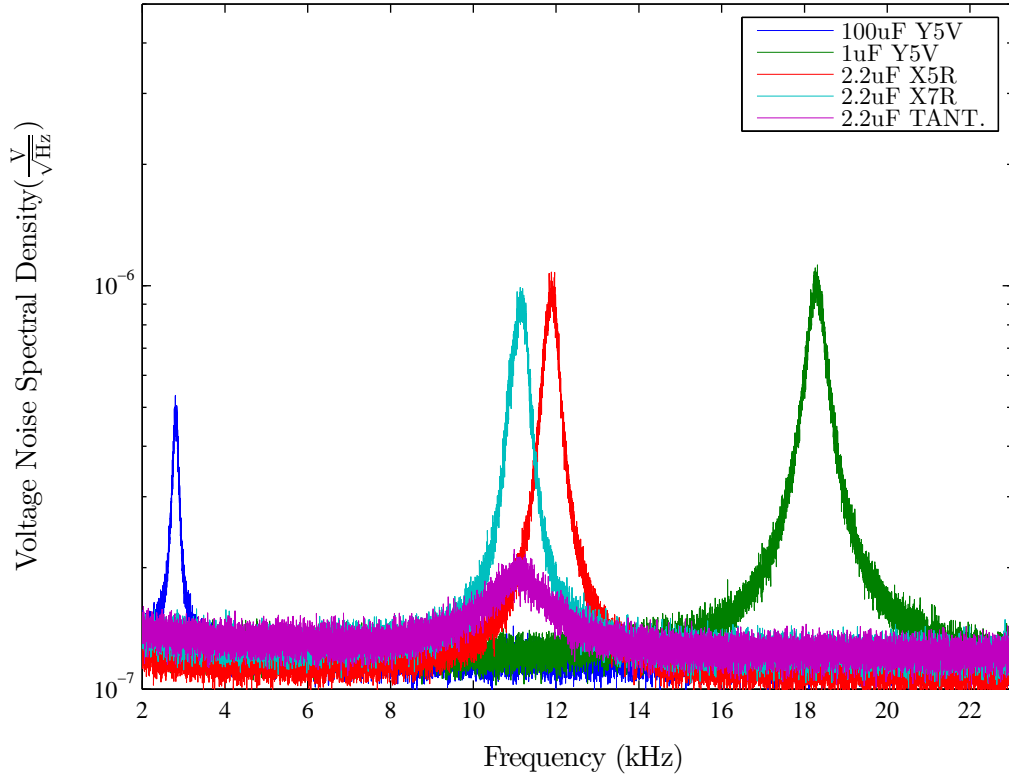


Figure 6.25: Comparison of voltage noise spectral density for various noise reduction capacitors.

the resonances encountered for different capacitor values and dielectric types. The Y5V, X5R and X7R multilayer ceramic dielectrics all show large resonances compared to the tantalum capacitor. This is probably due to the higher inductance of the multilayer ceramic capacitors, interacting with the impedance of the NR pin of the TLE2426CLP. No mention of this effect was given in the datasheet, or recommendations for capacitor specifications. It can be seen that the $2.2\ \mu\text{F}$ tantalum capacitor gives the lowest amplitude resonance, thus this capacitor was chosen for the final sensor.

The component values derived from the MATLAB simulations in Section

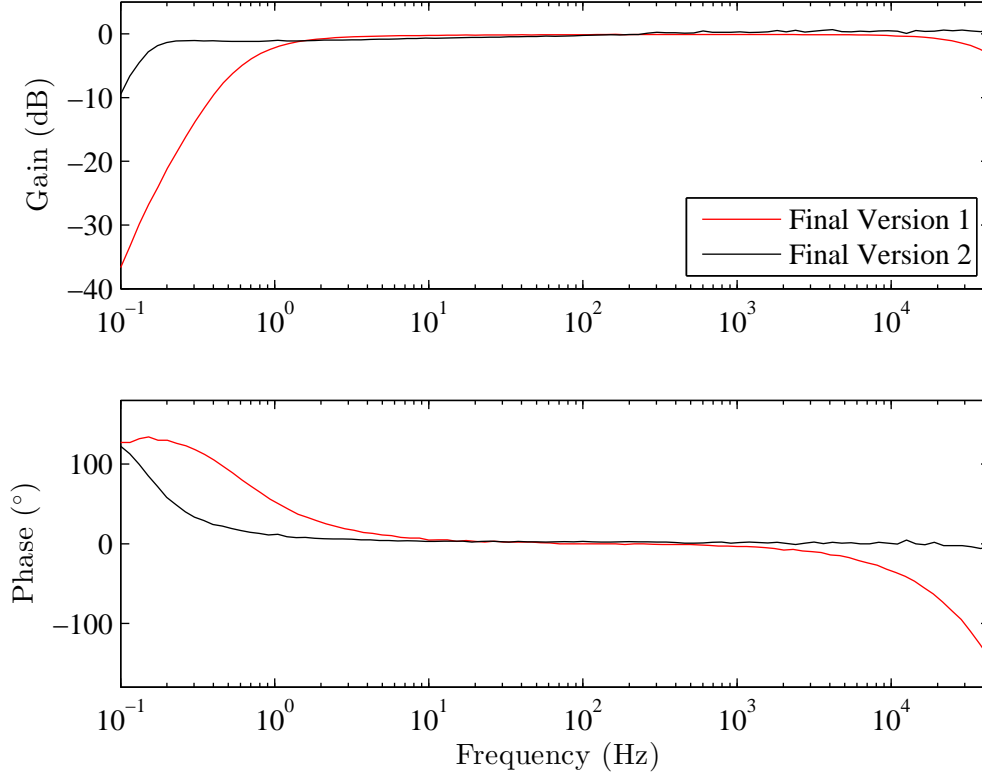


Figure 6.26: Comparison of frequency response of final sensor with 1 pF source capacitance. Version 1 uses component values: R_1 and $R_3 = 10\text{k}\Omega$, R_2 and $R_4 = 100\text{k}\Omega$, and C_1 and $C_2 = 100\mu\text{F}$. Version 2 uses component values: R_1 and $R_4 = 100\text{k}\Omega$, R_2 and $R_3 = 1\text{M}\Omega$, $C_2 = 4.7\mu\text{F}$, and $C_1 = 100\mu\text{F}$.

6.4.3 were fitted to the final sensor and the frequency response with source capacitance of 1 pF was measured. The low frequency -3 dB point was measured to be 0.8 Hz, which is higher than that predicted by the model of ≈ 1 Hz. The interaction between the active biasing circuitry and the bootstrap circuit was reconsidered to better define the component values. The active biasing circuit has a low pass response with a gain of A . At the cut off frequency ($f_{c_{ab}}$), the output magnitude is $(A-3\text{ dB})$. The bootstrap circuitry has a high pass response with cut off frequency (f_{c_b}). This gives an output magnitude at f_{c_b} of -3 dB. These circuits

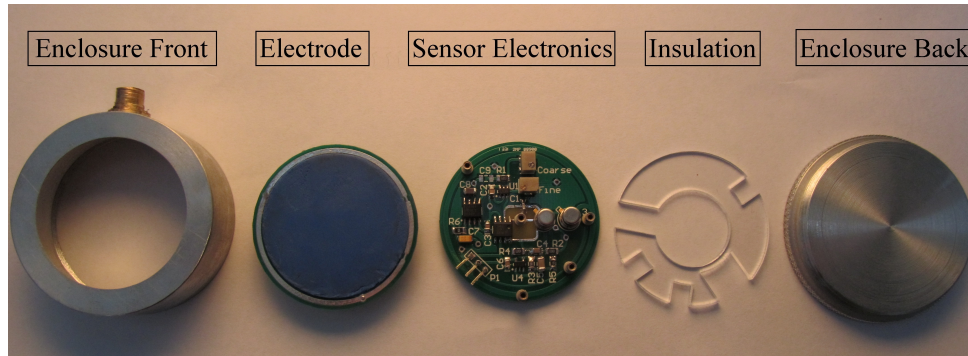


Figure 6.27: Non-Contact Bio-Potential Sensor - Components of Sensor

should be set so that the -3dB points cross over at the same frequency. This ensures that the bootstrap efficiency is not degraded by the active biasing circuitry. If the active bias gain is set to 20dB then due to the -20dB/decade roll off, the output magnitude will be -3dB at $10 \times f_{cab}$. Thus setting $f_{cb} = 10 \times f_{cab}$ will maintain the bootstrap efficiency. Figure 6.26 shows the comparison between these two realisations of the final circuit. Version 1 uses the component values defined by simulations and version 2 uses those defined by the more intuitive method given above. It can be seen that the cut off frequency has been lowered from 0.8Hz for version 1 to 0.15Hz for version 2.

6.6.1 Sensor Assembly

This section presents the design of the sensor enclosure and the assembly of the final device.

The enclosure for the sensor was designed so that it could be electrically connected to the shield of the electrode. This provides contiguous shielding around the entire sensor assembly. The enclosure was designed with a lip on the front so that the electrode shield trace could make contact with the lip. The back of the enclosure screws into the front, securing the electrode-sensor electronics assembly, and the acrylic insulation layer into place. Figure 6.27 shows the components of

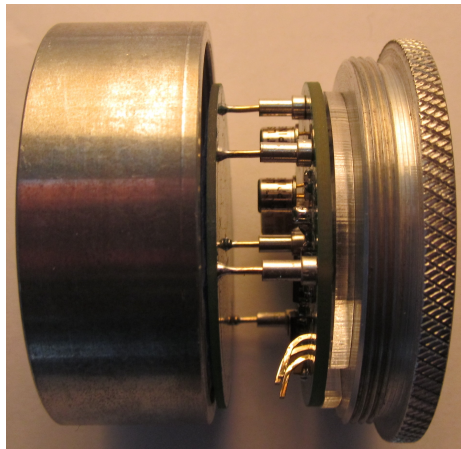


Figure 6.28: Non-Contact Bio-Potential Sensor - Assembly of Sensor

the sensor, and 6.28 shows how these components are assembled.

Chapter 7

Sensor Evaluation

In this chapter the input leakage current, frequency response, gain vs distance, input impedance estimate, step response, and noise of the final sensor are evaluated. An ECG recording using the final sensor is presented to demonstrate the practical application of the sensor.

7.1 PCB Leakage

To verify the effectiveness of the guarding scheme the input bias current of the sensor PCB was measured before populating the input biasing and capacitance neutralisation feedback circuits. The bias current was measured using the method presented in Section 4.2. The sensor input amplifier (LMP7721) has a typical input bias current of 3 fA (Texas Instruments, 2008). The input bias current was measured to be 2.8 fA. As this measured value is around the same as the specification it can be deduced that the input guarding scheme is effectively blocking any excess leakage currents flowing into the input as intended.

7.2 Frequency Response

The frequency response of the sensor from 0.1 Hz to 50 kHz was measured for source capacitances of 0.5 pF, 1 pF and 10 pF using the method defined in Section

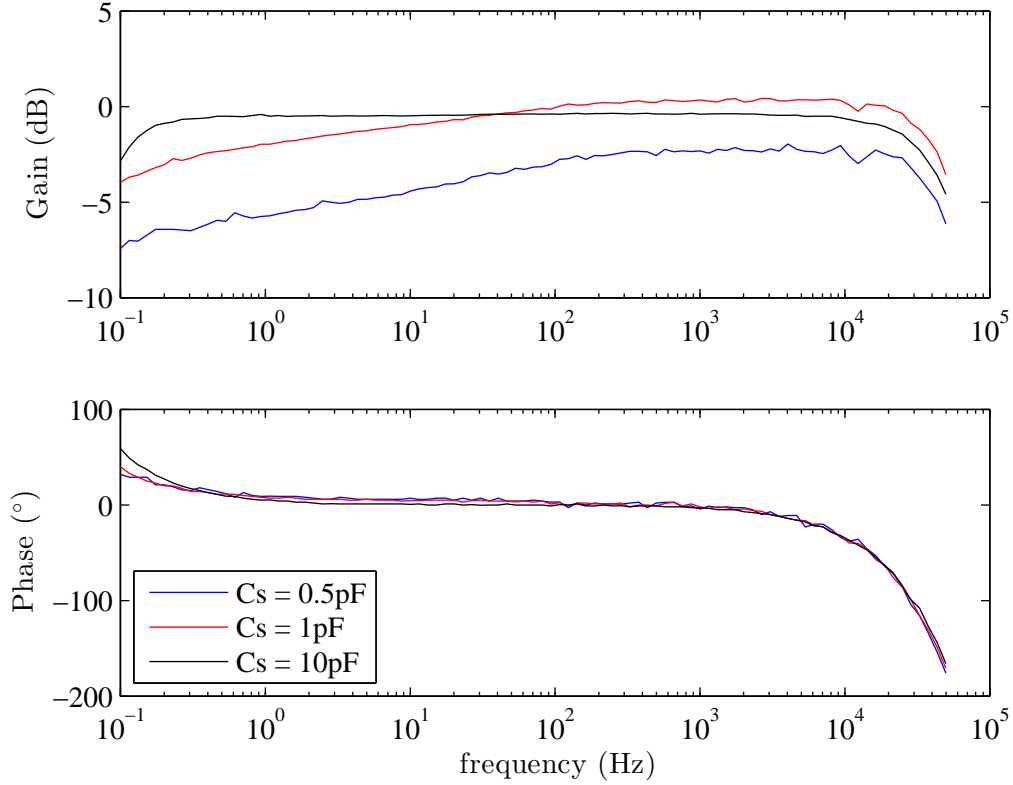


Figure 7.1: Frequency response of final sensor for different source capacitances.

4.3 with the addition of a 50kHz low pass filter at the output. The results of these measurements are shown in figure 7.1.

The response using a 10pF source capacitor maintains a flat frequency response down to 0.15Hz. With 0.5pF, and 1 pF the gain response seems to have a slight (1 dB/decade) attenuation below 100Hz. It is not clear what caused this response, particularly as there is no hint in the phase response of an additional pole in the system. A possible explanation is that at these lower source capacitances the input is coupled to the sides of the shielded test environment. This coupling could interfere with the applied input voltage, causing errors in the voltage reading. Another possible explanation is that the source capacitors used degraded the

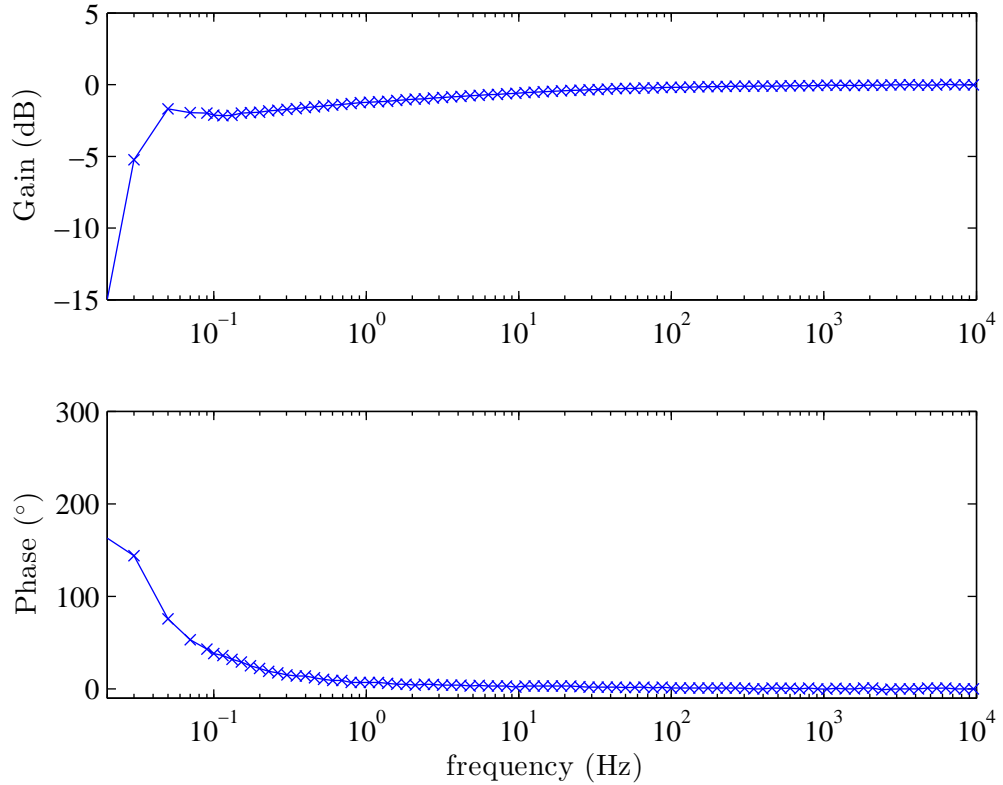


Figure 7.2: Frequency response of final sensor assembly with input from a driven metal plate

performance at lower frequency. The capacitor used for the 10 pF test came from a different manufacturer than that used in the 1 pF test. The 0.5 pF test used a series combination of the 1 pF capacitor. The fact that both the 0.5 pF and the 1 pF test show the same attenuation and they both used the same capacitor type, suggest this is a likely cause.

The frequency response of the final sensor assembly (electrode – sensor electronics – insulation – enclosure) was measured using an aluminium plate as the source. The input voltage was applied to the plate and the sensor assembly was set on top of the plate. The program of Section 4.3 was used to collect the data.

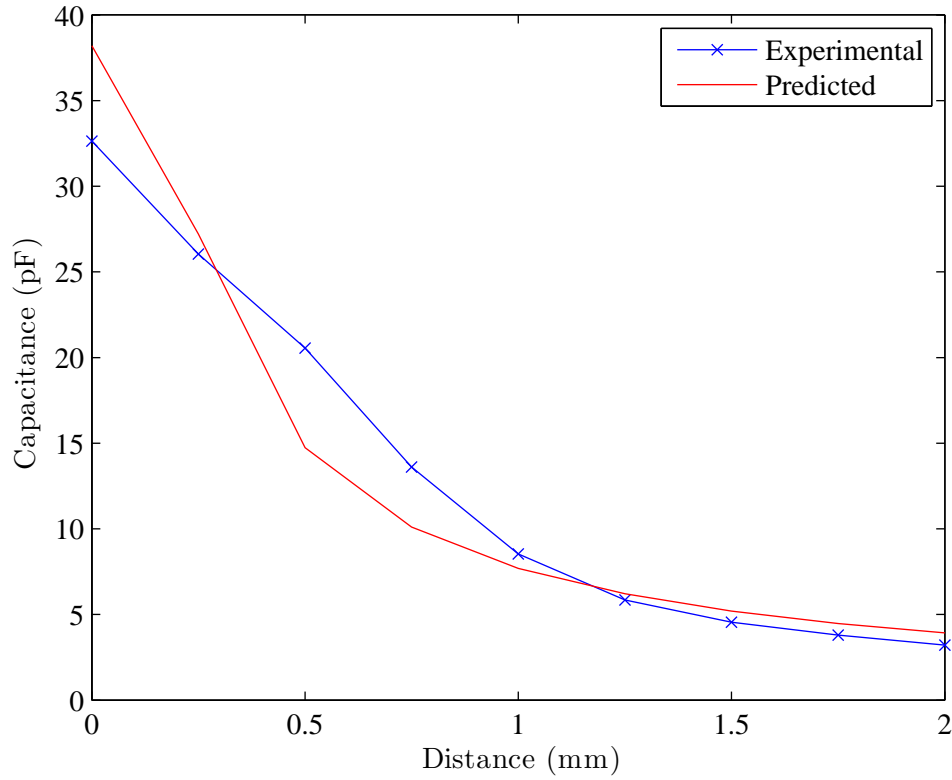


Figure 7.3: Experimental verification of source capacitance vs distance

Figure 7.2 shows the measured frequency response. The assembly achieves a low frequency response down to 0.04 Hz, complying with (and exceeding) the specified 0.1 Hz defined in Section 1.3.

7.3 Gain vs Distance

Using equation (6.4) the source capacitance vs distance was able to be estimated from the measured input capacitance, the input voltage, and the output voltage. The theoretical source capacitance from Figure 6.3 is plotted with the experimentally derived values in Figure 7.3. It can be seen that the model and experimental values match very closely, verifying that the silicone insulation provides an in-

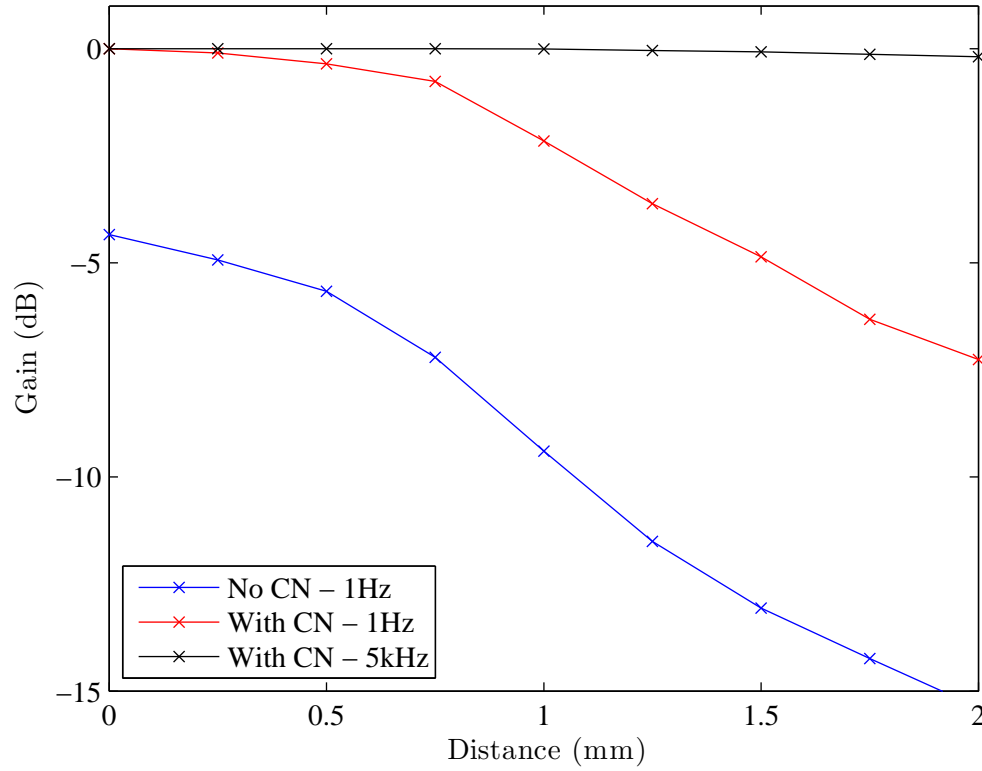


Figure 7.4: Gain vs Distance from source

crease in capacitance as predicted. The capacitance when source and insulated electrode are in contact is $> 30\text{pF}$.

The sensor gain vs distance from the source was measured before and after applying the capacitance neutralisation circuitry. These tests were performed using the apparatus and method given in Section 4.5. Figure 7.4 shows the results of these tests at a frequency of 1 Hz. It can be seen that the capacitance neutralisation circuit removes the signal attenuation when the sensor is within 0.5 mm of the source. This means when in use the sensor will be insensitive to small mechanical fluctuations such as patient muscle contractions. The gain vs distance was also measured at 5 kHz to show the higher frequency response. It can be seen that at

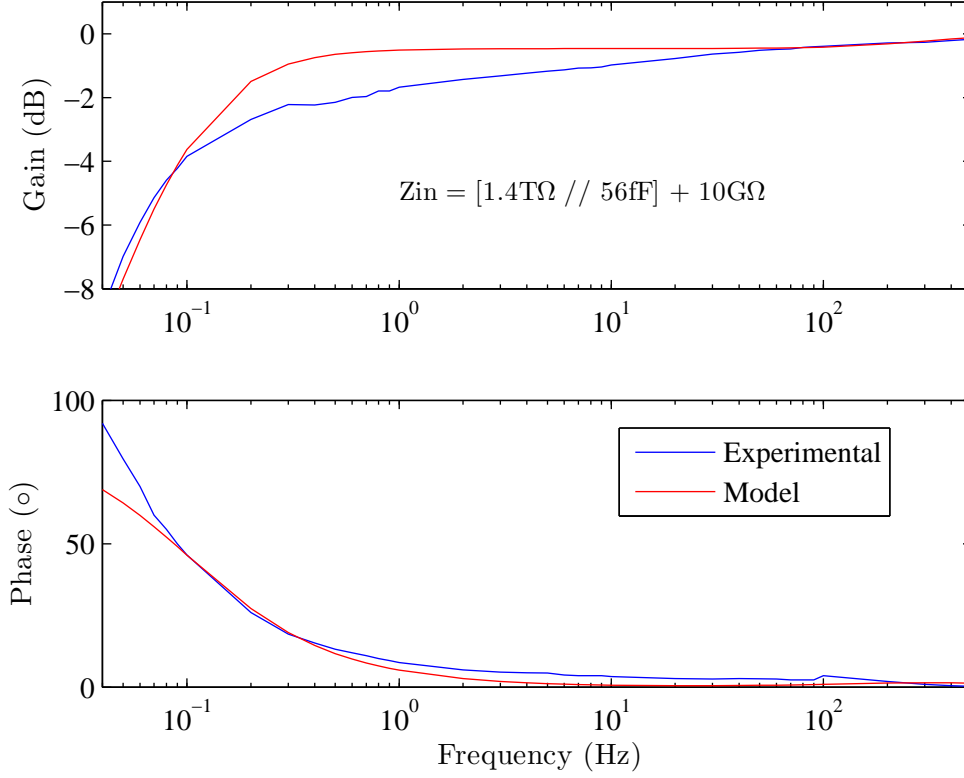


Figure 7.5: Experimental and model frequency response of sensor with $C_s = 1\text{pF}$. Z_{in} is the simple model used to estimate the input impedance ($1.4\text{T}\Omega$ in parallel with 56fF , both of which are in series with $10\text{G}\Omega$).

higher frequencies the response is much flatter. This is of particular interest to the higher frequency ECoG measurements, as the sensor can be positioned further away from the patient without severe attenuation of the signal.

7.4 Input Impedance Estimation

The input impedance of the sensor was modelled as a network consisting of a parallel resistor and capacitor, modelling the bootstrapped JFET biasing element, in

series with a resistance modelling the connection to the active biasing circuitry.

The input impedance was extracted from the frequency response by:

$$Z_{in}(s) = \frac{Z_s(s)}{\frac{V_{in}(s)}{V_{out}(s)} - 1} \quad (7.1)$$

The series resistance can be estimated by taking the real part of the input impedance at high frequency. This element was estimated to be $10\text{ G}\Omega$.

The parallel capacitance and resistance can be estimated from the low frequency response using the input admittance:

$$Y(s) = \frac{1}{Z(s)} \quad (7.2)$$

$$Y(s) = \sqrt{G(s)^2 + B(s)^2} \quad (7.3)$$

$$C = \frac{B(s)}{\omega} \quad (7.4)$$

$$R = \frac{1}{G(s)} \quad (7.5)$$

where B and G are the admittance parameters: susceptance and conductance respectively (Agilent Technologies, 2013a).

The parallel capacitance was found to be 56 fF , and the parallel resistance $1.4\text{ T}\Omega$. The frequency response of this model is plotted with the experimental data in Figure 7.5. There is some deviation from the model around the cut off frequency. However as the impedance is an order of magnitude estimate, and the model is very simple, some deviation is expected.

7.5 Settling Time

The settling time of the final sensor assembly was measured in order to evaluate the effect of the novel active biasing scheme. A 100 mV square wave was applied

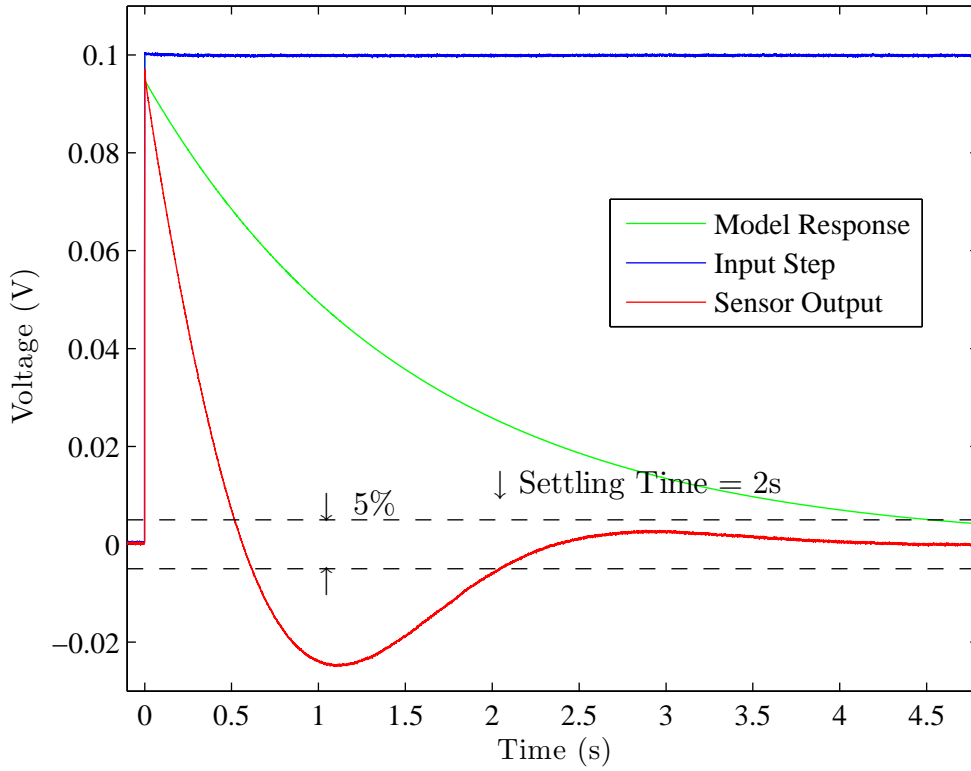


Figure 7.6: Step response of final sensor experimentally derived and predicted by simple model

to an aluminium plate and the sensor placed on this plate to measure the step response. Figure 7.6 shows the results of this test, as well as the response expected using the model developed in Section 7.4. The model does not include the active biasing scheme, thus provides an indication of the relative performance of a static biasing scheme, compared with the novel bias network developed in this research.

The settling time (within 5% of final value) of the final sensor to an input step of 100mV is around 2 seconds. The settling time for an equivalent input impedance without the active biasing circuitry is around 4.5 seconds, more than twice as long as was achieved with this novel biasing scheme.

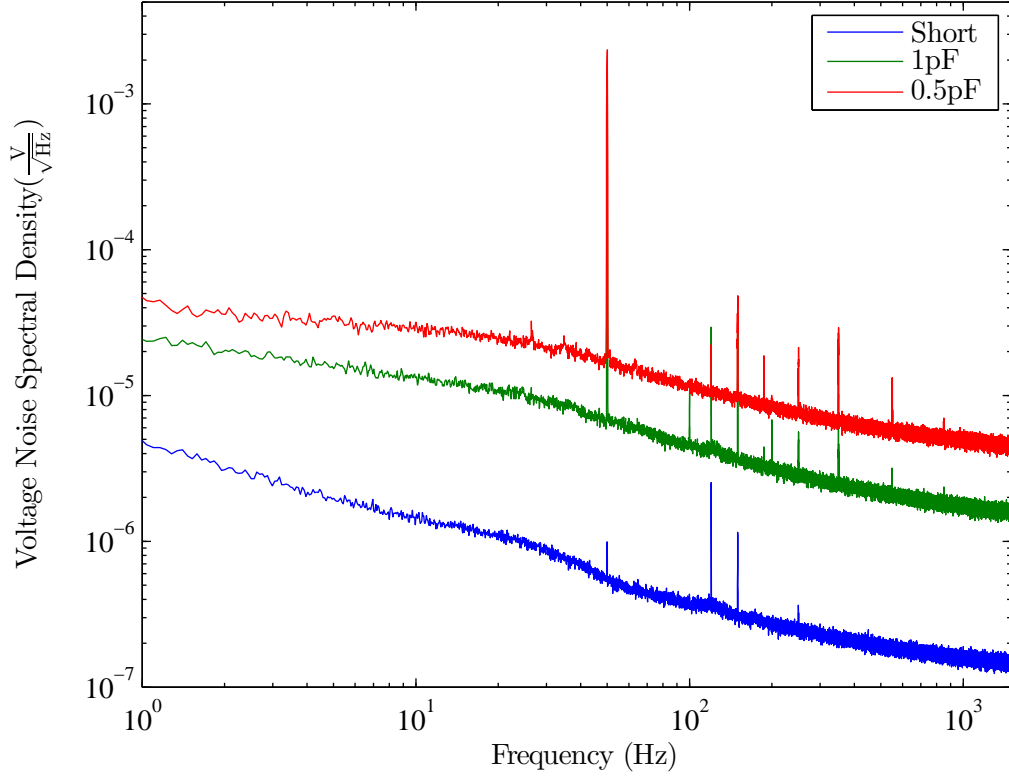


Figure 7.7: Input voltage noise spectral density of sensor.

7.6 Noise Measurement

The noise of the final sensor was measured using the method described in 4.4. The source capacitance was varied to show the increase in noise with lower coupling capacitances. Noise levels were observed to be sensitive to the tuning of the capacitance neutralisation feedback. If the gain of the feedback was reduced the noise level would also be reduced. Figure 7.7 shows the input voltage noise spectral density of the sensor after tuning the capacitance neutralisation according to the method in Appendix B.

The noise floor of the sensor is $200\text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz , rising to $5\text{ }\mu\text{V}/\sqrt{\text{Hz}}$ at

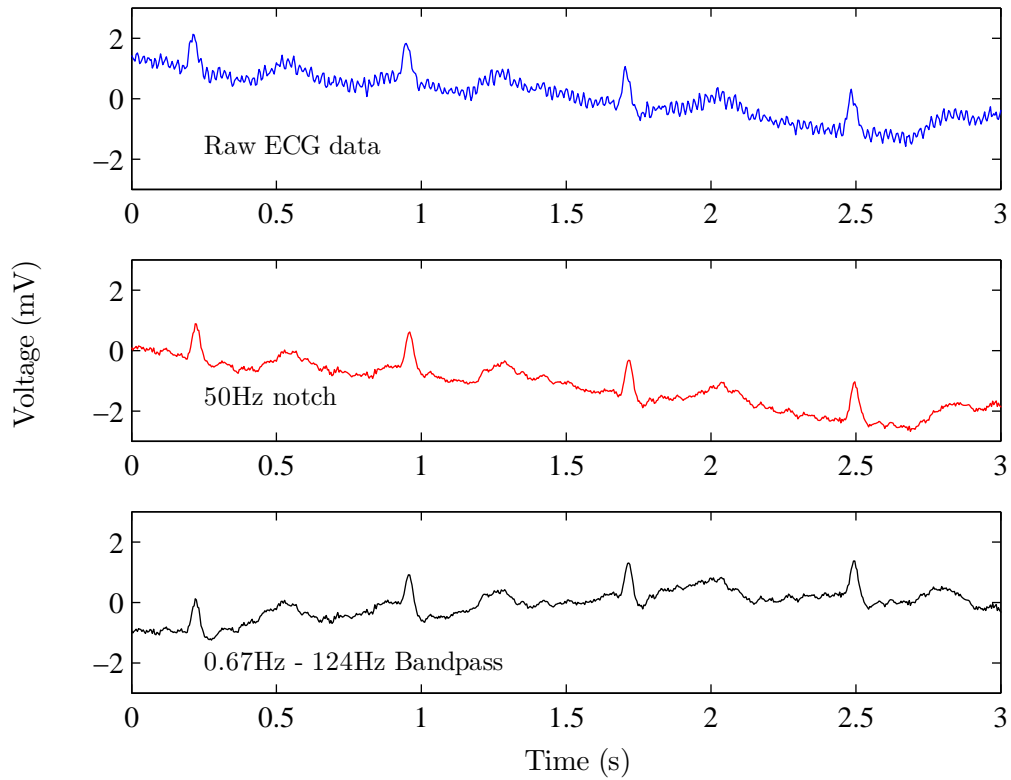


Figure 7.8: ECG recorded with a single sensor through a merino wool shirt. The top trace shows the raw data, with 50Hz interference present, the middle trace shows the signal after using a digital notch filter to remove the 50Hz, and the bottom trace shows the signal after bandpass filtering to the ECG bandwidth.

1 Hz. The noise is seen to increase as the source capacitance is reduced.

7.7 ECG Recording

To provide an indication of the effectiveness of the sensor as a non-contact bio-potential measurement device an ECG recording was taken using a single sensor. The sensor was applied with a merino wool undershirt on, and positioned to the left side of the chest.

Figure 7.8 shows the raw data with the 50Hz interference, the raw signal after applying a 50Hz notch filter, and then after band limiting between 0.57Hz and 124Hz. The shape of the ECG can clearly be seen, but this measurement needs to be performed simultaneously with the clinical standard Ag/Cl electrodes to verify the effectiveness of the sensor.

Chapter 8

Conclusion and Recommendations for Extension

As was shown in Section 2.2 knowledge of the electro-physiology of biological systems was historically furthered by advancement in the instrumentation. The ability of non-contact sensors to increase the spatial resolution of bio-potential measurements is such an advancement. This increase in spatial resolution could uncover new knowledge of electro-physiology. At very least it will improve diagnosis of well understood electro-physiological conditions. Furthermore the ability to monitor electro-physiology for long periods of time could uncover signs of disease and recovery hitherto unknown. This research makes an important contribution to the usability of non-contact bio-potential sensors by reducing the settling time for ultra-high impedance amplifiers.

8.1 Contributions

- A novel input biasing scheme for a non-contact bio-potential sensor which maintains high impedance for signal frequencies, whilst reducing the settling time to low frequency transient signals. This reduction in settling time means bio-potential measurements can be obtained quickly after applying the sensor. It also reduces the time spent in saturation after an input transient

event such as switching on a light, or excessive movements from the patient.

- The non-contact sensors and differential amplifier developed present a complete analog front end system for the investigation of bio-potential signals. This system will aid future researchers in acquiring bio-potential measurements for further analysis.

8.2 Conclusions

In Section 1.3 the research goals were defined as:

- Design and build a wide bandwidth (0.1 Hz – 20 kHz) non-contact sensor
- Develop original methods to reduce the settling time of non-contact sensors
- Build a system to acquire differential bio-potential signals

This section presents the evaluation of these goals.

The results presented in Section 7.2 show the sensor achieves a low frequency response down to 0.04 Hz. The bandwidth extends past 20 kHz, being cut off by the anti-aliasing filters of the differential amplifier at 50 kHz. These results show that the sensor complies with (and exceeds) the bandwidth goal of 0.1 Hz – 20 kHz

The sensor achieves a voltage noise spectral density of $200 \text{ nV}/\sqrt{\text{Hz}}$ above 1 kHz rising to $5 \mu\text{V}/\sqrt{\text{Hz}}$ at 1 Hz. The low frequency noise is similar to that achieved by the discrete sensor developed by Prance et al. (2000) of $100 \text{ nV}/\sqrt{\text{Hz}}$ above 1 kHz and $2 \mu\text{V}/\sqrt{\text{Hz}}$ at 1 Hz, but much higher than the integrated sensor

of Chi et al. (2011b) which achieves $200\text{ nV}/\sqrt{\text{Hz}}$ at 1 Hz. The integrated circuit approach of Chi et al. (2011b) focused on reducing the input capacitance without using neutralisation feedback. This suggests that the neutralisation feedback is a major source of noise in non-contact sensors. This is confirmed by the observations made in Section 7.6 that the noise levels were sensitive to the gain of the capacitance neutralisation feedback.

The response of non-contact bio-potential sensors to input transient events is a largely ignored problem in this field. Input transients shift the operating point of the sensor away from the bias voltage. When this signal is amplified saturation of the electronics is very likely, and bio-potential information will be lost. Furthermore, due to the long settling times of ultra-high impedance amplifiers the time spent in saturation can be unacceptably long. Sullivan et al. (2007) addressed this problem by implementing a bias reset network to prevent the sensor from saturating. This circuit only achieved a low frequency response down to $\approx 1\text{ Hz}$, which is deemed to high for analysing EEG and ECG signals. In this research an original input biasing network is presented that achieves a low frequency response down to 0.04 Hz , whilst greatly reducing the settling time of ultra-high impedance amplifiers.

In order to investigate the use of non-contact bio-potential sensors a differential amplifier was developed which takes the output of two such sensors, and amplifies the difference between them. The CMRR performance of this amplifier is critical to obtaining hi-fidelity measurements. Furthermore, the CMRR with frequency is critical for obtaining ECoG measurements in the audio frequency range. The amplifier developed has a CMRR of greater than 100 dB up to 10 kHz , providing excellent rejection of common mode interference over a wide frequency range. The amplifier developed has four gain settings to provide varying levels of amplification depending on the amplitude of the signals of interest. The accuracy of these gains is very important for evaluating bio-potential signals. The amplifier achieved gains of $20 \pm 0.02\text{ dB}$, $40 \pm 0.01\text{ dB}$, $60 \pm 0.03\text{ dB}$, and $80 \pm 0.3\text{ dB}$, pro-

viding very high amplitude accuracy. The input voltage noise spectral density of the amplifier was found to be $15 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz, rising to $55 \text{ nV}/\sqrt{\text{Hz}}$ at 1 Hz. These noise levels are far below that achieved in even the lowest noise non-contact sensors (Chi et al., 2011b). This ensures that the sensor rather than the differential amplifier imposes the limit of amplitude resolution.

As shown above this research has achieved (and exceeded) all of the goals set out in Section 1.3. Despite the success of this research there are limitations to the evaluation of the sensors developed.

8.3 Limitations

This section presents some of the observed limitations of this research.

Bio-potential measurements using the sensors developed in this research need to be compared to those recorded with the clinical standard Ag/Cl contact electrodes. Without this comparison the operation as a bio-potential sensor cannot be verified. The comparison would show any distortion of waveforms, motion artifacts, and amplitude errors.

The input to the ultra-high impedance amplifier is well shielded in the final sensor assembly, but for testing the electronics outside of the sensor assembly no such provisions were made. Signals applied to the input are subject to interference from other sources coupled to the input. This was deemed to be a potential cause of the strange low frequency response observed at lower source capacitances in Section 7.2.

8.4 Recommendations

This section presents recommendations for the extension of this research.

This research set about investigating the use of non-contact sensors for bio-potential sensing. Without focusing on a specific bio-potential the circuits developed were designed to work over a large frequency range, with varying source capacitances, and input amplitudes. Extension of this research should focus on a particular bio-potential; optimising the performance for this application.

An application specific sensor should consider the shape and size of the electrode which gives the best results. The bandwidth of the sensor could also be adjusted by tuning the active bias network to suit the frequency range required. The physical application of the sensor will be different depending on what bio-potential is to be measured. The shape of the body area, the movements of the patient, and the interference from other bio-potentials all need to be considered when designing an application specific sensor.

The response of the sensor to bio-potentials needs to be evaluated with respect to the clinical standard Ag/Cl electrodes.

Testing of the ultra-high impedance amplifier circuits could be improved by creating contiguous shielding from the test signal source, through the source capacitances used for testing, to the input of the electronics.

The capacitance neutralisation feedback presented in this research requires manual tuning. This limits the ease of production of these sensors, particularly if they are to be deployed in higher density arrays. The possibility of automatic tuning for capacitance neutralisation should be investigated. At present digital potentiometers present parasitic capacitances which are too large to warrant their use, however this problem may be resolved in the future making a digital solution possible. An alternative is to use voltage control techniques, tuning the gain with voltage controlled resistors. The specifics of such a scheme could be enough to constitute a final year undergraduate project, or even a Masters thesis.

As was pointed out in Section 8.2 the noise of the sensor could be reduced by fabricating an integrated circuit with lower input capacitance, eliminating the need for capacitance neutralisation feedback. An IC implementation would also significantly reduce the size, allowing higher density application of the sensors.

Another way to decrease the noise of the sensor is to add gain at the input amplifier. The reasoning for not including gain at the input amplifier in this research are mentioned in Section 6.2. In light of the fact that the settling time of the non-contact sensor has been reduced, the application of gain may not be such a problem for sensor saturation. However, the matching between sensors will still suffer, and any addition of gain should be compared to the reduction in CMRR between sensor pairs.

Appendix A

Spice Simulation for High Impedance Circuits

This appendix explains the changes made to the default SPICE simulation parameters, to allow high impedance circuits to be simulated.

The default SPICE simulation configuration in Altium Designer is not suitable for simulating high impedance circuits. The advanced SPICE options must be changed to allow high impedances to be included in the simulation, these options can be found in the mixed-signal simulation setup window. The key parameters for high impedance simulation are: "GMIN" which sets the minimum conductance in siemens of any device as well as the parallel conductance of every pn junction in the circuit, and "RSHUNT" which adds a resistance between every node and GND (Altium Ltd., 2008).

To allow high impedances to be recognised by the SPICE simulator GMIN must be set to $> \frac{1}{|Z|}$ where $|Z|$ is the magnitude of the largest impedance in the circuit. If GMIN is lower than this all conductances which would be lower are given the value of GMIN. For all simulations GMIN was set to 1×10^{-16} S. Having such low conductances can cause the SPICE simulator to produce singular matrices (non-invertible matrices). The presence of a singular matrix stops SPICE

from completing the simulation. Singular matrices can often be prevented by applying shunt resistances from every node to GND using the RSHUNT parameter. RSHUNT was set to $1 \times 10^{15} \Omega$ for all simulations.

Due to the long settling times involved in high impedance circuits it is necessary to adjust the "DC operating point iteration limit" of the SPICE simulator in order for the simulation to converge. The "DC operating point iteration limit" is referred to as "ITL1", and changes the number of iterations SPICE runs to find the DC operating point. ITL1 was set to 4000 for all simulations.

An additional SPICE parameter which maybe useful is "ITL4". ITL4 changes the maximum number of iterations performed at each timepoint in a transient analysis simulation. If an error is recieved when running a transient analysis which states: "doAnalyses: Timestep too small", then try increasing ITL4 until the simulation runs without error.

Appendix B

Sensor Calibration

Tuning the capacitance cancellation gain to give optimal performance requires a steady hand, the right equipment and above all patience! Too little gain and the input capacitance remains too high, too much gain and the sensor becomes unstable! This section describes the effective, systematic method used to ensure tuning was performed accurately and painlessly.

B.1 Laboratory Equipment

The Tektronix AFG3102 function generator, Stanford Research Systems SR1 Audio Analyzer, a low noise 5V power supply and a shielded enclosure were used to perform the sensor calibration. Figure B.1 shows how the equipment was arranged for the calibration.

B.2 Method

The function generator was setup to provide a 60mVp-p sinewave at a frequency of 5kHz. When correctly tuned at 5kHz the output voltage will equal the input voltage, with no phase shift, thus calibration can be achieved by making the output

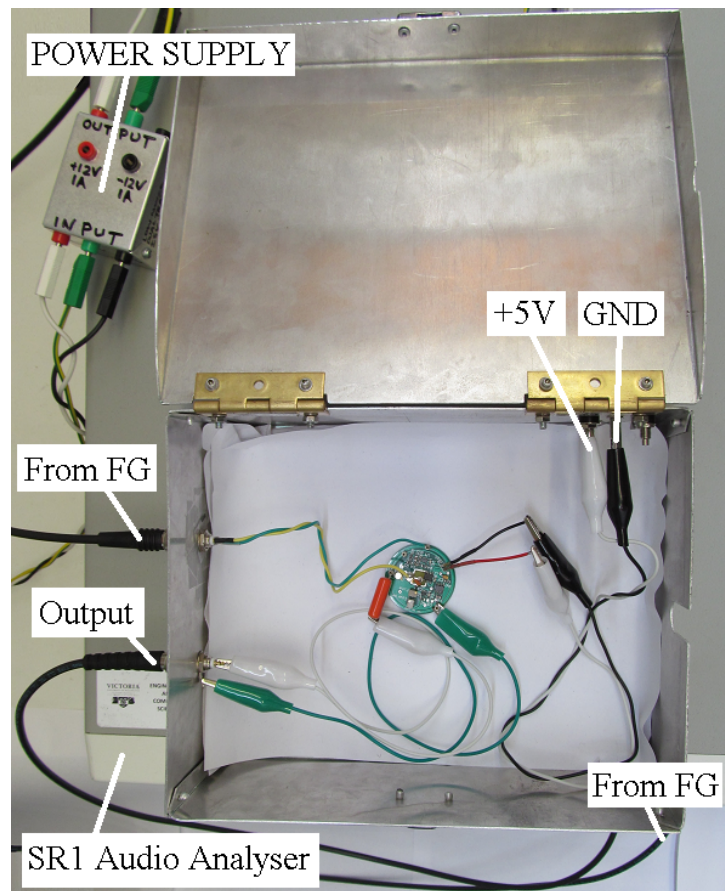


Figure B.1: Laboratory Setup for Sensor Calibration

equal input voltage. The SR1 audio analyzer was used to measure the input and output voltages, and was setup as follows:

- Analyzer: FFT (Dual Channel)
 - Source: Analog
 - Converter: Hi Res ($F_s = 128\text{ kHz}$)
 - Bandwidth: 6.25 kHz
 - Resolution (acquisition time): 8 k (1.02 seconds)
 - Window: Hann

- DC Correction: Average
- Analog Inputs
 - Input Configuration: BNC, Hi Z, DC coupled
 - Range: Auto
 - Hi-Res Converter Sample Rate: 128kHz
- Displays
 - Graph 1: Power Spectrum A and B
 - Graph 2: Time Record A and B

The power spectrum graphs were used to measure the input and output voltages. Resolution of $1\text{ }\mu\text{V}$ was achieved by zooming in on the 5 kHz frequency bin. The time record graphs were used to check that the output voltage had settled to its stable bias level, and that no oscillations were occurring.

Before applying power to the sensor both potentiometers (pots) were set to $0\text{ }\Omega$ s to ensure the sensor output was stable. Prior to calibration the assembly was powered, and signal applied to the sensor for one hour to allow the circuit to reach its stable operating temperature. The following list describes the method used to perform the calibration:

1. Turn $50\text{k}\Omega$ (Coarse) pot half a turn clockwise
2. Replace lid on shielded enclosure, wait for output to settle and check voltage
3. If output voltage is less than input voltage repeat steps 1 - 2
 - Output voltage is now greater than input voltage –
4. Turn Coarse pot anti-clockwise until output voltage is just below input
5. Repeat steps 1 - 3 for the $5\text{k}\Omega$ (Fine) pot
 - Output voltage is now greater than input voltage –

6. Turn Fine pot anti-clockwise by one quarter turn
7. Replace lid on shielded enclosure, wait for output to settle and check voltage
8. If output is greater than input turn Fine pot anti-clockwise by $1/8^{\text{th}}$ turn
9. If output is less than input turn Fine pot clockwise by $1/8^{\text{th}}$ turn
10. Repeat steps 7 - 9 decreasing the amount the pot turns until the output is less than the input by no more than $60\mu\text{V}$. This ensures sensors are matched to $\pm 0.1\%$

B.3 Notes for future calibrators

- To ensure stability at lower coupling capacitances step 10 must be followed explicitly, that is the output should be less than the input. If the output is greater than the input the sensor is over tuned, and low coupling capacitances will cause the output to oscillate.
- Any instrument can be used to perform the voltage measurements, however increased resolution allows sharper tuning.
- Using a standard lab oscilloscope will make fine tuning of the sensor very difficult.
- A configuration file for the SR1 audio analyzer is saved on it's hard drive (CapCancellationTuning.XML)
- when performing steps 7 - 9 as the output voltage gets closer to the input voltage simply touching the pots can alter the gain, be patient, focus and take deep breaths.

Appendix C

Circuit Diagrams and PCB layouts

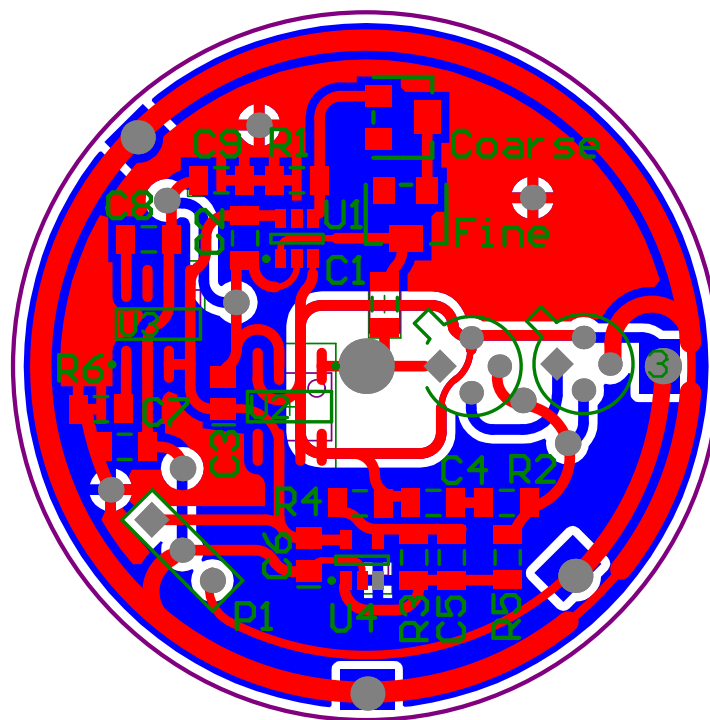


Figure C.1: PCB of Sensor electronics

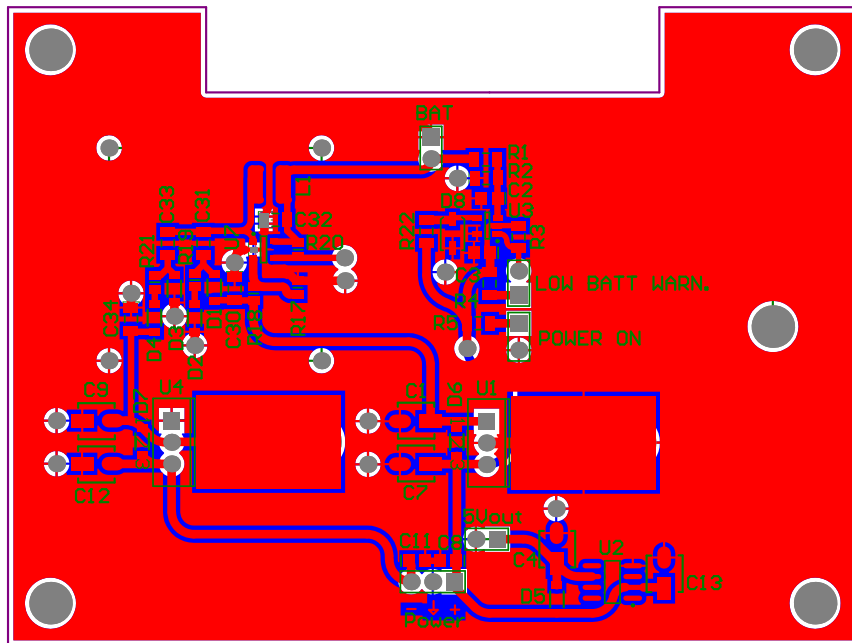


Figure C.2: PCB of differential amplifier power supply

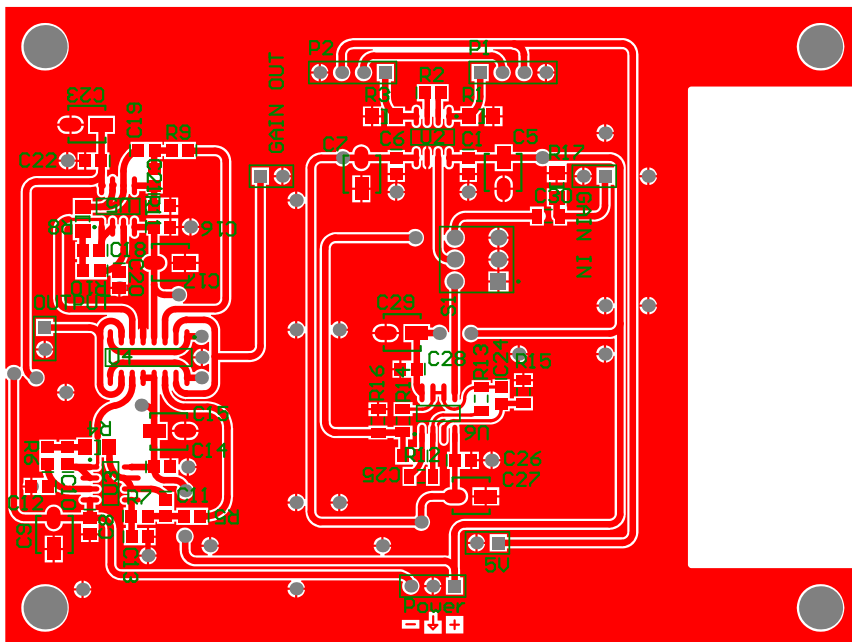


Figure C.3: PCB of Instrumentation amplifier and anti-aliasing filters

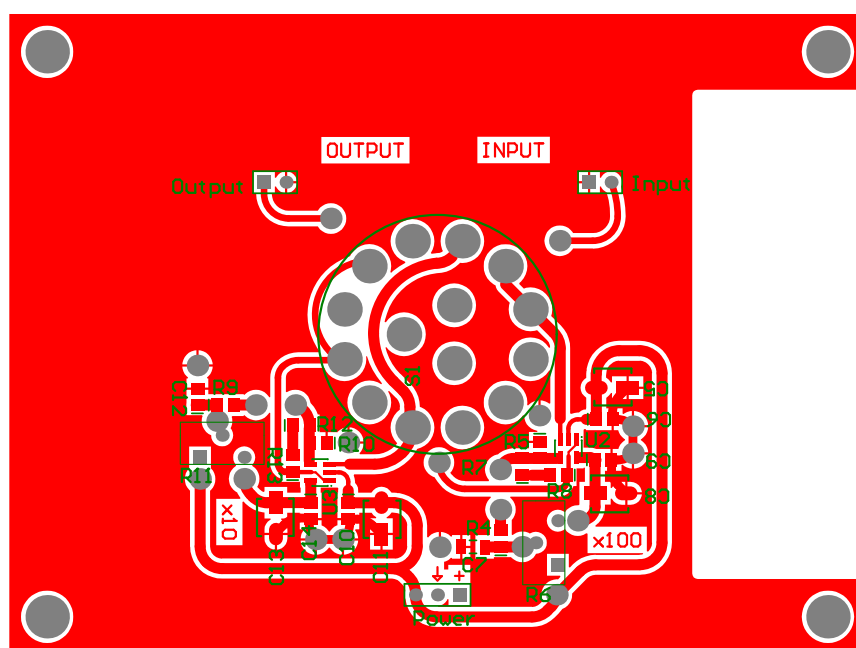


Figure C.4: PCB of high gain amplifier stage

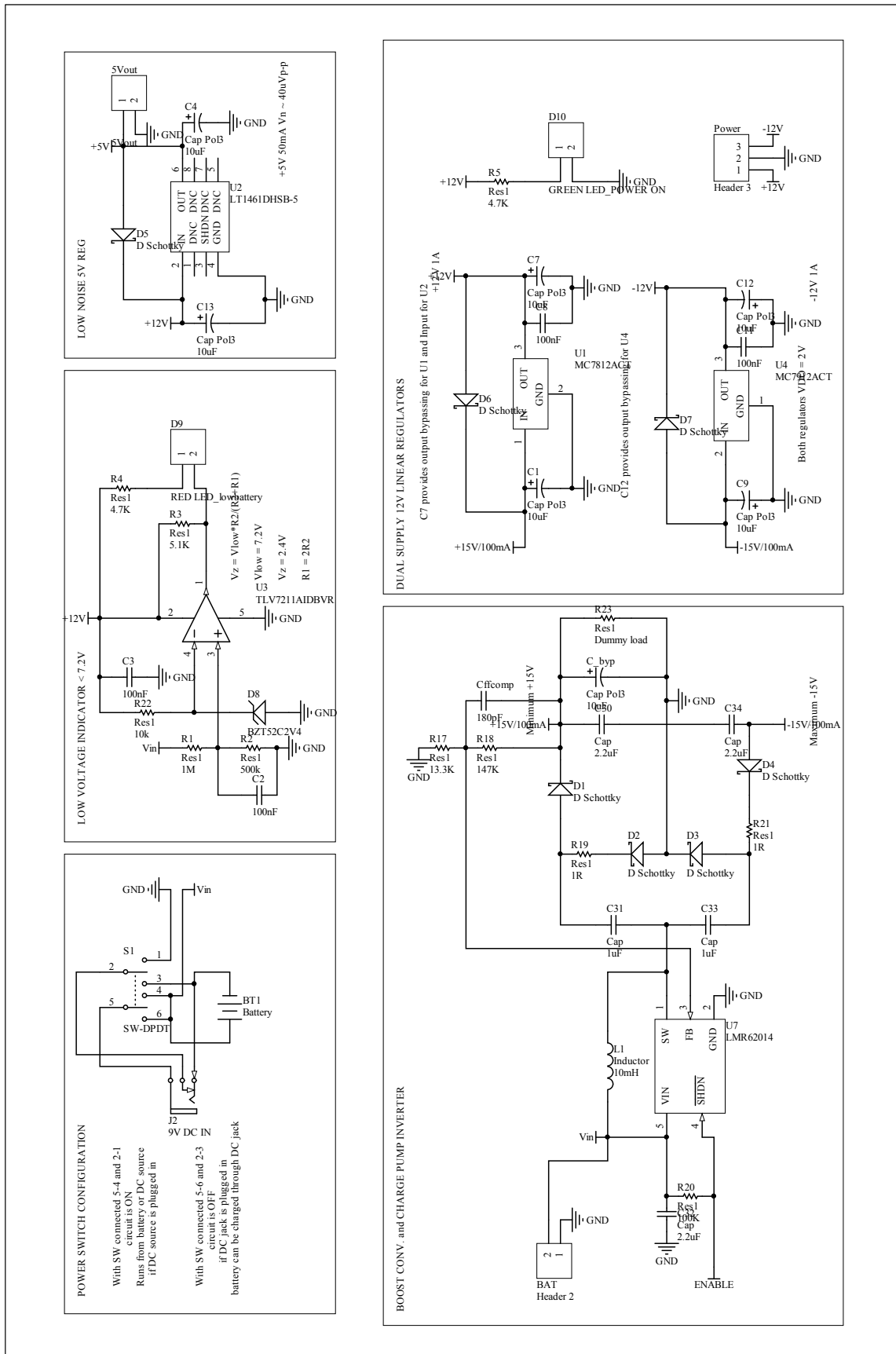


Figure C.5: Power Supply Circuits, from bottom left going clockwise: Power switch, battery monitor and low voltage indicator, low noise 5V regulator, $\pm 12V$ power supplies, Boost converter and charge pump inverter.

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