**Spatial network conduction in
carbon nanotube and
Ag–Ag₂S–Ag atomic switch
network device platforms**

by

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Abstract

Networks of nanomaterials sit at a confluence of desirable features for the fabrication of advanced electronic devices, including facile fabrication, high conducting element density, and novel electrical characteristics. The spatial conduction through carbon nanotube (CNT) and Ag–Ag₂S–Ag atomic switch networks was investigated to determine how better to implement them in novel sensing and computation device platforms.

Selective gating of localized regions of CNT networks with varying densities was investigated. To achieve this, lithographically defined FET structures were developed that allowed gating of localised regions of the CNT FET network area. The CNT FET device sensitivity to gating of different regions of the CNT network was measured for devices with network densities close to the percolation threshold. A 10^2 increase in sensitivity to local gating for CNT FET devices with low network densities was observed compared with high-density CNT networks. Network densities were all well below a density where metallic shorts could be present, so the trends observed were attributed to m-s junction dominated gating of the network. A better understanding of the dominant conduction in CNT network FETs at low network densities is important for tuning their properties for use as novel biosensing platforms or a tunable connectivity conducting film.

A CNT network simulation was developed to test the effects of local gating on networks of bundled CNTs with varying densities. Up to 70,000 bundles on a 60 μm x 60 μm simulated network area were used to generate an electrical network of field sensitive elements where the gate field could be spatially modified to investigate the effect of local gating. Monte Carlo methods were used to simulate large numbers of random networks with m-s junctions as the dominant gate-dependent element. Networks with 13.5% metallic bundles were shown to exhibit trends in local gating similar to the experimental systems. Current density maps showed key conduction paths in low-density

devices, which supports a model of m-s junction dominance to explain the local and global gate responses measured in experimental CNT FET systems.

Prototype Ag–Ag₂S–Ag atomic switch networks (ASN) device were fabricated using spray-coated silver nanowires which were sulfurised using gas-phase sulfur after deposition. Electrical formation of memristive junctions and hysteretic switching curves were shown under swept voltage bias demonstrating memristive behaviour. ASN devices have been demonstrated to show critical dynamics and memristive characteristics due to the complex connection of atomic switches formed at Ag–Ag₂S–Ag junctions between wires

A fabrication and measurement protocol for ASN based neuromorphic devices on multi-electrode array (MEA) platforms was developed. The electrical measurement system was designed and deployed to facilitate time-resolved measurement across multiple channels simultaneously on those MEA platforms. Under DC bias, MEA-based ASN devices showed switching events with a power-law distribution over two orders of magnitude of conductance changes and time intervals consistent with self-organized criticality within the network. The dynamic response of the critical system was measured across the network area. Changes in the relative voltage across the ASN network area were observed using 16 channel MEA platforms, showing spatiotemporal variation in voltage across the network. Novel application of principal component analysis to ASNs was used to demonstrate reduction of dimension while preserving relative voltage changes. This paves the way for scalable analysis of the complex dynamic signals from critical ASN systems.

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I don't know anything, but I do know that everything
is interesting if you go into it deeply enough.

Richard Feynman

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Chapter 1

Introduction

Network systems provide an alternate computing paradigm where the focus is shifted from improvement via miniaturisation, that has dominated modern transistor-based computing since the 1970's [1], to a model of improvement via complex interaction [2]. Electronic systems based on complex networks of nanomaterials draw inspiration from biological network systems such as the human brain, where computation is achieved by the distributed activity of massively interconnected but slow neurons [3], rather than centrally controlled and sequentially operated transistors. Software-based neural networks have exploded into widespread use and the public consciousness in recent years, highlighted by the defeat of a human grandmaster by Google's AlphaGo in 2015 [4], but are still inherently limited by the transistor-based hardware that they run on. Hardware implemented network systems that are engineered with network structures that are inherently neuromorphic allow a more closely matched, and thus efficient, realisation of biologically-inspired network systems. Such systems have the added benefit that rapid and scalable solution-based fabrication of nanomaterials are particularly suited to the fabrication of network structures [5, 6].

The motivating goal at the genesis of this project was to leverage the key benefits of nanomaterial-based electronic systems to fabricate an integrated device composed of two different networks of nanomaterials: An atomic switch network (ASN) layer which would be used to generate dynamic and complex electrical signals for computing, and a network of carbon nanotubes (CNTs) that would be used for local modulation of the

electrical connectivity in the device. When fabricated into a two-layer device, the CNT layer could provide direct control of current through regions of the ASN network layer, potentially allowing modulation of the ASN switching. In the course of researching CNT and ASN based electrical systems it became apparent that, while there existed significant research on the component CNTs and atomic switches [7], as well as a clear application for a combined device as a computational platform [8], the understanding of the interactions within each network would need to be extended before the fabrication of a device integrating both.

The substantial research on CNT networks as field effect transistors (FETs) [5] has led to their use in integrated logic circuits [9], memory elements [10], and chemical [11] and optical sensors [12]. However, the model which is predominantly used to explain their operation needs to be improved to account for the effect of network topology on gate-dependent conduction. The effect of localised gating on CNT networks of varying density was investigated with a focus on the CNT-CNT interactions that literature work [13–15] suggests cause the density-dependent gating observed here. Schottky barriers at junctions between metallic and semiconducting CNTs is proposed as the dominant mechanism behind local and global gate dependence. A CNT FET network simulation was designed and implemented with m-s junctions set as the gate-dependant elements. The trends in local and global on-off ratios from the physical devices agreed qualitatively with those found in simulation, supporting the dominance of metallic-semiconducting junctions on gating.

Demis et al. [16] have shown that the dynamic signals generated by switching within Ag_2S ASN devices are applicable to biologically-inspired computing. I adapted the fabrication of these devices from literature [17], and designed and implemented an in-house system for measuring their dynamic electrical properties. To verify my capability to fabricate these ASN devices I measured and analysed electrical switching above a voltage threshold, characteristic of ASN [6]. Temporal analysis of ASN systems using thresholding and event analysis was inspired by the biological analysis of neuronal systems [18–20]. The observed switching dynamics were characterised by a critical network state that causes distinctive spatiotemporal signal variation [21]. The event analysis demonstrated power-law scaling characteristic of network criticality within the ASN devices measured.

The application of those critical dynamics hinges on accessing multiple different signals from within the network[22]. I applied principal component analysis as a novel technique applied to ASN systems. Principal component analysis of the voltages measured across the network area was used to reduce the dimensionality of the spatiotemporal voltage signals, paving the way for scalable analysis of the large and feature-rich spatial variation in signal across critical ASN networks.

The work in this thesis paves the way for building an integrated CNT and ASN device by designing device platforms to enable investigation of the conduction within both network systems and using them to build better models and analysis systems to characterise these complex network systems. In the case of CNTs, an improved model for how gating within the network affects overall performance was proposed based on local gating of CNT network devices and tested using a simulation designed around the model proposed. Building the capability to fabricate ASN devices, and developing tools to analyse their spatiotemporal dynamics, has provided a system for future comparison of integrated CNT and ASN devices. Realising hardware-based biologically-inspired systems competitive with silicon-based transistor technology will require further work both on device fabrication and understanding of the network systems. This thesis has provided devices and models of the systems studied that provide a step forward towards biologically-inspired computation paradigms.

1.1 Thesis overview

This thesis encompasses research done onto two distinct network systems initially motivated by a future device combining both. The background, methods of fabrication and characterisation, and results are presented for CNT field effect transistor (FET) systems and ASN devices respectively as well as a chapter on the results of the simulation of a CNT network system. A breakdown of these chapters is presented below to give an outline of the thesis content.

Chapter 2: Carbon nanotube field effect transistors

Chapter 2 introduces CNTs and CNT FET systems, and gives a background of the current material and device application research in the literature. The prevalent approach to percolating metallic shorts in CNT network conduction literature is explored. Existing research on the mechanism of conduction at CNT junctions and their importance to CNT network conduction demonstrates a need for better understanding of the junction effect in gating of CNT networks.

Chapter 3: Fabrication of locally top-gated CNT FET device platforms

The methods used to fabricate network CNT FET devices that can be gated via both global back gate and local top gates are described in Chapter 3. The photolithographic processes developed to enable fabrication of the multiple stacked layers necessary for patterned top gates are then detailed.

Chapter 4: Local top gating of random network CNT FET devices

Density varying CNT network devices are measured, and their top gate response is compared in Chapter 4. An analysis of the film density and uniformity is performed by stick fitting to AFM images which are compared with results from classical stick percolation. The size of the bundled CNTs is used to determine the percentage of metallic components in the network. The on-off ratio across gate types is compared for CNT networks with density from 4 bundles/ μm^2 to 20 bundles/ μm^2 and demonstrates that top gates show sharp improvement at low on-off ratios compared with gradual improvement using back gates. The variation in the on-off ratio is attributed to m-s junctions dominating gating via topology induced key conduction paths.

Chapter 5: Simulation of junction dominated random network CNT FET devices

Chapter 5 begins with a description of the algorithm developed to simulate the formation of random CNT networks and their gate-dependence. M-s junctions are assumed to provide the only significant gate-dependence as suggested in Chapter 4. The trends

observed in on-off ratios with network density in experimental devices are compared with the simulated results. Qualitative agreement between simulation and experiment supports the dominance of m-s junctions in key conduction paths dominating gating.

Chapter 6: Fundamental concepts and current research on atomic switch networks

The importance of biologically-inspired computation and its implementation in hardware is expanded in Chapter 6. Research on atomic switches as nanoscale memristive elements is used to describe their switching mechanism and artificial synaptic properties, as well as recent work in Ag_2S ASN systems for biologically-inspired computing. Key concepts relevant to this work on ASN systems are introduced including: Properties of memristors and atomic switches, self-organised criticality characteristic of complex internal switching dynamics, and principal component analysis used for analysis of high-dimensional data.

Chapter 7: Fabrication and measurement of atomic switch networks

Chapter 7 describes the adaptation and optimisation of fabrication techniques for fabricating Ag_2S ASN devices from literature. Multiple solution-based fabrication methods are investigated, and spray deposition of silver nanowires is selected for this work. The chip design and electrical measurement setup that was designed to allow characterisation of ASN devices is detailed.

Chapter 8: Ag– Ag_2S –Ag atomic switch network devices

Chapter 8 details the measurement and analysis of the ASN systems used here. Proof of concept devices were demonstrated to form metallic filaments across the network consistent with the literature [7, 17]. Subsequent network switching is shown to be unstable due to internal switching dynamics. These internal dynamics are characterised using switching event analysis to demonstrate self-organised criticality within the system. Finally, the distribution of the dynamic events is spatially analysed by applying principal component analysis as a novel technique to ASN devices. PCA applied to multi-channel

voltage signals measured from across the ASN device area shows evidence of switching in a reduced dimensionality representation suitable for scaleable future analysis.

Chapter 9: Conclusions and future work

The key results of this thesis are summarised in Chapter 9 to highlight its contribution to the importance of m-s junctions in dominating gating in varying network densities, analysis of the spatiotemporal data produced from critical ASN systems, and the body of knowledge surrounding conduction through complex networks of nanomaterials. Future extension of this work, as well as the application of the techniques developed herein are discussed.

Chapter 2

Carbon nanotube field effect transistors

This chapter outlines the electrical properties of carbon nanotubes (CNTs) that make them ideal candidates for use as the active material in field effect transistor (FET) devices. The importance of research on single and crossed CNT devices in probing the conduction and gating of CNT systems is examined despite their limited application due to difficulty in mass fabrication [23, 24]. Existing research on network CNT devices, which are readily scaleable, is then examined with particular focus on the challenges in producing devices that exhibit high on-off ratios due to the mixture of CNT chiralities present [25, 26].

Random stick percolation is used throughout the literature to explain the variation in the performance of random network CNT FETs [27–30]. We introduce percolation theory and examine its application to physical CNT systems. The use of percolation theory in the literature in determining the contributions to the conduction of metallic and semiconducting CNTs within a network is discussed to determine its continued relevance to the analysis of CNT networks.

The existing research in the literature on CNT network devices fabricated using purified CNTs optimises device performance by reducing metallic tube conduction paths. We describe literature that is placing more emphasis on the junctions between metallic and semiconducting CNTs [31, 32]. This work builds on that research, attributing changes

in switching at low network densities to key junctions in the CNT network. The physics behind the Schottky junctions that are formed between metallic (m) and semiconducting (s) CNTs and the evidence in the literature for their dominance of conduction and gating in CNT networks are presented [15, 31].

I conclude by motivating the work in Chapters 4 and 5 using fabricated CNT FET devices and a gated CNT network simulation respectively. Further understanding of the role of m-s junctions within random CNT network topologies is essential to build on the understanding in the literature of the spatial conduction through CNT network systems.

2.1 Carbon nanotubes (CNTs); chirality and conduction

Carbon nanotubes are hexagonal arrangements of carbon atoms in a graphene-like sheet that have been rolled into a tube [33]. This work is concerned solely with single-walled carbon nanotubes, where there is only a single sheet of carbon atoms forming the tube, in contrast to multiwalled CNTs where multiple sheets of carbon are nested inside one another. Unless specifically mentioned, CNTs will refer to single-walled carbon nanotubes. CNTs elegantly embody a physically realisable one-dimensional conductor by restricting the ballistic transport properties of graphene to a single direction along their length [33].

CNTs show markedly different conduction properties along their length depending on the orientation of the carbon lattice with respect to the axis of the tube (chirality). The orientation of the carbon lattice is shown in Figure 2.1 (a) as a vector (n, m) which is the position of the vector along the two principal vectors denoted $(\hat{a}_1, \hat{a}_1)$ in Figure 2.1 (a) vectors which describe the tiling symmetry in a hexagonal lattice. There are two symmetric vectors denoted as the $(n\hat{a}_1, 0\hat{a}_1)$ zigzag vector shown in red, and the $(n\hat{a}_1, \hat{a}_1)$ armchair vector shown in blue. All other vectors are chiral, or have vectors that are between zigzag or armchair of the form $(n\hat{a}_1 + m\hat{a}_1)$. Rules for the conduction properties of the tube based on its chiral vector can be determined by examining the restriction of possible electron states in graphene. The chiral vector of the CNT denotes the direction of allowed conduction along the length of the tube and imposes restrictions on the allowed electronic states [33]. Chiral vectors with $n - m \neq 3z$ are semiconducting and

Figure 2.1: The chiral vector of a CNT with respect to the carbon lattice is shown in (a). The zigzag (red), armchair (blue), and an example chiral (Ch) vector are shown. (b) and (c) show the calculated density of states for a semiconducting and metallic CNT respectively and have been reproduced from Mintmire and White [34].

$n - m = 3z$ are metallic for integer z with example density of states (DOS) shown in Figure 2.1 (b) and (c) respectively [34]. The zero DOS at the Fermi level, $\Delta E = 0$, shown in Figure 2.1 (b) demonstrates semiconductor behaviour due to carriers having to be excited above the band gap to conduct. The non-zero DOS at the Fermi level shown in Figure 2.1 (c) demonstrates metallic-like conduction due to free carriers being present without the need for any excitation above a band gap. For the remainder of this work, the terms metallic (m) will be used to refer to CNTs with zero bandgap and semiconducting (s) or (s') will be used to denote those with a bandgap. There is variation in the band structure of semiconducting CNTs with different chiralities (s and s') [33, 35]. Schottky junctions form at m-s junctions between CNTs while heterojunctions form between semiconducting CNTs with differing bandgaps s-s' [13, 33, 36, 37]. The models used in Chapters 4 and 5 do not incorporate the variation in bandgap between semiconducting CNTs, consistent with research on CNT FET systems in literature [5, 31].

2.2 Description and properties of field effect transistors (FETs)

FETs are a class of three-terminal transistor devices with the most common type being the metal oxide semiconductor FET or MOSFET widely used in integrated circuits for processing, memory and power applications [38]. FETs are composed of the control terminal, which is called the gate, acting capacitively on the conducting channel to control the conductance between the source and drain as shown in Figure 2.2. FETs differ from other transistor architectures in the way that their gate (G) modulates the conduction between the source (S) and drain (D) terminals. In an ideal FET, the gate contributes no current to the device channel and only acts capacitively on the conducting channel to change the electric field across it.

Figure 2.2 (a) shows a simplified schematic of a back-gated CNT FET device. The source, drain, and gate electrodes are labelled S and D respectively as per the standard notation and were fabricated by depositing patterned chrome/gold on top of the CNT film. The CNT film, an AFM image of which is shown in Figure 2.2 (b), is shown in red, bridges the source and drain electrodes, and is the region of the device where conduction is modulated by the gate field. The device is fabricated on top of a degenerately n-doped, Si substrate which acts as the device gate. Degenerative doping refers to the implantation of a large proportion some donor element, usually phosphorous for n-type doping, giving the semiconductor conductivity comparable to a metal. The back of the device had a layer of gold deposited on it to improve electrical contact. A 300 nm layer of native SiO₂ on the surface of the wafer acts as the gate dielectric. The use of thermal oxide on a Si wafer as the back gate is typical of back-gated CNT devices in the literature [39–41]. The fabrication of a back-gated CNT FET is the first step in the fabrication of the multi-gate CNT FET devices used in Chapters 3 and 4. The silicon substrate shown in Figure 2.2 (a) acts as the back gate for the device, so that when a gate voltage V_G is applied to the back gate electrode (G), an electric field is created in the channel, but ideally no current flows. The current flowing from source to drain across the channel I_{DS} is solely due to the driving voltage between the source and drain V_{DS} and the conductivity of the channel. The current measured should thus only reflect a change in conductance in the

Figure 2.2: Diagram showing a simplified layout for a back-gated CNT FET device. (a) the CNT film is shown on top of a SiO_2 capped silicon wafer. The source (S), drain (D), and gate (G) electrodes are shown contacted to the CNT film and the substrate respectively. The electrical connections are shown for the driving voltage V_{DS} , gate voltage V_G , the source-drain current measured I_{DS} , and ground. (b) an AFM image of a small portion of the CNT film is shown.

film brought on by the electric field caused by V_G . Any current that does pass through the gate dielectric is termed leakage current and is always undesirable for device operation.

2.2.1 Electrical properties of field effect transistors

A FET is characterised by a metrics determined from electrical measurement which describe its electrical performance. Most important for this work is the ability to switch I_{DS} between a high current (on) and a low current (off) state by varying the gate voltage. The two measurements that are predominantly used to electrically characterise FETs are output and transfer measurements. Output measurements are performed at a constant gate voltage, while the source-drain voltage is swept [38]. Figure 2.3 (a) shows a series of output measurements where V_{DS} was swept from -5 V to 5 V while V_G was fixed between -20 V and 20 V . Output measurements provide information on the linearity of the current response of the device channel at different voltages. They are presented here for completeness to show an example of the V_{DS} dependence of the devices

Figure 2.3: Example of three terminal electrical measurements on a back gated random network CNT FET. (a) shows output curves where V_{DS} is swept from $-5 V$ to $5 V$ and V_G is held at $-20 V$, $-10 V$, $0 V$ and $20 V$ for each curve as labeled. (b) transfer characteristics sweeping V_G between $-20 V$ to $20 V$ while V_{DS} was held at $100 mV$.

measured. Transfer measurements are performed at a constant driving voltage across the source and drain while measuring the change in I_{DS} due to the swept gate voltage [38]. Figure 2.3 (b) shows a transfer measurement on a back-gated CNT FET device where $V_{DS} = 100 mV$, and the gate voltage is swept from $-20 V$ to $20 V$ and back down again. Arrows in the current curve denote the direction of the voltage sweep as the current varies from $20 nA$ to $\sim 10 pA$.

Hysteresis in CNT FETs

The difference in the forwards and backwards sweep shown in Figure 2.3 (b) is called hysteresis and is a well-known phenomenon in CNT FETs and many other transistor systems [38, 42]. Hysteresis in CNT FET systems is caused by charge traps near to the CNTs [43]. For CNTs on a SiO_2 substrate, the charge traps are primarily due to absorbed water on the surface as both loosely bound H_2O and silane ($Si-OH$) groups [43–46]. At a negative gate voltage, electrons are wicked into the CNTs from the surrounding water leaving ionised H^+ in the silane and water. These traps persist as the voltage is swept to

positive, causing an enhancement of the gate voltage, which results in off switching at lower voltages. Conversely at high voltages electrons are injected into the bulk SiO₂, and trapped there. The trapped electrons screen the gate voltage as it is swept back towards the negative resulting in a higher on switching voltage.

We do not use the hysteresis in our measurements as a metric for the CNT FET device performance, as this work is primarily concerned with the magnitude of the gating effect. It is described here for completeness as all experimental devices measured show hysteresis to varying degrees. If the hysteresis is not desired in future application it can be passivated using polymer capping layers, and baking steps to remove the water-based charge traps and the ability for charge to be injected into the bulk silicon [43].

On-off ratio of FETs

The conduction properties of the FET can be directly obtained from the electrical measurements shown in Figure 2.3. Of primary significance here is the on-off ratio, as it describes the magnitude of change in current caused by varying the gate voltage. The on-off ratio is used here as a comparative metric, where devices with the same electrode and dielectric fabrication are directly compared using their respective on-off ratios. Higher on-off ratios are desired for switching [47] and sensing [11]. For computation, a clear difference between on and off current is necessary to denote logic 1 and 0 [48], and in sensing application, a high on-off ratio is used to detect small electrical changes in the FET in the presence of the analyte [11].

The maximum and minimum source-drain current measured in the transfer curve, as shown in Figure 2.3 (b), are defined as the on and off-currents I_{on} and I_{off} respectively. The on-off ratio is defined as I_{on}/I_{off} and is a measure of the magnitude of the FET's ability to switch under gate bias. It is often given in orders of magnitude, so for example in Figure 2.3 the device shown has an on-off ratio of 10^4 . Network CNT devices in the literature achieve on-off ratios of 10^6 when CNTs which were purified to have > 99% semiconducting CNTs from the conducting channel, and $\sim 10^3$ for devices using as-grown CNTs with 66% semiconducting CNTs [5].

The on-current is determined by the overall density of CNTs in a network, while the off-current is limited by the density of metallic CNTs present due to their inability to be

switched 'off' causing shorts through the network [5]. The metallic tube content in network CNT FET devices is thus central to producing high on/off devices. This work uses on-off ratios as the primary metric for exploring the impact of the junctions between metallic and semiconducting CNTs rather than the impact of metallic shorts in Chapters 4 and 5.

The threshold voltage V_{Th} , transconductance g_m , and mobility μ are all standard metrics obtained from the transfer characteristics and are described here for completeness.

Threshold Voltage V_{Th}

The threshold voltage is defined as the voltage at which the device begins to switch on from the off state, and is measured by fitting a line to the linear portion of the transfer curve and taking its intercept with the minimum current [49]. The threshold voltage is thus a measure of the barrier that must be overcome before switching can begin, which for semiconductors can be related to the bandgap above which charge carriers are available for conduction within the device channel [38]. For CNT FET devices it can be taken as a measure of the Schottky barrier height which is discussed in further detail in Section 2.4.3

Mobility μ

The mobility can be calculated using the following equation [50]

$$\mu = g_m \frac{L}{W} V_{DS} C \quad (2.1)$$

where L and W are the lateral device length and width respectively. V_{DS} is the driving voltage, C is the gate capacitance per unit area, and g_m is the transconductance. The transconductance is defined as the rate of change of the output current with the gate voltage $\frac{dI_{DS}}{dV_G}$, which can be measured from the gradient of the transfer curve shown in Figure 2.3 (b). It is typically taken as the maximum value of that slope for the device.

Network CNT FET mobilities tend to be $10 \text{ cm}^2/\text{Vs}$ to $20 \text{ cm}^2/\text{Vs}$ [12, 26, 51, 52], 2-3 orders of magnitude lower than a single CNT FET devices which have been shown to have mobilities of $79\,000 \text{ cm}^2/\text{Vs}$ [53].

2.3 Carbon nanotube field effect transistors in the literature

There has been extensive research into CNTs as novel electronic materials, with the first CNT FET demonstrated in 1998 by Tans, Verschueren, and Dekker [24], and research continuing unabated to the present [9, 10, 12, 13, 15, 23–26, 32, 43, 44, 46–48, 50, 52–104].

There is extensive work on the use of CNTs in FET devices particularly for their attractive electrical characteristics such as mobilities of $79\,000\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ [53] and switching speeds of $\sim 50\text{ GHz}$ [23] in single CNT devices. Research on CNTs as gas and liquid sensing systems leverages the fact that conduction is inherently a surface property in CNTs, which have no bulk, making them very sensitive to their surrounding environment [11, 12, 56, 65, 74, 102, 103, 105–110]. Thin films of randomly oriented CNTs benefit from more scaleable fabrication processes. Thin film networks of CNTs have been used to fabricate FETs with on-off ratios of $>10^3$, and mobilities of $\sim 10\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ [25]. While these metrics not as impressive as single CNTs, the scalable solution processing has seen them applied in integrated circuit and sensing platforms [10, 11, 26, 47, 51, 56, 74, 102, 103, 110].

2.3.1 Single or crossed CNT devices

Single CNT devices and devices composed of two crossed CNTs have been and continue to be used for their high mobility and on-off ratios, and their lack of obfuscating factors when studying the electronic properties of CNTs [13, 15, 23, 24, 43, 46, 54, 59, 66–68, 71, 76, 78, 86, 88, 98, 104, 111–116]. The most straightforward device structure for electrically measuring a single CNT or crossed CNT system is a back-gated FET. The CNT(s) rests on top of a degenerately doped silicon wafer capped with a layer of SiO_2 which acts as the gate dielectric [13, 15, 24, 44, 53, 54, 68, 71, 76]. Such an arrangement has allowed extensive study of the conduction and gate-dependence of controlled systems of CNTs.

Foundational work by Fuhrer et al. [13, 68] used crossed single CNTs to measure the electrical properties of the junction between tubes. They measured linear ohmic behaviour between two crossed metallic CNTs, and two crossed semiconducting CNTs. The crossed metallic and semiconducting CNT measured showed nonlinear current re-

sponse consistent with a p-type Schottky junction being formed at the m-s junction [68]. Their work has been pivotal in understanding the properties at the junctions between CNTs and is often cited in the literature as a source of measurement for the resistances of m-m, m-s, and s-s' junctions, as well as the presence Schottky barriers formed at m-s CNT junctions.

Lee et al. [15] showed conclusively using scanning photocurrent microscopy (SPCM) while gating the whole network that the barriers to conduction were localised to the m-s junctions within the network. SPCM measurements on crossed nanotube junctions were used to measure dissociated electron-hole pairs that were photo-excited at local electric fields present at transport barriers. Their initial work on sparse networks highlights that in the on-state, barriers to conduction exist at the electrode contacts, as well as some junctions in the network. When the CNT networks were gated off, they observe only junctions within the network as conduction barriers. They confirm this by taking SPCM of crossed m-m, s-s' and m-s junctions, showing that the photocurrent response of the junctions dominates in the device off-state. They attribute the dominance of those junctions within the network as opposed to the electrodes to flattening of the Schottky barriers at the electrodes, which does not occur between CNTs at positive gate voltage [15, 68].

The work on single and crossed CNTs in the literature provides a simple platform for the investigation of the properties of CNTs. However, the fabrication of device contacts to single CNTs requires the use of electron beam lithography, which offers unparalleled feature size and accuracy but is inherently non-scalable. The need to 'write' the pattern desired by scanning an electron beam means that it is unfeasible for large or repeat patterning. A large section of the literature thus is focused on larger scale CNT structures such as ordered arrays or random networks of CNTs in a film [10, 11, 26, 47, 51, 56, 74, 102, 103, 110].

2.3.2 Network CNT devices in the literature

Electronic devices fabricated from networks of CNTs show significant potential for application due to their scalable fabrication and device properties which, while they do not

rival single CNT devices, have been shown to be suitable for extensive fundamental and applied research [9–12, 23, 26, 47, 51, 52, 58, 66, 73, 96, 110, 117].

Networks of CNTs can be fabricated more readily than single CNT devices due to their scalable processing. Networks of CNTs can be fabricated by growing large numbers of tubes directly on the substrate [14, 25, 58], or using solution-based methods to deposit pre-grown CNTs on to the substrate. Solution deposition methods such as inkjet printing [5, 51] and directed transfer using surface functionalisation [26, 52, 84, 85, 87, 91], have spurred research into using CNT TFTs as a scalable fabrication path for continued device application research [10, 48, 51]. These networks have been fabricated at wafer scale [70], or restricted to regions on the order of a single tube length, offering scope for tailoring of the film size to the requirements of the desired application.

Here commercially available CNTs fabricated by arc discharge are used, which are sorted using density gradient ultracentrifugation (NanoIntegris IsoNanotubes-s) [55]. The method of CNT film fabrication used here is detailed in Chapter 3. The literature on the fabrication of CNT networks uses many specific methods, but all must grapple with the same difficulties inherent in collections of CNTs.

The main challenge in using networks of CNTs is optimising a device system where there is no longer deterministic control of the elements involved. CNT networks, whether grown on the surface or deposited post-growth by some method, are inherently random arrangements. Variation in conduction characteristics between CNTs with different chiralities, and the significant impact of junctions between CNTs on conduction, has motivated this and other work to investigate the impact of these differing CNTs and junctions on the conduction and gating behaviour of network systems.

One of the most significant challenges faced in using CNTs is the 1:2 ratio of metallic to semiconducting CNTs that are produced during growth [118]. Devices fabricated from these as-grown CNTs suffer from high off-currents, resulting in low on-off ratios [25]. Research has been done on mitigating this challenge by altering the network after fabrication to remove the metallic CNTs with selective burnoff with high currents [63] or etching the network with photolithographically defined patterns to disrupt the metallic conduction paths [58, 60, 62, 90].

Purifying CNTs to tune the composition of a network before it is deposited allows a

far more controllable approach to improving the electrical characteristics of networks of CNTs. Research on CNTs purification has yielded a number of methods using selective polymer wrapping [119], gel-chromatography [120], and density gradient ultracentrifugation [55]. These techniques allow the fabrication of CNT devices using samples of CNTs that have been selected for such properties as length, diameter, or chirality. The purification of as-grown CNTs has enabled the fabrication of devices with networks comprised of tubes with semiconducting concentrations over 99% showing improved device characteristics [48]. Higher mobilities and on off ratios have allowed increased performance in transistor structures such as gigahertz ring oscillators [47], logical integrated circuits [9], stable memory arrays on flexible substrates [10]. High sensitivity real-time biosensors leveraging the increased on-off ratios have been fabricated using networks of purified CNTs [11, 102, 103]. Takahashi et al. [12] have used films of CNTs as high mobility transistor elements with organic polymer-based photodiodes to produce 18x18 pixel(1mm pitch) optical light sensors on flexible substrates.

Rouhi, Jain, and Burke [5] have presented a clear analysis of the hurdles that must be overcome to enable informed optimisation of CNT FET systems using solution based fabrication techniques. Relevant to this work, they identify the importance of density on the "critical performance parameter" of on-off ratio but go on to describe the well-known model of metallic CNTs causing low on-off ratios by limiting the off-current possible. They then highlight the network density regime where the network conducts but the metallic CNTs do not cause shorts across the network area. They then point out how the development of devices with purified CNTs where the metallic tube concentration can be $\geq 99.9\%$ makes this regime more feasible to engineer.

In order to better understand this sub-metallic percolation regime, the network makeup must be understood. One of the most prevalent theory approaches has been to model the device using a stick percolation model [121]. Stick percolation is most often referenced to explain the optimisation of the electrical performance of CNT networks by varying such parameters as tube morphology and conductivity, device area, and network properties such as density and alignment [27–30].

2.3.3 Percolation theory and its application to CNT networks

Percolation theory is very general and concerns the properties of the connected clusters that occur in random systems. An excellent introduction to the concepts can be found in D and A [122]. The focus of this work will be on stick percolation systems specifically, where the position of the sticks and their orientation are randomly selected. The classical stick percolation model is described in Pike and Seager [121], and their results are used here.

Consider a two-dimensional system of size $\ell \times \ell$ sticks that have equal length L and a random position and orientation. Sticks are connected if the line segments that describe them overlap. Sticks that are connected to one another via a path through other connected sticks are considered to be a part of a connected cluster. A spanning cluster is defined as a connected cluster that contacts opposite edges of the system boundary, although it can be defined between any non-adjacent edges in principle. Without a spanning cluster of conducting elements from one edge of a system to the other conduction is not possible. This work adopts the notation most common in the literature on CNT networks [30, 32, 72], where the percolation threshold ρ_{Th} is the density above which a spanning cluster can exist. ρ_{Th} can be calculated for a system with stick length L using:

$$\rho_{Th} = \frac{4.236^2}{\pi L^2} \quad (2.2)$$

where the constant 4.236 has been determined numerically up to ± 0.001 for this system by performing Monte Carlo analysis of many random systems with varying stick densities [121].

The probability of a connected cluster occurring increases towards one above the percolation threshold. It is important to note that Equation 2.2 describes a system where the dimensions of the system $\ell \gg L$ and L is constant. In general, this does not perfectly describe a physical system of CNTs, which will have some finite boundaries and variation in the length of CNTs. Li and Zhang [123] show that a finite square system broadens the transition region from non-connected to connected devices with increasing density. They show significant broadening up to $\sim 20\%$ of the percolation threshold value. Additionally Hicks, Behnam, and Ural [27] show that length variations have the

effect of shifting the percolation threshold to densities $\sim 10\%$ below the classical ρ_{Th} .

Experimental studies on the optimisation of CNT TFTs follow a similar vein of focusing on the device geometry and network density and semiconducting percentage as levers for optimisation with success [32, 69, 72, 79]. In studies of the switching characteristics of random network CNT FET devices, poor on/off ratios has been attributed to high off-currents caused by percolating metallic conduction paths shorting the network conduction [50, 84]. The importance of optimizing the device by mitigating metallic shorts in order to improve in particular the on-off ratio is a prevalent view throughout the research on CNT networks [27–30, 32, 50, 69, 72, 79, 84]. This model is sufficient for devices with low channel widths comparable to the length of the CNTs used, where even for low metallic CNT concentrations there is a significant probability of metallic shorts, or for devices where the networks are so dense that the metallic CNTs are percolating. However, for systems where this is not the case, it is no longer reasonable to assume that shorts across the network are the principal cause of change in on-off ratios as alluded to by Rouhi, Jain, and Burke [5]. In Chapters 4 and 5 of this thesis, I use the model of junction dominated conduction in networks where the metallic content is below percolation to explain trends in on-off ratios.

2.4 The importance of CNT junctions in network CNT devices

The work by Lee et al. [15] and Fuhrer et al. [68] clearly indicate the importance of the junctions between CNTs as being the dominant feature in conduction through CNT systems. The Schottky barriers formed when a semiconducting CNT is in contact with a metal, whether a metallic CNT or a fabricated electrode, are vital to the understanding of conduction in CNT-CNT systems. CNT Schottky junctions have been the subject of extensive research due to their primary importance to the transistor characteristics of CNT based FET devices [13–15, 31, 54, 59, 67, 68, 71, 114, 124, 125].

With the commercial availability of CNT materials with up to 99.9% semiconducting CNTs (NanoIntegris), the importance of metallic tubes as shorts across networks of CNTs

has become something that can be mitigated when fabricating CNT FET based devices [48]. Recent work by Lee et al. [51] using solution fabrication of purified CNTs has led to devices with a 90% yield, on-off ratios of 4.25 ± 0.13 orders of magnitude, and mobilities of $(6.7 \pm 2.5) \text{ cm}^2/\text{Vs}$ across 23 devices. They attribute these metrics to the removal of metallic shorts through the network [51].

Purified CNTs do allow the removal of metallic shorts across network device regions, but they do not remove metallic CNTs entirely. Where >99% purified CNTs are used, the low proportions of metallic CNTs makes metallic shorts unlikely compared with unpurified networks of the same density. In CNT networks with a low density of metallic CNTs, the focus should be on the impact of these metallic CNTs as junction forming elements rather than for the impact of metallic shorts [13–15, 31]. Instead of continuing to focus on the removal of metallic paths in the CNT network, as is still prevalent in the literature despite using purified CNTs, this work focuses on their impact on conduction when they do not short the network.

Spatially mapped conducting probe measurements in the literature on networks of CNTs have shown conduction to be dominated by certain junctions which have been attributed to the conduction barriers formed at m-s junctions in the network [14, 31, 77, 80, 97, 124, 126]. An example of conductive AFM (cAFM) measurement is shown in Figure 2.4 (a) showing the relative conductivities of a section of a CNT network [14]. Stadermann et al. [14] use cAFM where the conductance is measured between the AFM tip and the network to plot the conductance as a function of distance along the conduction path as shown in Figure 2.4 (b). Significant conduction drops are seen only at the junctions between CNTs, labelled as A and B. These conduction changes only at some junctions are attributed to Schottky barriers, which only form at m-s junctions [14, 31, 124, 126].

Research on Schottky barriers, first by Fuhrer et al. [13] and then by others, at crossed nanotube junctions has shown that the m-s junctions that they measured were shown not only to have a higher resistance and so dominate conduction but to be the only significantly gate-dependent junctions between CNTs [13, 15, 68, 114]. Work by Hicks, Behnam, and Ural [27], Behnam and Ural [29], and Hecht, Hu, and Grüner [127] modelling the variation of conduction with CNT network density has shown that $R_{tube} \ll R_{junctions}$ for models of one-dimensional conductors when compared with conduction

Figure 2.4: An example of cAFM performed on-conducting networks of CNTs is reproduced here from Stadermann et al. [14]. Conductance is measured from the tip to an electrode contacted to the network (not pictured). A map of conductance is shown in (a) and is plotted as a function of distance along a connected CNT path is shown in (b). Significant conductance jumps are labelled in (b) and shown in (a) as A and B.

through mixed bundles and single CNTs.

There is an oversimplification of the language used to describe CNT network systems in the literature. In particular the use of "tube" to refer to the elements of a CNT network, when in fact AFM images of the network structure indicate that it is a mixed network of bundles and single CNTs. Stadermann et al. [14], Kalinin et al. [77], Kodama et al. [80], Nirmalraj et al. [124], and Garrett et al. [128] explicitly worked with networks of bundles, and experimentally observe the junctions between them to dominate conduction and gating. The primary work on crossed nanotubes investigating in detail the Schottky junctions that form all use crossed single nanotubes [13, 15, 68, 114, 116]. Rouhi, Jain, and Burke [5], Behnam and Ural [29], and LeMieux et al. [85] refer to "tubes", but images of their films indicate networks of CNTs that are 10 nm, 15 nm and 75 nm in height respectively indicating a quasi 2D film of bundles. Topinka et al. [31] uses "tubes" but provides no direct evidence for this. Regardless their simulation model applies as long as m-s junctions can form between bundles which Stadermann et al. [14] and Nirmalraj et al. [124] clearly show. Although there is vague language used in the literature regarding whether networks are comprised of single tubes or bundles, the literature results

compare well with each other.

It is the position of this work that the demonstrated junction dominance of conduction and gating through CNT networks is of great importance to understanding the conduction through CNT network systems. For network systems fabricated with purified CNTs, the impact of metallic CNTs will be primarily to introduce m-s junctions into the network. The impact of these Schottky junctions on the gating is of critical importance.

2.4.1 Schottky barriers, an explanation

Before considering the Schottky barrier found at the interface of a semiconducting CNT with a metallic CNT or a metal electrode it is first important to understand the basic physics behind a Schottky barrier formed at the interface between a general metal and a semiconductor [38, 129, 130]. The notation of Sze and Ng [38] will be followed in the following example.

Consider a metal of work function ϕ_m , and a p-type semiconductor with band gap E_G and electron affinity χ shown in Figure 2.5 (a). We use a p-type semiconductor in this example to be consistent with the CNTs used in this work which exhibit p-type semiconductivity [42]. When the metal and semiconductor are brought into contact, charge will flow between the two until the Fermi levels in both align. The result of this is a depletion region in the semiconductor at the interface with the metal similar to what would be seen in an abrupt and one-sided $p - n$ junction. The band diagram of the ideal case for contact is shown in Figure 2.5 (b), where the Schottky barrier to holes is denoted as ϕ_{SBp} . The height of the Schottky barrier for electrons at the junction is given by:

$$\Phi_{SBe} = q(\phi_m - \chi) \quad (2.3)$$

where ϕ_m is the work function of the metal, and χ is the electron affinity of the semiconductor. These are the energy required to remove an electron from the Fermi level and the conduction band to vacuum respectively. The corresponding barrier height for holes is given by:

$$\Phi_{SBp} = E_G - \Phi_{SBe} \quad (2.4)$$

Thus the barrier height for both carrier types is a function of the work function of the metal and the electron affinity of the semiconductor. However, in practice, the simple

Figure 2.5: Band diagram for electrons for (a) a metal and a p-type semiconductor and (b) for their band diagrams when in contact.

model for the barrier height given in Equation 2.4 is not sufficient to predict experimental measurements. The most common deviations from the ideal model being caused by a non-zero gap between the two materials and the presence of interface states in the semiconductor where states at the barrier act to create a dipole across the interface, lowering the effective barrier height [38, 125].

2.4.2 Conduction through a schottky barrier

Conduction through an energy barrier presented by a Schottky junction is typically described by tunnelling through the barrier or thermionic emission over the barrier [38]. The tunnelling current depends on the energy of the electrons and the width of the energy barrier, while the thermionic emission current depends on the height of the barrier. For CNT systems at room temperature thermionic emission dominates the current through the Schottky junctions formed between CNTs [13], and between CNTs and electrodes [89, 125].

Thermionic emission across an ideal Schottky barrier is only dependent on the barrier height and the energy of the electrons. Assuming:

1. The barrier height is high $\varphi_B \gg k_B T$
2. The doping concentration is lower than the density of states in the valence or conduction band

The ideal diode equation, as presented in Sze and Ng [38] and Svensson and Campbell

[125] can be used to describe the current dependence at a Schottky junction as:

$$I = AA^*T^2 \exp(-\varphi_B/V_T)[\exp(V/V_T) - 1] \quad (2.5)$$

where $V_T = k_B T/e$ is the thermal voltage, φ_B is the Schottky barrier height, A is the barrier area, and A^* is the effective Richardson constant. Note that here V is equivalent in notation to V_{DS} .

2.4.3 Schottky barriers in CNT systems

Schottky barriers affect the electrical characteristics of a CNT FET in two ways; the Schottky contacts that occur at each of the source and drain electrodes where they contact the semiconducting CNTs [54, 71, 89, 125], and between the metal and semiconducting CNTs within the network [14, 15, 31, 68, 124]. Noshio et al. [89] have shown that the work function of the metal contacts affected whether the CNT FET showed p-type, n-type, or ambipolar conduction. Their work correlated both the direction of switching, which was affected by the dominant carrier type, and the magnitude of the on-current, which depended on the barrier height Φ_{SB} . They also showed an increase in on-current with metal work function for p-type devices consistent with Equation 2.4, and a decrease for n-type devices consistent with Equation 2.3. The barrier height in both cases determined the transmission coefficient of carriers tunnelling through the Schottky barrier [89]. Although the Schottky barriers at the electrode are important for CNT FETs in general, both the experimental work and simulations that I performed in this work were designed so that the electrode barriers were of minimal impact to the gating in order to focus on the CNT-CNT Schottky junctions within the network.

CNT-CNT Schottky barriers

Schottky type contacts have also been shown to form at the contact between metal and semiconducting CNTs [68, 114]. These junctions have been further shown to dominate the conduction and gating in network CNT FET devices [14, 15, 31, 77, 124]. Fuhrer et al. [68] demonstrated that for a single m-s CNT junction there was a Schottky barrier of 190 meV to 290 meV [68]. They used 1 nm to 1.5 nm diameter CNTs which have a bandgap

between ~ 0.5 eV to 0.7 eV [33], which shows good agreement with $E_{\text{Barrier}} = E_G/2 \sim 250$ meV to 350 meV. Conduction within networks of CNTs is dominated by the conduction through junctions as determined by research in the literature where conductive AFM measurements are taken along portions of networks of mixed bundle and tubes [11, 14, 124, 126].

Stadermann et al. [14] took cAFM images, similar to those shown in Figure 2.4, of a CNT network before and after an applied gate bias to the network. They showed that the high resistance junctions restricted conduction to certain regions of the network. The regions of the network showing conduction were separated from the non-conducting regions by m-s junctions. They attribute the conduction difference between these regions to the increased Schottky barrier size at high gate voltages.

Topinka et al. [31] showed that varying percentages of semiconducting CNTs would alter the conduction "phase" in a conducting CNT network by making the simplifying assumption that m-s junctions would completely block conduction while other junctions and CNTs would conduct equally. The "phase" of conduction that they calculated from simulations of the conduction through the CNT network is illustrated in Figure 2.6. The "phase" is shown with respect to the semiconducting percentage and CNT network density. They showed the overall conduction to be at a maximum both for 0% semiconducting and 100% semiconducting, corresponding to the pure metallic and unblocked semiconducting networks in Figure 2.6, which is consistent with there being no Schottky junctions present in the network. At 80% semiconducting CNTs they found a minimum of conduction as all conduction paths included highly resistive Schottky junctions. They further expanded this idea to a phase diagram that indicates the nature of the conduction within the network.

Topinka et al. [31] stated that those networks that were defined as blocked semiconducting networks in Figure 2.6 offer the most potential for gating in a real CNT network FET due to the Schottky junctions dominating conduction. When the assumption of completely blocking m-s junctions is relaxed to include some gate-dependence, those junctions will most closely resemble the blocking case when off-gated.

The work in this thesis takes the position that the Schottky barriers at those m-s junctions would not wholly block conduction as assumed in the Topinka et al. [31] model, but

Figure 2.6: Plot showing the network “phase” as a function of tube density normalised to the percolation threshold and the percentage of semiconducting CNTs. Grey (sub-percolation) denotes an unconnected network, and light grey (metallic network) a network shorted by metallic CNTs. Light blue (blocked semiconducting network) and green (binary network) are networks where Schottky barriers block conduction, while dark blue (unblocked semiconducting network) has conduction that consists of unblocked semiconducting paths. Topinka et al. [31] denote the region in red as being suited to fabricating CNT network FETs (CNTN-FETs) with high on-off ratios. Reproduced from Topinka et al. [31]

would instead significantly impact the gate-dependence. The extension of the Topinka et al. [31] model to include explicit gate-dependence in the m-s junctions in the network is explored in Chapter 5, and furthermore investigates a model of topology enabled junction dominated gating in those networks.

2.5 Motivation for continued study into CNT network conduction

Work by Fuhrer et al. [68] and Tombler et al. [114] in 2000 clearly showed the importance of Schottky junctions formed at the junction between metallic and semiconducting CNTs. The removal of metallic CNT paths that short circuit conduction to achieve high on-off ratios has persisted in the literature despite the widespread use of purified CNTs with high percentage semiconducting CNTs in recent years [32, 48, 55, 84, 87, 119, 120]. Rouhi, Jain, and Burke [5] in 2011 stressed the need to better understand the variation in on-off ratios when the CNT network density is below the metallic percolation threshold. The use of percolation theory to investigate the metallic and semiconducting paths within the network is introduced, and an overview of its application in research on CNT network systems are given. The work in this thesis considers the junctions between CNTs as the dominant feature in conduction when the network density is low enough that no complete metallic paths exist.

Research has been done on the impact of the Schottky barriers at m-s junctions within the network on the overall device performance [15, 31]. There is substantial experimental and theoretical evidence for junction dominated gating in CNT network systems [13, 15, 31, 68, 131]. In particular, the literature using localised imaging techniques has shown that the junctions within the network dominate the conduction through the network [14, 31, 124, 126].

The predominant motivating factor for the work in this thesis is to understand the effects of CNT network conduction with varying network density that we have seen in previous work on CNT aptasensors. We showed that the sensitivity of CNT based aptasensors is improved by lowering the CNT network density, where all devices fabricated had metallic densities below the percolation threshold [11, 110]. The improvement is linked to increased sensitivity to local aptasensor gating is due to high sensitivity sections within the CNT network. The following chapters describe how we fabricated CNT network FET devices. We characterised their physical network properties and their electrical switching when locally and globally gated. We then compare those results to a simulated model with m-s junctions as the dominant gating element.

Chapter 3

Fabrication of locally top-gated CNT FET device platforms

Carbon nanotube field effect transistors (CNT FETs) were fabricated so that the whole network could be gated as well as localised regions. A back-gate was used for global gating, and top-gates were fabricated at select areas across the CNT network area to achieve local gating. Five distinct fabrication layers were necessary to produce these devices, each requiring process optimisation and modification to suit multiple stacked and sequential fabrication steps. The recipes and experimental procedures used to fabricate and measure the CNT FET platforms are detailed in this chapter.

3.1 CNT FET device structure

A schematic of the CNT FET structure used in this work is shown in Figure 3.1 (a). Degenerately doped Si wafers with a 300 nm top layer of thermal SiO₂ were used as substrates. The thermal SiO₂ was grown by the wafer manufacturer at 800 K to 1200 K using high purity water to produce a layer of SiO₂ on top of the silicon. The wafers were pre-prepared in-house with a layer of gold on the back side to facilitate electrical contact to the Si back gate. The conducting region of the CNT film is 60 μm $\times$ 60 μm as shown in Figure 3.1 (b). This region was defined by removing the CNTs deposited on the device surface except in a 60 μm $\times$ 80 μm region. The source and drain electrodes were fabricated with a 10 μm

Figure 3.1: Device schematic for back and top-gated CNT FET device. Cross section (a) showing device stack and electrical connections. Top down (b) shows the lateral positioning of top gates relative to the 60 μm × 60 μm conducting CNT region and source and drain electrodes. The top dielectric and substrate are omitted from (b) for visual clarity

overlap on each end of the CNT region providing electrical contact and restricting the conducting area to 60 μm × 60 μm. 10 μm wide top gate electrodes were positioned 8 μm laterally from the source and drain electrodes. The central pair of local top gates were positioned in the center of the device region laterally, and 7 μm from the outside top gates. They extend 20 μm across the device region from each side, leaving a 20 μm gap in the middle.

The layout of the top gates was selected to allow gating of only a localised region of the network independent of any effect on the network from the source and drain electrodes. Specifically, Schottky barriers that form between the electrodes and the CNTs will not be affected by these top gates, ensuring that any gate-dependence measured must originate within the CNT network. The top gates that span the width of the con-

ducting channel are referred to as the total top gates as they will affect a section of all the conduction paths across the network. The central top gates, which span only one-third of the network width are referred to as the partial top gates and were designed to probe the effect of gating regions of the network that do not encompass the full possible conduction paths. Some redundancy in measurement options was incorporated, hence two of each type of gate.

The fabrication of these devices was carried out as follows:

1. The substrate wafer was prepared by deposition of ~ 50 nm of gold on the back Si
2. Alignment markers were prefabricated in gold to allow registering of all following fabrication steps to within ± 1 μm
3. A CNT layer was deposited and then etched to remove all of the CNTs not in the active region of the device. CNT deposition and processing, as well as investigation of density variation, is detailed in Section 3.3
4. Source and drain electrodes were then patterned using an in-house photolithographic process detailed in Section 3.2.2 to remove all edge spikes in the electrodes that could disrupt subsequent layers. A detailed recipe can be found in Appendix A.2
5. A layer of SU8 polymer dielectric was patterned to allow electrical contact to the source and drain electrodes while providing a robust dielectric for the top electrodes. The SU8 dielectric is described in Section 3.2.1 and the recipe details are in Appendix A.4
6. Top gate electrodes were fabricated as shown in Figure 3.1 (b) to allow for localised gating of the CNT film

3.1.1 Standard positive photolithography

Photolithography is a standard microfabrication technique that uses a specially designed photosensitive resin (photoresist or resist), which when exposed to ultraviolet

(UV) light changes its chemical and mechanical properties. By exposing a thin layer of resist to UV through a patterned mask, those regions of the film can be developed to expose only the desired regions of the substrate for further additive or subtractive fabrication processes. The masks were designed in house using Layout Editor and were patterned via a UV laser writer. AZ1518 positive photoresist (MicroChemicals) [132] has been used for the majority of the photolithography here.

A thin film of liquid photoresist was deposited onto the substrate to be patterned via spin coater. The process of spin coating uses centripetal force and liquid tension to spread the resist in an even thin layer across the surface. The thickness of the photoresist layer is determined by the spin speed and the photoresist viscosity. In this work, a spin speed of 4000 rpm was used to achieve a thickness of 1.8 μm using un-diluted AZ1518. The resist layer was then exposed to UV light via a chrome-on-glass photomask, which produces the pattern required. All photolithographic alignment and exposure was performed on a Karl Suss MJB3 mask aligner using a USHIO SHP 350W mercury vapor lamp to produce the UV light. The mask was aligned with the chip to be patterned and exposed to UV for 10 s as shown in Figure 3.2 (a). The photopolymer molecules in the region of the resist exposed to UV light are shortened via chain scission so that they become more soluble in a polar developer solution. AZ351B (MicroChemicals) [133] metal ion containing developer was used in this work diluted 1:4 developer to de-ionised water. Light agitation of the chip in developer for 20 s was used to wash away those portions of the photoresist that have been exposed as shown in Figure 3.2 (b). The resist process is imperfect and is well known not to produce perfectly vertical sidewalls in the developed regions. In general, the sloped sidewall is expected and does not interfere with the desired pattern. Adverse effects of the edge angle are discussed in detail in Section 3.2.2.

At this point, the desired pattern exists in the photoresist, with the desired area of the substrate exposed. When fabricating an electrode pattern, 5 nm of Cr followed by 50 nm of Au is deposited on top of the patterned photoresist using a thermal evaporator (Angstrom Engineering, Nex Dep 200). The thermal evaporator operates by passing high current through a tungsten holder containing the target metal. By heating the metal to its evaporation point in a vacuum chamber at $\sim 10^{-6}$ Torr, the metal was evaporated and traveled from the target to the substrate adhering there. In this way, metal features of

Figure 3.2: Key steps in the standard AZ1518 positive photolithographic process. Exposure of the deposited photoresist to UV light through a patterned mask (a). (b) the pattern etched into the photoresist following a development step removing the exposed resist. (c) Au metal deposited via thermal evaporation. (d) the patterned metal which remained after the photoresist was removed in a lift-off step. Images not to scale.

precise thickness were deposited.

The chrome was used to provide adhesion to the SiO₂ surfaces used throughout this work, to allow the deposition of gold with good mechanical adhesion. As it is on the bottom, its impact on the conduction through the electrodes is minimal. After metal deposition, a layer of metal exists across the entire substrate, both the photoresist and the patterned gaps, as shown in Figure 3.2 (c). A lift-off step consisting of a 10 min soak in acetone followed by 10 s of sonication in acetone was used to dissolve the remaining photoresist on the surface and any metal deposited on top of it, leaving only the metal in the desired regions shown in Figure 3.2 (d) defined by the mask pattern. A final cleaning step in >99.5% purity isopropanol followed by drying in forced N₂ gas was used to remove

any remaining chemical or metallic contaminants from the surface of the device.

3.2 Top gate dielectric selection and fabrication

The back gate in this work was achieved by using the entire degenerately doped Si substrate as a global back gate electrode and the native 300 nm SiO₂ as a back gate dielectric. In order to fabricate patterned top gates on the device as shown in Figure 3.1 (a), a deposited dielectric layer was needed. The requirements for such a layer were that it be electrically insulating to prevent any leakage current from affecting the device behaviour and that the dielectric constant was comparable to the dielectric constant of 3.9 for SiO₂ [38] used as the back gate dielectric.

For this work, I aimed to match the top and back gate effect on the conducting channel in order to directly compare the transfer measurements. The gate of a CNT FET acts capacitively on the conducting channel [38, 42]. The equation for the charge density for a capacitor is:

$$\sigma = \varepsilon \frac{V}{d} \quad (3.1)$$

where σ is the charge density at the surface of the dielectric, ε is the dielectric constant of the material, V is the applied voltage across the dielectric and d is the dielectric thickness. The thickness and dielectric constant of both the top and bottom dielectrics must be selected to match the charge density for a given gate voltage.

We investigated top gate dielectric materials that had comparable dielectric constants to the SiO₂ back dielectric. Once a material was selected, the thickness of the layer was tuned to achieve equivalent charge density in the conducting channel using Equation 3.1. SiO₂, Al₂O₃, AlN, and polymer SU8 were initially preselected for investigation as to which would be the most suitable dielectric materials, due to their ability to be fabricated in-house and their dielectric constants of 4, 8.5, 9.1 and 3.9 [38, 134, 135] respectively. SU8 was chosen for use in the final devices fabricated, due to being robust to the subsequent photolithography necessary for top gate electrode fabrication and its simple fabrication process.

The investigation of SiO₂, Al₂O₃, and AlN is outlined here. SiO₂ was fabricated via sputter coater deposition (HHV Auto500 with Advanced Energy Cesar 136 600W RF gen-

erator) from a SiO_2 target in Argon. To produce stoichiometric SiO_2 O_2 gas would have to be introduced during the deposition process. SiO_2 was not developed further due to the significant growth parameter optimisation that would be required. Al_2O_3 was likewise sputter coated, and AlN was deposited using an Al effusion cell and Kaufmann ion source for nitrogen in a Thermionic UHV system. Both of the aluminium containing dielectric films produced suitable insulating films in initial tests. Kapton tape was used to mask the top and bottom electrodes to facilitate rapid testing. However, when they were fabricated as part of a full device stack in a 300 nm layer, as shown in Figure 3.1 (a) electrical shorts across the layer were observed. The cause of this was significant etching, on the order of 5 nm/s to 10 nm/s, of the aluminium layers due to the chemical developer used to photolithographically define local top gate electrodes as the final device layer on top of the dielectric. The basic (PH ~ 13) developer chemicals are known for attacking alkali-sensitive metals such as aluminium and copper, effectively acting as etchants [133]. The failing of Al_2O_3 and AlN was attributed to this. The etching away of the dielectric layer meant that both of the aluminium containing dielectrics were unsuitable for use as the top gate dielectric layer in the device stack used, despite good film qualities and high dielectric constants. Low aluminium attack developers exist [133] but were not available during this work.

Due to its suitable dielectric constant of 3.9, polymer SU8 was selected as the top gate dielectric as the most robust and readily fabricated dielectric material tested. In order to match the charge contribution to the conducting channel, I developed a fabrication process capable of producing good quality films with a thickness of 300 nm as described below.

3.2.1 SU8 as a sub 200 nm organic dielectric layer

SU8 is a polymer photoresist that is optically transparent and can be easily fabricated into layers of 0.5 μm to 200 μm thickness with high aspect ratios [135, 136]. It is also resistant to chemical solvents, acids and bases, especially after a hard bake step to fully crosslink the polymer [136]. Its chemical resistance coupled with its dielectric constant of 3.9 [135] makes it a suitable choice for a polymer dielectric layer that would be robust

enough to allow a further photolithographic step to be performed on top of it to fabricate gate electrodes. However, in order to get electric fields at the CNT layer comparable to the fields generated by back-gating the devices through 300 nm of SiO_2 , which has a dielectric constant of 3.9 [38], a 300 nm thick SU8 layer would be required from Equation 3.1. The lowest concentration by weight of liquid SU8 available is the SU8 2000.5 from MicroChemicals [136], which has a concentration by weight of solids of 14.3% and at the maximum spin speed given in the datasheet of 4000 rpm produces a thickness of 500 nm. To produce sub 500 nm films here, solid GMPI 1060 SU8 was dissolved in cyclopentanone at concentrations of 10% and 15% by weight.

Figure 3.3: Spin curves for SU8 photoresist designed with 10% (blue) and 15% (red) solid SU8(GMPI 1060) in cyclopentanone. Spin curves were measured on 4 mm × 7 mm substrates with an acceleration of 10 000 rpm/s from 1000 rpm to 6000 rpm. Interference patterns at the edge of the transparent film (inset) were due to edge beading up to thicknesses of 1.5 μm at the far edge.

The spin curves for the 10% and 15% by weight preparations of SU8 in cyclopentanone are shown in Figure 3.3 in red and blue respectively. The thinnest layer of SU8 fabricated was (180 ± 10) nm and showed robust electrical insulation and good physical uniformity. The full fabrication recipe used in this work is shown in Appendix A.4. The variation in film thickness was measured by taking three measurements across the center $4 \text{ mm} \times 2 \text{ mm}$ region of 3 different $7 \text{ mm} \times 4 \text{ mm}$ chip using a Dektak profilometer. The uncertainty in thickness in Figure 3.3 is the standard deviation of these measurements.

The corner regions of the 10% SU8 solution spun on to $7 \text{ mm} \times 4 \text{ mm}$ chips showed edge beading effects. In this work, I was concerned with the thickness uniformity and electrical insulation in the center of the chip where the active CNT region of the device sits. When the photoresist is spun on to a chip, some pools up at the corners and edges resulting in a bead of photoresist which remains on the edge of the chip. The edge beading in Figure 3.3 (inset) had minimal impact on this work, beyond slightly increasing the distance that could be achieved between mask and chip in the subsequent photolithographic patterning of the top gate electrodes. If the uniformity of SU8 layer thickness was critical across the entire chip region, existing techniques for edge de-beading could have been implemented [133, 136]. The extent of the edge beading was never observed to be more than 1 mm laterally from the edge of the chip and thus did not impact the active device region.

3.2.2 T-profile resist recipe for electrode edge spike reduction

Initial tests of fabricating a top dielectric layer were met with failure, where all of the layers fabricated were electrically leaky, allowing currents over 1 mA to flow through them. Leaking SU8 dielectric layers were measured when the test devices used electrodes fabricated with photolithography. However, when the leakage currents were tested with electrodes that were fabricated without the use of photolithography, i.e. by simply masking off regions of the device using Kapton tape, the SU8 layer was insulating (current $< 1 \text{ nA}$). The lack of leakage through the SU8 when changing the electrode fabrication used to measure it suggested an issue with the electrodes which was causing leakage through

the SU8 dielectric layer.

AFM imaging of the bottom electrodes fabricated using the standard positive photoresist process shown in Figure 3.2 highlighted the issue. The edges of the electrodes which are shown in Figure 3.4 (a) had vertical spikes along their entire edge. Cross section of the AFM image shown in Figure 3.4 (a) (inset) showed that these spikes varied in height from 40 nm to 150 nm, and were restricted entirely to the electrode edge. The edge spikes were not large enough to fully puncture the 300 nm SU8 dielectric layers used. However, spikes on the electrode beneath the dielectric layer would provide regions with greatly enhanced electric fields at the spikes under the voltage difference between the source and drain electrodes and the top gates that is necessary for FET operation. Electric field enhancement could cause dielectric breakdown consistent with the conduction through the SU8 measured.

The source of the electrode edge spikes was determined to be due to the positive resist used in the fabrication of the electrodes and was mitigated by selecting and optimising a different photolithographic process to achieve an undercut profile. The 30° positive slope profile in the positive resist [132] was determined to be the cause of the electrode edge spikes. When metal was deposited vertically onto the patterned resist, some metal was deposited on the sloped sidewalls of the resist as shown in Figure 3.2 (c). The metal that was incidentally deposited on the sloped sidewalls of the photoresist was not disconnecting from the metal deposited in the bottom during lift-off, resulting in the large spikes seen in Figure 3.4 (a). In order to remove these spikes that were disrupting the fabrication of an electrically insulating dielectric layer, an undercut photoresist profile was needed. A photoresist process was developed similar to a bilayer fabrication process to achieve an overhang or undercut in the profile [137]. The efficacy of this process in removing the edge spikes on deposited electrodes can be seen in Figure 3.4 (b), where the edges were shown to be free of spikes.

The resist recipe that was developed was a T-profile recipe based on the image reversal (IR) photoresist AZ5214E (MicroChemicals) [138]. IR resists were designed to be operated as a positive or negative resist. The photopolymer will undergo breaking under exposure to UV light as with the AZ1518 positive photoresist. Thus an IR resist can be used as a positive photoresist without further modification. However, the photopoly-

Figure 3.4: AFM images of Au electrodes on SiO₂. The electrode edge in (a) was fabricated using the standard AZ1518 positive photoresist recipe, while (b) was fabricated using the optimised T-profile recipe developed for AZ5214E. Cross sections across the electrode edge (inset) show 100 nm edge spikes in (a) and 0 nm and 5 nm edge spikes in (b).

mer in an IR resist can also be baked after exposure to UV, which crosslinks the organic polymers to make them resistant to development [133].

The crosslinking of UV exposed regions possible with IR resists has been leveraged to produce and optimise a multistep resist process that removes the effect of the angled sidewalls in the positive photoresist recipe by producing an overhang in the resist sidewall, hence its description as a T-profile resist recipe. The IR resist was spin coated onto the substrate at 4000 rpm for 60 s. Before exposure of the resist to the mask, the entire layer of photoresist was flash exposed for 0.15 s to achieve $\sim 1/100$ th of the dose normally required to expose the resist. Such a short flash exposure has the effect of disrupting the photopolymers only in a thin layer at the top of the photoresist, as shown in Figure 3.5 (a). The photopolymers are disrupted via absorption of UV light. Due to attenuation of the UV within the photopolymer, the time of exposure required to fully disrupt the polymer increases with the depth of the polymer [138]. Hence a short exposure only delivers sufficient dose to a layer at the top of the photoresist to fully disrupt it.

The substrate was then subjected to a crosslinking bake step at 110 °C for precisely

Figure 3.5: Key steps in the T-profile AZ5214E photolithographic process. (a) flash exposure of the entire surface followed by a bake step crosslinks a thin layer on the surface. (b) full exposure of the deposited photoresist to UV light through a patterned mask. (c) the pattern etched into the photoresist following a development step showing the overhang caused by the top crosslinked layer. (d) Au metal deposited via thermal evaporation cannot land on the sidewalls due to overhang. (e) the patterned metal remaining after the photoresist was removed in a lift-off step shows no edge spikes.

2 min to crosslink this very thin layer of exposed photopolymer and thus make it chemically more robust. Following the crosslink, Figure 3.5 (b) shows the resist exposed to UV through a mask using a normal 10 s dose required to expose the full photoresist layer. The substrate was then developed for 30 s while agitating lightly. The exact exposure, bake, and development parameters are detailed in Appendix A.2 in such a way as to be fully reproducible.

The thin layer was more resistant to development and so was etched at a slower rate producing an overhang as shown in Figure 3.5 (c). The extent of crosslinking determines how much the top layer develops and whether it can be developed at all. Thus the flash

exposure dose and the crosslink baking time and temperature were carefully optimised to achieve an overhanging edge on an uncompromised pattern. The fabrication parameters were investigated using a grid search where successive test fabrication runs were fabricated with varying permutations of parameters.

The flash exposure was tested between 0.15 s and 1 s, the post-flash crosslinking bake was tested between 100 °C and 120 °C and for bake times of 1 min and 3 min. Success was determined when AFM images showed no evidence of any metallic edge spikes, as shown in Figure 3.5 (d). When the metal for the electrodes was deposited vertically, the overhang in the resist edges prevented it from being deposited on the sidewalls of the resist channel. The resist was removed in the lift-off step via a 5 min soak in acetone followed by a 10 s sonication in acetone. The resulting metal feature had no remnants of the metal from the sidewalls which had previously produced the edge spikes that were an issue with the positive resist recipe. The edge spikes were observed to be removed as shown in Figure 3.4 (b), and the SU8 was successfully fabricated as an insulating dielectric layer with the electrodes below it fabricated using the developed T-profile resist recipe.

3.3 Fabrication of random network CNT films via solution deposition

CNT networks were fabricated with varying CNT density on the substrate via a solution deposition process to facilitate the formation of a uniform random network [91, 101, 102]. Degenerately doped Si substrates with a 300 nm layer of SiO₂ were cut into 4 mm × 7 mm chips and cleaned with standard acetone and IPA rinsing before drying with N₂. Sheets of prefabricated CNTs (Buckypaper) containing 99% semiconducting CNTs (Nanointegris, IsoNanotubes-S) were weighed with a precision balance (Sartorius ME36S) and dispersed into dichlorobenzene (DCB) (99% Sigma Aldrich) via ultrasonication for 15 min to produce a dispersed suspension with a CNT concentration of 5 µg/ml. the CNT suspension was achieved in the absence of surfactants that are often required to achieve a dispersed solution. The effect of this was that the deposited CNT film was

free of any surfactant contamination, which is vital for use in sensor platforms where the surface area of the CNTs is of primary interest [11, 102, 103, 110, 139].

Polymethylsiloxane (PDMS) stamping was used to transfer a monolayer of 2-thiolpyridine on to the chip surface to facilitate CNT adhesion to the SiO₂. A blank cured PDMS surface was exposed to a 50 W O₂ plasma for 1 min, prior to spincoating a 10 mg/ml solution of 2-thiolpyridine (or 2-mercaptopyridine) in ethanol for 40 s at 2000 rpm. The 2-thiolpyridine coated PDMS was then brought into contact with the clean SiO₂ surface of the chips for 3 min before rinsing the chips in ethanol (< 3 s) to remove any excess 2-thiolpyridine followed by a N₂ blow dry. This short rinse step was found to be necessary due to some excess 2-thiolpyridine greater than a monolayer causing inhomogeneity in the resulting CNT films. After the short ethanol rinse the chips were submerged in the prepared CNT-DCB suspension for a fixed amount of time from 1 min to 80 min in order to vary the number of deposited CNTs [101]. After CNT deposition the chips were submerged in ethanol for 10 min and then blow dried with N₂ to remove any residual 2-thiolpyridine.

After CNT film deposition on the SiO₂ substrate the CNT channel region of the device was defined using photolithography followed by a 200 W O₂ plasma for 3 min (Oxford Instruments, Plasmalab 80 Plus) to remove any CNTs not protected by photoresist leaving behind only those CNTs in the desired channel region. The effect of photoresist lift-off in acetone using a short sonication of <10 s had a negligible effect on the CNT films. The effect of sonication in acetone on the films is investigated in detail in Section 4.2.1. The CNTs in each of the device channels were imaged using atomic force microscopy (tapping mode, Nanosurf, NaioAFM) prior to the deposition of the SU8 dielectric layer to characterise the morphology and topology of the film. All AFM image processing was performed using the open source software Gwyddion. The AFM image of a CNT film in Figure 3.6 shows a mixed network of single CNTs and bundles of CNTs. This is typical of the solution deposition process that was used, and consistent throughout this and past works [11, 101, 103]. The bundles are formed by Van Der Waals attraction between CNTs causing them to lie alongside one another. The diameter of single CNTs used is (1.5 ± 0.2) nm (NanoIntegris). Thus any structure with a height $\gtrsim 1.5$ nm can be designated as a bundle. The nature of the bundles, both physically and electronically, is

Figure 3.6: AFM image of solution deposited CNT film typical of this work. The network shows a mixture of single CNTs, with a height in the AFM image of ~ 1.5 nm, while bundles have a height $\gtrsim 1.5$ nm.

examined in detail in Section 4.3.1.

3.4 Electrical characterisation of CNT FET devices

Electrical measurements were performed with an Agilent 4156C parameter analyser on a Rucker and Kolls probe station with micromanipulators used to contact the device electrodes. The electrical connection of all electrodes for measurement was shown in Figure 3.1. All CNT FET transfer characteristics were measured at $V_{DS} = 100$ mV while V_G was swept from 20 V to 20 V and then back down again. Device output characteristics were measured with V_G stepped in 5 V increments from 20 V to 20 V while V_{DS} was swept from 5 V to 5 V. Each device has a back gate and 4 top gates, as shown in Figure 3.1, for a total of 5 gate arrangements per device, all of which were measured using the same procedure. When performing a top-gated measurement, the back gate was grounded to prevent spurious signals due to backplane capacitance.

The leakage current I_G from the gate terminal was recorded for each measurement

to verify that the device current I_{DS} was real. Devices which showed $I_G > 0.01 I_{DS}$ were discarded as "leaky". These devices typically showed an I_{DS} curve, which was the mirror of the I_G , consistent with current flowing through the gate dielectric. Leakage current was attributed to pinhole damage of the SiO_2 dielectric layer or CNTs which were not sufficiently removed in the plasma-etch step that bridges the dielectric at the edges of the chip. With careful fabrication, the device failure rate due to leakage was kept to below 10%.

3.5 Summary

We built on existing expertise in fabricating CNT FET device with random CNT films as the active material [11, 91, 103, 110, 139, 140]. We extended and adapted those methodologies to suit the multilayered device construction necessary for back and localised top gating of the CNT networks. Top dielectric layers were considered that had dielectric constants similar to the back SiO_2 dielectric were investigated. The photopolymer SU8 was selected for its closely matched dielectric constant of 4.4 [135], its ease of patterning and its resistance to chemical or physical damage during subsequent fabrication steps. A process was developed which allowed fabrication of robust SU8 polymer dielectric layers with thickness as low as (180 ± 10) nm. The electrode fabrication process previously used was re-engineered to remove vertical edge spikes as large as 140 nm that were damaging the insulating capabilities of the dielectric layer. These were removed by optimising a photolithographic process that produced an overhang in the patterned photoresist, removing the possibility of metal deposition on the sidewalls of the resist that were thought to be the cause of the electrode edge spikes. The optimised bottom electrode fabrication and SU8 fabrication process ensured that the SU8 could be used as the insulating dielectric layer as part of the full multilayer device stack.

A device platform that allowed global back gating and localised top gating of density varying random CNT networks was developed. Fabrication of the active CNT network film was achieved via 2-thiopyridine assisted solution deposition. The operation of CNT FET devices fabricated with these density varying films as locally gated devices is detailed in Chapter 4.

Chapter 4

Local top gating of random network CNT FET devices

4.1 Introduction

The motivating idea behind investigating locally gated randomly oriented carbon nanotube (CNT) network films was to produce a locally tunable conduction layer which could be integrated into a neuromorphic network system in order to modulate the conductivity through select regions of the combined network system. Neuromorphic atomic switch network systems have been applied to proof of concept computational models where they require a linear readout layer to allow signal generation and logic functionality [22, 141]. Being able to directly modify the conductivity of certain regions would allow direct control that could remove the need for the external linear readout layer.

In order to achieve local conductivity tunability in CNT network films, the response of the network to localised gating must be understood. CNT network field effect transistor (FET) devices with varying network densities were fabricated leveraging fabrication expertise from previous work [91, 103, 140]. Their electrical characteristics were investigated when gated via both a global back gate and patterned local top gates as described in Chapter 3.

Analysis of the physical characteristics of the CNT films produced was performed with a focus on both the morphology of the elements that comprised the networks and

how they made up the network topology. The network density of each CNT film was characterised by fitting a stick model to each individual CNT or CNT bundle in AFM images taken from the device channel for each network density. Films with network densities from 4 bundles/ μm^2 to 24 bundles/ μm^2 were produced by varying the submersion time during CNT deposition. Of primary interest in CNT networks is the proportion of the network that is comprised of metallic CNTs which have been shown to dominate the gating of the system [13, 14, 31, 54]. The concept of the proportion of metallic CNTs is extended to the system of mixed bundles of CNTs by determining the probability that a given bundle from the experimentally measured distribution of bundle sizes contains at least one metallic tube.

After characterising the physical morphology and topology of the networks, their performance in CNT FET devices was investigated by considering their transfer characteristics. CNT FET devices were gated via back gate, and two local top gates positioned across the width of the network area and across one-third of the network area called the total and partial top gate respectively. The on-off ratios for all three gate configurations were obtained from the transfer characteristics measured for all devices where conduction occurred. Back-gating was observed for all devices measured, and the on-off ratios were shown to increase gradually from 10 to 10^4 as network density decreased. Top gates also showed an increase in the on-off ratio at low network density, but instead of a gradual increase, they remained ≤ 10 for network densities above 15 bundles/ μm^2 , and a sharp increase to a maximum on-off ratio when top-gated of 10^3 at the lowest network densities measured.

The role of m-s junctions in the CNT network is discussed, with emphasis on how the network topology at low density causes these junctions to be more dominant. The need to continue the investigation of the impact of m-s junctions on the gating of CNT networks is highlighted. CNT networks see primary use in device applications as FET gated materials [5], and a better understanding of their network conduction will improve their use in particular for sensing and tunable conductivity sheets where the understanding of the spatial extent of their gate-dependence is vital.

4.2 Solution deposited CNT networks

In order to investigate the effects of the network topology on the gate-dependence of the CNT FET, a series of devices with varying densities was needed. CNT film post-processing was investigated to reduce density in a controlled manner to produce varying on-off ratios. Patterned etching of pre-deposited films and CNT removal via extended ultrasonication were investigated. Ultimately, density variation by varying the deposition time of the network as described in Section 3.3 was used to produce density variation, but the investigation of post-processing is described below.

4.2.1 Post processing of dense CNT networks

Post-processing of dense CNT films to provide a CNT film with a tuned density was investigated. Two methods were investigated: the etching of patterns into the CNT network to change its overall density [60, 62, 90], and mechanical removal using extended ultrasonication. Both processes were expected to reduce the overall network density.

Figure 4.1 shows the results of these tests. The effect of post-processing of the CNT films was characterised by their transfer characteristics before and after processing. Figure 4.1 (a) shows a level shift in the transfer characteristics of the CNT FET after patterned etching of the CNT film. The pattern was etched in a similar manner to the etching step used to restrict the CNT to the device channel. The desired pattern was left exposed while the regions of the CNT network that were to be protected were covered with photoresist. The film was etched in an O₂ plasma for 3 min. The pattern etched was a regular grid of 5 µm circles in a regular array with a pitch of 10 µm offset at 45 degrees to the direction of conduction as shown inset in Figure 4.1 (a). Sonication of a prefabricated dense CNT film was investigated as a mechanism to reduce the density of a fabricated CNT film. Figure 4.1 (b) shows the change in transfer characteristics for sonication times from 0 min to 10 min. AFM images of the CNT film before and after 10 min sonication are shown in Figure 4.1 (c) and (d) respectively.

Etching of a 10 µm pitch pattern into a dense CNT film as shown in Figure 4.1 (a) was shown to reduce the conductivity of the film but did not improve the transfer characteristics. Reduction of the conductance of the film is consistent with the work in Choi et al.

Figure 4.1: Post processing of solution deposited CNT films produces a significant change in conduction properties. A shift of current in transfer characteristics to lower values is shown in (a) after etching a grid of $5\ \mu\text{m}$ diameter circles in a $10\ \mu\text{m}$ pitch regular grid as shown inset schematically. (b) transfer characteristics of a device after increasing sonication in acetone from 1 min to 10 min shows improvement in transfer characteristics for the CNT film shown. AFM of the CNT network for the device before (c) and after (d) 10 min of sonication. Electrical measurements were performed using a back gate on a device with a channel length and width of $60\ \mu\text{m}$.

[60]. However, they observed increased on-off ratios with decreased conduction. They observed the greatest on-off ratios in films that were etched with $50\ \text{nm}$ diameter holes with a pitch of $142\ \text{nm}$ and decreasing on-off ratios as the pitch was increased. Without

being able to produce hole and pitch dimensions an order of magnitude smaller than is possible using optical photolithography, it would not be expected that their result would be reproduced. The micron-scale grids used in this work have shown to have some effect on the conduction most likely due to reducing the effective area of the conducting film, rather than affecting the network topology in such a way as to significantly alter how they respond to gating. This is consistent with work by Choi et al. [60] where they show that for large feature sizes etching is consistent with a change in density, where etching feature sizes $<$ the length of bundles causes disruption of the connectivity between bundles without significantly affecting the network density.

Extended ultrasonication was shown to have a significant effect on the transfer characteristics of a CNT FET device with an initially dense CNT network, as shown in Figure 4.1 (b). The on-off ratios were improved from <10 to >100 for this device. Across all devices showed a minimum change of 1 order of magnitude and a maximum change from an on-off ratio of 10 to 10^5 . This method for altering the CNT film transfer characteristics was not used throughout this work due to its lack of repeatability. In general, for films with initial on-currents of $10\text{ }\mu\text{A}$ prior to sonication, sonication times from 5 to 60 minutes would be required to reach the maximum change in on-off ratio and 5 minutes more than that time would cause the device to become non-conductive. This method was thus ineffective at producing a range of devices with varying on-off ratios.

AFM images taken before and after sonicating the device are shown in Figure 4.1 (c) and (d) respectively, where they show a drastic reduction in film uniformity after sonication. The network density was not observed to be changed in a uniform fashion. Large regions of the network, which are shown to be $1\text{ }\mu\text{m}$ to $3\text{ }\mu\text{m}$ wide, have all the CNTs and bundles removed while elsewhere the density appears relatively unaffected, as shown in Figure 4.1 (d). The cause of this inhomogeneity could be due to variation in the strength of adhesion to the SiO_2 surface, or localised variation in the strength of sonication experienced by the surface. Future work controlling precisely the strength of sonication, and the position of the chip could be used to investigate the exact cause.

Significant on-off ratio improvements were achieved, but the lack of repeatability in the sonication time required to achieve a specific result made the process impractical. Additionally, the maximum on-off ratio improvement shown was only realised after over-

shooting the sonication time, destroying the film entirely. The time required for a given improvement in electronic quality varied between 5 min and 30 min for samples with the same initial network density. These issues with repeatability as well as the degradation of the film uniformity that was observed made this process less suitable than the CNT density variation that could be achieved by varying the submersion time during deposition.

4.2.2 Varying CNT network deposition time

The CNT films with densities from (4 ± 2) bundles/ μm^2 to (24 ± 6) bundles/ μm^2 were fabricated using the solution deposition method shown in Chapter 3 by varying the deposition time from 1 min to 80 min. The films produced are shown to be a mixture of single CNTs and bundles of CNTs consistent with previous work [11, 103].

AFM images of CNT films with deposition times of 1 min, 5 min, 10 min and 20 min are shown in Figure 4.2 and show a clear increase in the film density with increasing deposition time. AFM images were taken from each device after the film was etched as described in Section 3.3, and before the SU8 dielectric was deposited. The AFM images were used to characterise the morphology of the bundles and CNTs present in each film, as well as the topology of the CNT network

4.3 CNT network morphology and topology

4.3.1 CNT bundle size and composition

CNT bundles are formed due to the Van der Waals attraction between CNTs. Bundles are taken to mean any bundle of one or more single CNTs. A bundle is comprised of CNTs which lie alongside one another. The lengths of a bundle can be much longer than the length of its constituent CNTs, as tubes can overlap along the bundle length. It is essential to understand the nature of the bundles that make up the CNT networks that were used in device fabrication, both for understanding of the experimental results shown here and subsequently to inform the model used for the CNT network simulation

Figure 4.2: AFM of CNT films with deposition times of 1 min, 5 min, 10 min and 20 min in (a), (b), (c), and (d) respectively. All images were taken on a $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$ square region. Scale bar is $2\text{ }\mu\text{m}$

in Chapter 5.

When considering CNT networks the prevalent stance in the literature is that metallic CNTs within the network are the limiting factor for high on-off ratios in CNT FET devices, because the metallic components provide ungated electrical shorts across the network. It has been shown here and in previous work [11, 103, 110] that the CNT networks fabricated via 2-thiopyridine stamped solution deposition as described in Chapter 3 are comprised of mixed single CNTs and bundles of CNTs. In order to relate this work to the existing literature on CNT networks, a simple framework for discussing bundles as

metallic or semiconducting has been developed.

Circle packing for CNT bundle composition

In order to accurately describe the conduction through the networks of bundled CNTs used here, a method of determining whether a given bundle is metallic or semiconducting. Firstly the diameter ϕ of a CNT bundle was measured using the height of a cross-sectional profile of each bundle obtained from AFM images of the network. An example of the measurements made are shown in Figure 4.3 (a) where the profiles of three example bundles were obtained by taking a perpendicular cross-section at the midpoint of each bundle in an AFM height scan as shown in Figure 4.3 (inset). Calculating the number of CNTs in a bundle with diameter ϕ has been achieved using circle packing, where solutions exist for the number of circles with diameter $d < \phi$ that can be packed into a larger bounding circle [142–144]. Solutions exist for packing up to 2000 circles, which is well in excess of what is necessary here [142].

An example of circle packing for three bundles is shown in Figure 4.3 (b) where the bundle diameters were measured to be $\phi_1 = 10$ nm, $\phi_2 = 5$ nm, and $\phi_3 = 2.5$ nm and yield packing numbers of $n_1 = 35$, $n_2 = 8$, and $n_3 = 1$ respectively. Diagrams of the solutions to the packing problem for those three example cases are shown in Figure 4.3 (b). A total of 84 bundle heights from two AFM images of CNT networks with deposition times of 1 min and 15 min respectively were measured. A histogram of the combined bundle diameters from both images is shown in Figure 4.3 (c) and shows a mix of single CNTs with diameters < 2 nm and bundles of CNTs with diameters up to 17 nm. The average CNT bundle diameter was calculated to be (5.8 ± 3.7) nm. There was no noticeable difference in the proportions of bundle sizes between the two images.

The CNTs used in fabrication have a manufacturer stated diameter of 1.2 nm to 1.7 nm (Nanointegris). The average value $d = 1.5$ nm was used for the circle packing solutions as the diameter of a single tube. The number of individual CNTs in each bundle was calculated using known circle packing solutions [142]. The histogram of the number of CNTs per bundle is shown in Figure 4.3 (d).

Figure 4.3: Example calculation of the number of CNTs per bundle is shown in (a) and (b). The diameter of three example bundles $\phi_1 = 10\text{ nm}$, $\phi_2 = 5\text{ nm}$, and $\phi_3 = 2.5\text{ nm}$ was determined from the peak height of AFM cross sections shown in (a) which have been offset for visual clarity. Cross sections were taken from the AFM image (inset) of the CNT film. The number of CNTs in each bundle was determined to be $n_1 = 35$, $n_2 = 8$, and $n_3 = 1$ via circle packing shown in (b) for the three example bundles. Histograms are shown of (c) the diameters of all bundles measured, and (d) the number of CNTs contained in all bundles measured calculated for each bundle using circle packing.

Metallic bundle assumption

We make the assumption that if a bundle of CNTs contains at least one metallic CNT that bundle will be metallic, and conversely that a bundle with no metallic CNTs will be semiconducting in nature. A metallic bundle defined as such will act as metallic for the purpose of conduction along its length, and the formation of junctions with other bundles [11, 95, 145]. We assume that bundles are formed of circular tubes of equal length that lie parallel to one another, and that the bundles themselves are circular.

There are limitations to this assumption which become more prominent at large bundle sizes. For bundles with >7 tubes, some tubes are enclosed within the bundle (e.g. $n_1 = 35$ and $n_2 = 8$ diagram in Figure 4.3 (b)). If these tubes were metallic, they would be prevented from making contact with adjacent bundles by the outer layer of tubes in the bundle. These internal tubes will cause some bundles which are assumed to be metallic to not form clear m-s junctions with adjacent bundles. On average some m-s would actually behave as s-s', and some much smaller proportion of m-m junctions would behave as m-s. The net effect would be that we overestimate the number of m-s junctions in the network. 51% of the bundles that we measured have more than seven tubes, with the measured proportion of larger bundles showing a tailed likelihood shown in Figure 4.3 (d). Our assumption thus provides an upper bound on the m-bundles and m-s junction in the network. We use the m-bundle percentage to assert that no metallic shorts exist in the CNT networks presented here. Thus our assertion that no metallic bundles exists holds true as there are likely even less metallic bundles than estimated.

In order to bring this estimate closer to the real number of metallic bundles, experimental studies of the nature of the bundles involved as well as geometric models taking into account the flexible nature of the tubes could be used. cAFM studies where the bundle diameters involved in each junction are correlated to their electrical properties could be used to provide data that would allow the probabilities of m-s junctions forming between large bundles to be used to extend this work [14, 124]. Additionally, experiments using single crossed bundles could be performed, similar to those performed by Fuhrer et al. [13] and Lee et al. [15] on single crossed tubes. Coupled with AFM of the bundles, this would likewise be able to correlate electrical characteristics with known bundle geometries. Extending the modeling of the CNT bundles using a flexible tube model could

take in to account the limits of the rigid cylindrical bundle, but poses serious issues for calculating the number of tubes per bundle, as solutions must be calculated numerically for non-circular and non-parallel geometries.

Metallic bundle percentage

An analogous metric to the percentage of single metallic CNTs in a network has been developed using the number of CNTs in a bundle n , the number of bundles measured containing n CNTs N_n , and the probability of a given single tube being metallic p_m . The manufacturer stated 1% of metallic CNTs in the CNTs used (Nanointegris) gives $p_m = 0.01$. The probability that a bundle of n CNTs contains at least one metallic tube is then:

$$p_{\text{metallic}}(n) = 1 - (1 - p_m)^n = 1 - 0.99^n \quad (4.1)$$

From this the probability that any given bundle in the systems measured contains at least one metallic tube can be stated as:

$$P_{\text{metallic}} = \frac{1}{\sum N_n} \sum_{n=1}^{n=\max} N_n p_{\text{metallic}}(n) \quad (4.2)$$

where N_n was taken from the experimentally measured distribution of the number of CNTs in each bundle as shown in Figure 4.3 (d). It should be noted that N_n can be zero if no bundles exist with that n .

Using the 1% concentration of single metallic CNTs used (Nanointegris), and the measured number of CNTs per bundle, the probability of a bundle being metallic has been calculated to be $P_{\text{metallic}} = 0.135$. The calculated proportion of bundles which will be metallic is equivalent to the metallic percentage used as a metric for networks of single CNTs. As such, this work will consider the percentage of metallic elements, mixed tubes and bundles, to be 13.5% for analysing the nature of the CNT networks.

The uncertainty in the metallic bundle percentage can be estimated in the simple case by taking an upper and lower estimate for the number of tubes present per bundle. Taking the circle packing solutions for $d = 1.3$ nm and $d = 1.7$ nm respectively and propogating those values through Equations 4.1 and 4.2, $P_{\text{metallic}} = 0.135 \pm 0.036$. This uncertainty calculation is limited by requiring the tubes in a bundle to be all of the same

length and requiring the bundle to be cylindrical. If these conditions were relaxed, the circle packing solutions becomes non-trivial and existing solutions could not be used [144]. Thus, while this uncertainty in the metallic percentage can be used as an indicator of confidence, the precise values should be considered with care.

4.3.2 CNT network density and percolation threshold

The CNT network morphologies were characterised by analysing the AFM images taken for each of the CNT films fabricated as described in Chapter 3. By varying the deposition time for producing the CNT films from 1 min to 80 min the average bundle density of the CNT network was varied from (4 ± 2) bundles/ μm^2 to (24 ± 6) bundles/ μm^2 as shown in Figure 4.4, consistent with other work [48, 102]. The variation in CNT bundle density across each AFM image was calculated by splitting each $5 \mu\text{m} \times 5 \mu\text{m}$ image into 25 $1 \mu\text{m} \times 1 \mu\text{m}$ sections (quadrats). The CNT bundle density in each quadrat was calculated by counting the number of bundles in each quadrat, determined using the bundle center to avoid overcounting for bundles that span multiple quadrats. The mean and standard deviation of bundle densities across quadrats for each sample is shown in Figure 4.4. Three AFM images were taken from random locations in each device channel. There was no significant visual difference between different $5 \mu\text{m} \times 5 \mu\text{m}$ regions in the $60 \mu\text{m} \times 60 \mu\text{m}$ device area. Because of the number of tubes which must be counted by hand for each image and the close similarity between images across the device channel, one image from each channel was deemed acceptable for determining uncertainty statistics. The changing uncertainty in density with deposition time is explored in detail in Section 4.3.3.

An example of an AFM image of a CNT film containing bundles of CNTs of varying sizes can be seen in Figure 4.5 (a), which was fabricated with a deposition time of 15 minutes and had an average density of 14 bundles/ μm^2 . The line segments manually fitted to each CNT bundle and the calculated intersections for that image can be seen in Figure 4.5 (b). The lines fit to each bundle have been used to calculate the density and the length of each bundle. There was no measured alignment between CNTs in the films investigated. The 25 quadrats used to calculate the variation in density across each CNT

Figure 4.4: CNT bundle density distributions calculated by splitting each AFM image into 25 $1\ \mu\text{m} \times 1\ \mu\text{m}$ quadrats and taking the density in each. The distribution of the densities across the quadrats is plotted for each CNT film fabricated with a given CNT deposition time, where the data point represents the mean bundle density across the image, and the error bars represent one standard deviation of the quadrat densities. Devices which were subsequently measured to be electrically non-conductive are shown in red, while electrically functioning devices are shown in blue.

film image are shown in the example given in Figure 4.5 (a) and (b). The quadrat analysis of density provides 25 density data points per film measured. These data points were used to calculate the mean and standard deviation of density for each film.

Figure 4.5: An example of (a) a 5 μm square image taken of a CNT network fabricated with a 15 min deposition time with a resulting average bundle density of 14 bundles/ μm^2 in the device channel. (b) Line segments that were manually fitted to the bundles (blue) and the calculated intersections of those lines (red). The density of sticks in each 1 μm square quadrat is shown in (c) shows the bundle length distribution measured for the CNT film shown in (a), and (d) shows the bundle length distribution calculated from all sticks across the 17 films studied.

The CNT bundle length distribution for a given deposition time, an example of which is shown in Figure 4.5 (c), was consistent across all devices fabricated. A total of 4804 sticks were measured across 17 CNT films with a range of CNT submersion times of

1 min to 80 min. The total distribution of stick length across all samples is shown in Figure 4.5 (d). The average CNT bundle length was calculated to be $L = (0.66 \pm 0.44) \mu\text{m}$ using the lengths of bundles from all devices.

The classic 2D stick percolation model by Pike and Seager [121] was examined to provide context to the CNT bundle density distributions shown in Figure 4.4 and relate them to the connectivity of the CNT network and thus the conduction across the CNT FET device. A general explanation of percolation can be found in Section 2.3.3. The percolation threshold density calculated for a random network of sticks with length L can be calculated using [121]:

$$\rho_{Th} = \frac{4.236^2}{\pi L^2} \quad (4.3)$$

The percolation threshold ρ_{Th} gives the stick density at which the average size of a connected cluster tends to infinity, where cluster refers to a continuously connected group of sticks. L is the length of a stick. For this work, the average bundle length $L = 0.66 \mu\text{m}$ was used. The stick percolation threshold across all of the CNT networks measured was calculated to be $\rho_{Th} = 13.3 \text{ bundles}/\mu\text{m}^2$ using Equation 4.3.

The percolation threshold can be directly related to whether the CNT network will span the FET device channel, or not, and how many conduction paths will span the device channel [25, 28, 72]. CNT bundle densities very near the percolation threshold will have few conduction paths across the network making the junctions along that path more critical in determining the conduction through the device channel and the response of the device to gating. Consider the metallic bundles to be a second network with a density of 13.5% of the total bundle density [26]. The maximum CNT bundle density for a device measured in this study was $(24 \pm 6) \text{ bundles}/\mu\text{m}^2$, which has a corresponding metallic bundle density of $2.9 \text{ bundles}/\mu\text{m}^2$. We assume that the metallic and semiconducting like bundles have the same length distribution. The percolation threshold calculated can thus be used to investigate the network as a whole and the subnetworks consisting of only metallic bundles or only semiconducting bundles. Thus the likelihood of a metallic path spanning the device can be discounted as the metallic bundle density is well below the percolation threshold. Metallic spanning paths that short conduction through the network are thus rejected as the primary cause of high off-currents in the CNT FET devices measured.

4.3.3 Film uniformity and the limits of percolation analysis

One of the key assumptions in the 2D stick percolation analysis is that the distribution across the surface is random and thus follows a homogeneous Poisson process or has complete spatial randomness (CSR) [146]. CSR arises when the process used to determine the locations of events on a plane is random. A property of CSR is that the mean density across all quadrats μ and variance σ^2 are equal and thus satisfy:

$$\sigma^2/\mu = 1 \quad (4.4)$$

This relationship between the mean density and its variance across quadrats can be used as a test for how close an observed process is to CSR. Random processes where the ratio $\sigma^2/\mu = 1$ are perfect Poisson processes and will exhibit some clustering due to the non zero variance of the density between quadrats. For processes where the ratio $\sigma^2/\mu \rightarrow 0$ the distribution of bundles tends towards regularity where an ordered array with even spacing and thus no variance in density would have $\sigma^2/\mu = 0$. For $\sigma^2/\mu > 1$, the distribution will exhibit more and more clustering as the variance in density across quadrats increases [146].

Figure 4.6 shows that CNT films with an average bundle density of <10 bundles/ μm^2 have more regular distributions with values $0.3 < \sigma^2/\mu < 1.3$ barring a single outlier with $\sigma^2/\mu = 2.2$. Devices with an average bundle density of >10 bundles/ μm^2 have more clustered films indicated by $1 < \sigma^2/\mu < 7$. The results shown in Figure 4.4 show an increase in the rate of change of bundle density with deposition time above 10 bundles/ μm^2 which corresponds to the observed increased network clumping as shown in Figure 4.6. Increased clustering behaviour for higher average network densities which have been deposited for a longer time as shown in Figure 4.4 could be explained by considering the attraction during deposition between the CNTs in suspension, the substrate, and CNTs that have already been deposited.

Consider the sequential deposition of CNTs onto the substrate. At the start of the deposition process, there were few bundles on the substrate, so the CNTs would be attracted to the 2-thiolpyridine which was uniform across the substrate surface and so will result in a non-preferential spatial deposition. When a CNT in the suspension comes close to the surface it is brought into contact with the SiO_2 by the 2-thiolpyridine [91].

Figure 4.6: The ratio of the variance of the density of CNTs across each device over the mean density of CNTs calculated by splitting each AFM image into 25 $1\mu\text{m}$ squares and taking the bundle density in each square. The ratio gives an indication of the uniformity of the distribution, with $\sigma^2/\mu = 1$ corresponding to CSR. $\sigma^2/\mu < 1$ indicates regularity, and $\sigma^2/\mu > 1$ indicates a clumping distribution.

Additionally, if there is already a CNT or bundle already on the substrate such that the CNT in suspension and the CNT on the surface would come into contact with it, there is an additional attraction due to the Van der Waals attraction between bare CNTs. Attraction to CNT bundles already on the surface could yield preferential deposition to regions

with more bundles resulting in the observed clustering for higher density CNT networks.

Testing the proposed physical cause for these observed transitions in the network topology above 10 bundles/ μm^2 could be approached in future work. Using surfactant wrapped CNTs in suspension to suppress the CNT-CNT attraction is a known method for producing CNT films of single nanotubes. Examining the Poisson ratio of such films would give insight as to whether the clustering can be attributed to the preferential adhesion of CNTs in suspension to regions of the substrate with CNTs already present. Conversely, the process by which the CNT film is generated can be modeled by incorporating a probability of deposition for a tube which depends on the presence of tubes already present. A secondary Poisson process where sticks are placed at Poisson random points, and then subsequent sticks are placed with some normal distribution about those could also be compared to experimental results to determine whether the experimentally observed variation in Poisson ratios could be reproduced.

The primary focus of this work was to examine the link between network density and CNT FET electrical performance. Future work focusing on the properties of the network density using experimentally measured networks and models of the deposition process would continue to build off of the work done here to characterise the experimentally observed network properties.

4.4 Electrical characterisation of locally gated CNT FET devices

4.4.1 CNT FET transfer characteristics

Figure 4.7 (a) shows the top gate device geometry selected to allow direct comparison between the electrical measurements made with different gate configurations. The close matching of thickness and dielectric constants between the back dielectric SiO_2 (300 nm) and top dielectric SU8 (325 nm) (see Chapter 3), which both have dielectric constants of 3.9 [38, 135], ensures that the gate fields generated by different gate electrodes at the CNT network closely match between gate configurations. Using equation Equation 3.1 and the thicknesses and dielectric constants of both materials, the capaci-

tance of top and back gate agree to within 5% for a given gate voltage.

Transfer characteristics were measured for all gate configurations in each CNT FET device. Examples of the transfer curves of three devices with CNT bundle densities spanning the percolation threshold of 13.3 bundles/ μm^2 are shown in Figure 4.7 where only one partial and one total top-gate are shown for visual clarity. The on-off ratios for all gates on each device are explored in greater detail in Figure 4.8. The three devices in Figure 4.7 (b), (c), and (d) were fabricated with 3 min, 5 min, and 15 min CNT submersion times resulting in CNT bundle densities of (4 ± 2) bundles/ μm^2 , (8.5 ± 2.0) bundles/ μm^2 , and (14 ± 5) bundles/ μm^2 respectively. Application of the back gate affects the conductivity of the entire active device area through the 300 nm of SiO_2 (solid blue). The total top gate (green dashes) gates only a 12 μm wide section of the network that spans the entire 60 μm device channel width. The partial top gate (red dots), which is also 12 μm wide, spans only one-third of the device channel width, at a length of 20 μm . An annotated image of the device is shown in Figure 4.7 (a), and the full dimensions and device cross section can be found in Chapter 3. The devices shown in Figure 4.7 (b), (c), and (d) have back-gated on-off ratios of 10000, 10000, and 47 respectively. The back gating affects the CNTs bundles across the entire network between the source and drain electrodes, including at the interface between the CNT film and the metal source and drain electrodes where Schottky barriers are formed. These Schottky barriers dominate the gating in CNT FET devices where the gate area spans the entire CNT film [71, 89, 125]. In contrast, both the total and partial top gates do not affect the CNT bundles in the network close to the electrode edge due to the 12 μm lateral separation between the top gates and the source or drain electrodes. The switching observed from gating the total top gate can thus be attributed solely to gating within the network, discounting contribution from the source and drain electrodes.

The ability of the localised top gates to affect the conduction can be directly related to conduction within the network. It is thus of interest that the partial top gate alters the conduction through the network by a significant factor only for the lowest density device shown in Figure 4.7 (b) with an on-off ratio of 10^3 . The total top gate and the back gate on-off ratios are 10^4 for the same device, which implies that the effect that causes the maximum gating is localised to the region gated by the partial top gate, rather

Figure 4.7: (a) annotated optical microscope image of top gate geometry used to allow gating of regions of the CNT network. (b), (c), and (d) are transfer curves for CNT FET devices with average network densities of 4 ± 2 , 8.5 ± 2.0 , and (14 ± 5) bundles/ μm^2 respectively. Each curve shows the gate voltage V_G swept between -20 V and 20 V, while measuring the current through the device I_{DS} . The back gate (solid blue) gates the entire active device area. The total top gate (green dashes) spans the entire device channel width, while the partial top gate (red dots) spans only one-third of the total device channel width. Transfer curves for only the leftmost total top gate and the bottom partial top-gate are shown in (b), (c), and (d) for visual clarity. The color of the transfer curve in (b), (c), (d) is matched to the color of the outline of the corresponding gate area in (a).

than being distributed across the network area. The lack of partial top gate effect in Figure 4.7 (c), when the other two gates show on-off ratios $\geq 10^{2.7}$, shows high on-off ratios due to gate-sensitive regions that are not localised under the partial top gate. The cause of the localised gate sensitivity is proposed to be due to m-s junctions that are in, some cases, localised such that they are sensitive to partial top gating. The on-off ratios for all of the conducting devices fabricated were compared to explore the variation in gate sensitivity further.

4.4.2 Effect of CNT network density on FET on-off ratios

Figure 4.8 shows the on-off ratio of back gates (blue), total top gates (green), and partial gates (red) over the full range of CNT FET devices fabricated with respect to their average CNT bundle densities. The on-off ratios of the transfer curves shown in Figure 4.7 (b), (c), and (d) are shown in the shaded region of Figure 4.8. Above the classic percolation threshold density of $13.3 \text{ bundles}/\mu\text{m}^2$, the back-gated on-off ratio decreases from 200 to 20 as the CNT bundle density increases, the total top gate on-off ratio decreases from 10 to 4, while the partial top gate on-off ratio shows no change and remains < 4 . The transfer characteristics of all devices with CNT bundle densities above the percolation threshold had the same general shape, as shown in Figure 4.7 (d).

Eight CNT FET devices were fabricated with average CNT bundle densities above the percolation threshold of $13.3 \text{ bundles}/\mu\text{m}^2$. All were conductive, resulting in a 100% device yield consistent with the high probability of a connected and thus conductive device above percolation. The two devices fabricated with CNT bundle densities below the percolation threshold have back-gated on-off ratios > 1000 and total top gate on-off ratios of 700. Their full transfer characteristics can be seen in Figure 4.7 (b) and (c) respectively. The device with the lowest CNT bundle density (transfer curves in Figure 4.7 (b)) of only $(4 \pm 2) \text{ bundles}/\mu\text{m}^2$ had a partial top gate on-off ratio of 300, almost two orders of magnitude higher than any other device measured. Only two out of nine devices fabricated with CNT bundle densities below $13.3 \text{ bundles}/\mu\text{m}^2$ were conductive, resulting in a 22% device yield. This is consistent with the low probability of a complete conduction path forming for a CNT network density below the classic percolation threshold ρ_{Th} .

given the variation in network density and L observed in the devices measured. More data points at low densities would be desirable, as Figure 4.8 shows the most significant change between 4 bundles/ μm^2 and 15 bundles/ μm^2 . However, the low network densities that are the cause of this change also causes low yield at devices at these densities. This provides a strong motivation for the simulated investigation of these systems in Chapter 5, as low yield at low densities can be compensated for by being able to simulate orders of magnitude more systems.

The decrease in the back-gate on-off ratio as the CNT bundle density increases is consistent with the observed trend in on-off ratios in previous work, where it was attributed to an increased number of metallic conduction paths carrying an increased current in the off-state, thus reducing the on-off ratio [5, 61, 85, 101, 147]. The maximum metallic bundle density of 2.9 bundles/ μm^2 was calculated from the metallic bundle percentage of 13.5% times the maximum observed network density of (24 ± 6) bundles/ μm^2 . This maximum metallic bundle density was well below the classical percolation threshold of 13.3 bundles/ μm^2 as well as being below the lowest network density observed to exhibit conduction of 4 bundles/ μm^2 . Even when considering that the metallic content of the networks will have increased from the 1% expected from the as purchased buckypaper to 13.5% when taking into account the metallic content of CNT bundles. The density of metallic bundles is thus lower than what could be reasonably expected to cause metallic conduction paths across the network, either by considering the experimental lower conduction limit or the percolation threshold.

Stadermann et al. [14] has shown that for low-density regions of a CNT network the conductance is dependent on m-s junctions with large conductance drops across them and that for high-density networks the conductivity is instead related to the number of local connections. I propose that the decrease in switching performance with increased film density was due to the increased number of local parallel conduction paths that circumvent gate-sensitive metallic-semiconducting CNT bundle junctions within the network.

Figure 4.8: on-off ratio with respect to the average CNT bundle density for the full set of conductive CNT FET devices gated via the global back gate (blue), the total top gate (green) and the partial top gate (red). The highlighted devices denoted with (b), (c), and (d) correspond to the transfer curves shown in Figure 4.7 (b), (c), and (d) respectively.

4.5 Junction dominated gate-dependence of network CNT FETs

The metallic bundles in the CNT networks allow conduction through paths consisting of metallic bundles, and also through paths where junctions with semiconducting bundles have been formed in the network. An m-s junction causes an increased resistance

when compared with a s-s' junction or a m-m junction due to the Schottky barriers that form [14, 15, 31, 68, 92, 114, 124, 126, 127]. The significant presence of bundles in the CNT films measured results in a high number of m-s junctions that dominate the conduction through the CNT network. Previous works by others have used scanning probe techniques to show that conduction through CNT networks is dominated by key m-s junctions. These effects are observed in the literature as conduction steps, at only some junctions, within the network [14, 31, 116, 124].

In past work with collaborators, we have investigated the local gating at individual crossed junctions within a CNT network [11]. This was achieved using a conductive AFM tip held at a distance from the junction to electrostatically gate a single junction within the CNT network. The conductance was measured through the network as a whole while individual junctions were gated. The CNT networks were fabricated as described in Section 3.3 by me, and the AFM gating was performed by Marissa P. Dierkes under the supervision of Dr. Colleen Marlow. Our results showed that only certain junctions affect the conductance through the network as a whole when gated using the AFM tip. This is consistent with the work in the literature showing conductivity jumps at only some junctions [14], which are caused by Schottky barriers. Schottky barriers between CNTs in the literature have strong gate dependence, while m-m and s-s junctions that do not form Schottky junctions do not [68, 114]. Our work in Thanihaichelvan et al. [11] which combines this AFM tip gating with sensitivity data from electrostatically gated CNT sensors supports the idea of some junctions dominating the gate response of the CNT network as a whole.

The significant increase in top-gated on-off ratios for CNT bundle densities below the percolation threshold can be explained by gate-sensitive m-s junctions becoming more dominant as the network morphology changes. Figure 4.9 depicts a schematic representation (not to scale) of the conduction path(s) through CNT networks with varying network density. Bundles containing only semiconducting CNTs are shown in black, while metallic bundles with at least one metallic CNT are shown in grey. The gate-sensitive m-s junctions formed at their intersections are highlighted by green circles to illustrate when they dominate conduction, and when they can be gated by the local gates shown in blue.

Figure 4.9: Representation of the conduction paths present in top-gated CNT random networks for networks (a) and (b) below, and (c) above the percolation threshold for semiconducting CNT bundles. Dimensions are not to scale. The total network area is shown in red, and the area gated by top gates are shown in blue. Junctions between metallic and semiconducting bundles are highlighted in green.

Figure 4.9 (a) shows a network which is above its percolation threshold, but where the semiconducting bundles are not percolating. There are few conduction paths, and those paths contain gates sensitive m-s junctions which can be gated by the top gates shown. The network shown in Figure 4.9 (b) likewise has very few conduction paths, but all conduction paths cannot be gated with the partial top gate, only the total top gate. Such a network would exhibit a strong gate response to the total top-gate but not the local top-gates. In Figure 4.9 (c) the network is more dense, such that the semiconducting bundles percolate and the network exhibits a higher degree of connectivity [31, 131]. The gate-sensitive m-s junctions shown in green have parallel conduction paths around them locally such that current through the network is not forced through those junctions. Thus, while those junctions will be able to be gated by any number of gate configurations, the effect of that gating on the network will be minimised. The lack of conduction dominance by m-s junctions in highly interconnected local regions of a CNT network has been shown using cAFM [14] and can be linked to reduced gating across the device if these junctions are being circumvented locally. The transfer characteristics are seen in Figure 4.7 (d) and the on-off ratios shown in all of the devices with CNT bundle densities above the percolation threshold in Figure 4.8 are representative of the schematic in Figure 4.9 (c).

4.6 Conclusion

In this chapter, the spatial extent of conduction through CNT networks of mixed bundles was investigated via localised gating of CNT networks of varying density to show the effect of network topology on electrical characteristics. CNT networks were fabricated with varying deposition times to tune their density. In order to fully characterise the morphology and topology of the different networks, stick modelling of AFM images taken from samples at each deposition was used. Cross sections of the bundles measured were used to define a probability that a bundle of a given diameter would contain at least one metallic single tube. We made a simplifying assumption that any bundle containing a metallic tube would act as metallic. The proportion of metallic bundles was calculated to be 13.5% for the networks fabricated based on this assumption.

The length and position of bundles were measured for CNT films from each deposition time. The classical stick percolation threshold was calculated to be $13.3 \text{ bundles}/\mu\text{m}^2$ using the average bundle length measured of $(0.66 \pm 0.44) \mu\text{m}$. The stick positions measured across all network densities were used to calculate the variation in density across each network measured. Networks fabricated with densities $<10 \text{ bundles}/\mu\text{m}^2$ tended towards complete spatial randomness or regularity, while networks with densities $>10 \text{ bundles}/\mu\text{m}^2$ tended to be more clustered or clumpy than a random network. Such deviation from a random network as well as the uncertainty in L has indicated that while the percolation threshold provides a useful metric for describing the density of the network, it cannot be taken as a hard limit as would be expected from classical stick percolation. A more in-depth study of how the percolation threshold is affected by variations from the perfect randomness would benefit from continued study in order to build from work in the literature considering finite size affects [28] and variation in the stick length [27]. The electrical characteristics of the CNT networks fabricated further support the need for a more detailed analysis of percolation. CNT networks with densities as low as $4 \text{ bundles}/\mu\text{m}^2$ were shown to conduct, where classical stick percolation would exclude any networks with densities below $13.3 \text{ bundles}/\mu\text{m}^2$ from doing so.

The gate-dependence of the density varying CNT networks were investigated after

characterisation of the physical characteristics of each CNT network. The local gate response was significant for devices with CNT network densities <10 bundles/ μm^2 with a maximum on-off ratio of 10^3 at these low network densities. Back-gated on-off ratios varied from 10 to 10^4 from high to low density in the range of 4 bundles/ μm^2 to 25 bundles/ μm^2 .

The networks studied all had bundle densities below what would be required to have metallic shorts across the network. We attribute the increase in gate sensitivity to the increased dominance of m-s junctions within the network. The few parallel conduction paths within the network at low densities results in current flow being forced through gate-sensitive m-s junctions. The increased back gate sensitivity is due to a decreased number of alternate conduction paths as density decreases. At low network densities these few paths would be increasingly localised which will increase the likelihood that localised gating will have a significant effect on conduction throughout the device, provided that the gate-sensitive junctions were in the region of local gating. We further examine this model in Chapter 5 by constructing a simulation of a CNT network system where m-s junctions are the only gate-dependent elements. The effect of changes in the gating with network density are compared between the experimentally measured systems and the simulated work.

In order to progress understanding of CNT network electrical systems, a more nuanced understanding of the effect of network topology on electrical performance must become standard. The analysis of the density uniformity in this work highlights the need to extend the model of a percolating system beyond perfectly random constant length percolating systems. The significant gate responses shown at densities below the classic percolation threshold further highlight the need for improving on the model of network topology and conduction to better represent the actual physical system.

Chapter 5

Simulation of junction dominated random network CNT FET devices

5.1 Introduction

Networks of carbon nanotubes (CNTs) allow the electrical characteristics of CNTs to be realised in device platforms that can be readily fabricated at scale [5, 84, 85]. Simulations of the conduction through networks of CNTs in the literature have been almost exclusively focused on how the conductivity of a network of CNTs depends on the physical parameters of the network such as network length and width, stick density, alignment, size distribution, and the relative resistance of its components [27–32, 69, 79, 90, 93, 123, 131, 148–150], rather than focusing on the gate-dependence of a CNT network in a field effect transistor (FET) device.

The effect of network topology and how the conduction mechanism at m-s junctions affects the overall conduction when gated is investigated here. Excluding Kocabas et al. [79], none of the CNT network simulation literature uses a model which explicitly incorporates the gate-dependence. To examine the gate-dependence, we draw on literature studies that extend the study of the dependence of the network conduction on its physical parameters. The idea of a blocking network put forward in Topinka et al. [31] is extended by treating metallic-semiconducting (m-s) junctions as the only explicitly gate-dependent junctions. Treating m-s junctions as blocking conduction [31], and

the extension of their assumption to making m-s junctions gate-dependent so that they effectively block current at high gate voltages, is consistent with the literature on Schottky junctions formed at m-s junctions [36, 68]. By doing so, the effect of gating simulated networks at a variety of densities can be investigated.

This chapter begins by describing the developed algorithm for the formation of conducting CNT networks, and the subsequent solving of the resulting conducting network for the current and voltage throughout. The simulation framework was written to be adapted to any arbitrary conduction mechanisms, or indeed materials, in order to provide an adaptable codebase for further study. Despite the number of CNT network simulations in the literature, there are none based on an open and accessible codebase. This work endeavors to change this by ensuring that all of the code and development information is open source and transparent.

Monte Carlo methods were used to generate many random networks with the same network parameters. Firstly, the physical percolation threshold of the system was investigated, and the variation in the size of connected clusters of CNTs over this percolation threshold was shown. The gating of the system was then investigated by applying gate voltages to localised regions of the simulated CNT networks and measuring the overall conduction response. The systems were shown to have higher switching responses at low network densities just above the percolation threshold. This is explained by considering the restriction of conduction through key paths. The trends in both local and global gating are explained in terms of m-s junctions in these key paths dominating the conduction through the network. The importance of these dominant m-s junctions in explaining the gate-dependence shown in both low and high-density networks was compared with the experimental results from Chapter 4.

We conclude by examining the significance of these results in informing the understanding of conduction through random networks of CNTs for device platforms. Future use of the simulation developed, further applications, and the limitations of its use are then discussed.

5.2 CNT network simulation algorithm and conduction mechanism

An algorithm for the formation of the network and solving for the electrical state was developed to test the effects of gate-dependent m-s junctions on CNT networks with varying network density. The key characteristics of such a network simulation were that:

1. It must be able to produce a random network of sticks and determine the intersects.
2. It must be able to generate an electrical system from the sticks and intersects and solve for the current and voltage through the system as a whole.
3. It must maintain spatial positioning of components to allow localised addressing of components within a region.
4. It must include gate-dependence.
5. It must be capable of handling systems of a size comparable with the experimental work in Chapter 4. Areas of $60\text{ }\mu\text{m} \times 60\text{ }\mu\text{m}$, and stick densities of 5 sticks/ μm^2 to 20 sticks/ μm^2 .
6. It must be computationally efficient enough to run such simulations within a reasonable time (less than a day) on a single core.

The challenges and design evolution involved in meeting these points are detailed in Appendix B. The algorithm developed is detailed below.

5.2.1 Algorithm for random network generation and conduction solving

The parameters required in order to generate a simulated network of CNTs and its electrical characteristics are μ the density of sticks in the network and the network dimension l . The number of sticks n to be generated in the model is thus $n = l^2 \cdot \mu$. We denote the

length distribution of those sticks L and the percentage of those sticks that are metallic as opposed to semiconducting p_m . Additionally, the conduction mechanism at the junctions must be specified. The conduction mechanism and mapping are covered in detail in Section 5.4. Provided that the conduction elements have a linear response to their driving voltage, the conduction elements can be considered as simple resistors. The algorithm for the formation and solving of the system is thus solvable without resorting to differential equations.

Figure 5.1 shows a simplified diagram of the main steps in the formation of a model of a conducting system of CNT bundles. Figure 5.1 (a) depicts the formation of the physical sticks, which are representative of bundled CNTs. The physical characteristics of each stick are generated at this stage. Figure 5.1 (b) shows the detection of junctions within the network of physical sticks. The connected clusters of sticks within the network are identified and shown in Figure 5.1 (c). The spanning cluster, which connects both of the source and drain electrodes, is used to produce an electrical circuit graph structure shown in Figure 5.1 (d). The circuit graph is used to calculate the current and voltage through the system. A step by step description of the algorithm used to generate the physical network, identify junctions and clusters, produce a circuit graph structure for conduction calculation, and then solve that graph for the input voltage conditions follows. The description references Figure 5.1 where appropriate, and notes where aspects of the algorithm are not immediately obvious when only considering the restricted system shown there.

Algorithm sequence

1. The process of generating a simulated CNT network begins with the generation of n sticks across a square area of length l as shown in Figure 5.1 (a). Each stick is generated with a random center point (x_i, y_i) within that area using a Poisson random process. A random angle θ_i and length L_i from the experimentally determined distribution of bundle lengths L are assigned. Each stick is denoted as either semiconducting or metallic with a probability of being metallic defined by p_m . Stick properties are stored in a data frame structure, with one row per stick and columns for each property.

Figure 5.1: Pictographic representation of the network construction process in the simulation of a network CNT FET. The black edges to the left and right denote the source and drain electrodes. (a) random stick placement where colors of the sticks are representative of whether they are semiconducting (blue) or metallic (red). The parameters for a single randomly placed stick x_i, y_i, θ_i, L_i have been labeled. (b) junction identification with junctions labeled with key m-s junction highlighted (green), (c) cluster identification showing connected clusters of sticks. The pink cluster is the spanning cluster and is used in (d) the electrical network construction where sticks become graph nodes, and junctions become graph edges containing conducting elements.

- Intersection between sticks is determined by pairwise calculating the interaction of line segments using a standard algorithm [151]. The location of each intersect (x_{ij}, y_{ij}) is recorded as well as which sticks composed the intersection. The positions and types of intersects are recorded, as shown in Figure 5.1 (b), whether they are m-m, m-s, or s-s. Intersects with the left and right edges are also recorded as electrode junctions. Intersects that would occur outside of the device area are discarded. All junction information is stored in a data frame structure, with one row

per junction and columns for each property.

At this point, the data on the system exists in two dataframe structures: 1. the list of sticks and their properties, and 2. the list of intersects and their properties described above. However, this type of flat data structure is not a natural way to interact with the data, which is reflected in the efficiency of the following steps when they were initially performed using these two lists. A more natural way to represent the data is in a graph structure using the python *networkx* module [152] as described below:

3. A circuit graph structure is constructed by using the list of junctions as an edge list. Each stick in the network is represented as a node in the graph structure and each junction in the network as an edge. Each node and edge in the graph holds a dictionary of the properties of each stick and junction respectively.
4. Cluster determining algorithms are mature and heavily optimised for graph structures. The number and size of connected clusters within the graph are calculated Using Tarjan's algorithm for connected component calculation implemented in *networkx* [152, 153]. The size of each connected cluster is then stored to provide insight into the percolating characteristic of the network.
5. If both the left and right edges of the device area contact a single connected cluster, then that cluster is denoted as the spanning cluster and conduction will be able to occur. The following steps on conduction are only performed on the spanning cluster provided that it exists.
6. Each graph edge is populated with a conduction object depending on the mapping between the type of junction and the conduction objects uses. The only requirement of such an object is that it be able to return its conductance when queried. The conductance need not depend on the gate voltage (*e.g.* for m-m junctions) but does for m-s junctions. The graph edges are then updated with a conductance for the voltage state, initially $V_G = 0$ for all junctions.
7. Using the conductance of each edge as an edge weight, an adjacency matrix is formed which is then modified to include a voltage source at a fixed voltage V_{DS}

at the node representing the left edge of the device, and ground at the node denoting the right edge of the device. For details of the formulation of this matrix see Cheever [154].

8. The voltages at each node in the graph were calculated using modified nodal analysis, which is an extrapolation of Kirchhoff's circuit laws to a matrix equation form [155]. The currents in the network were then calculated by applying Ohm's Law using the conductance of each edge and the voltage difference across its two endpoint nodes $I_{ij} = G_{ij}(V_j - V_i)$. The total current through the network can then be measured as the sum of currents through the source or ground node.
9. Each edge in the graph stores the position of the corresponding junction x_{ij}, y_{ij} as metadata. The gate voltage can be changed for only those junctions that exist within a specified spatial region. After the gate voltage has been set, and the edge conductance across the network is recalculated, and the voltages and currents in the network can be updated.
10. The current through the elements in the network can be summed to get a total current for a given gate voltage. Varying the gate voltage produces transfer curve measurements. The current and voltage within the network can be visualised spatially for current density and equipotentials respectively.

After this algorithm, the simulation produces a full physical map of the sticks, their properties, and connections. A conduction graph encoding the position and electrical properties of the conducting elements is formed that can be addressed locally to change the gate voltage. The conduction graph can then be solved to produce the voltage at each graph node (stick), and the current through each graph edge (junction). The algorithm detailed above is capable of simulating a $60\text{ }\mu\text{m}$ square network with a density of up to $20\text{ sticks}/\mu\text{m}^2$ or ~ 70000 total stick elements. Such a simulation would require ~ 2.5 hrs on a single core of a standard modern CPU (Intel(R) Core(TM) i5-4590 CPU 3.30GHz) for the full network generation and conduction calculation at a single gate voltage.

The code written to run the simulations presented in this work has been made open

source and is covered by the MIT open license agreement [156]. Link to the code repository, descriptions of the specific inputs and outputs of the simulation code, and discussion of the development process that occurred during development can be found in Appendix B.

5.3 Simulation and modeling of CNT networks in the literature

Behnam and Ural [29] considered how the ratio of the tube to junction resistance effects the fit of their simulation to the experimentally observed dependence of the overall resistance on the network length. However, it was only one of many parameters investigated, and so the only conclusion that they drew regarding this was that the highest ratio investigated of 100 was most suitable for fitting their observed trends.

Pimparkar et al. [90] considers the impact of varying the percolation threshold locally within the network by etching the network into thin strips, and so disrupting metallic conduction paths that would otherwise exist due to the density of the network as a whole. By disrupting the network locally and anisotropically, they were able to improve the device characteristics and thus show good agreement between their experimental tests and simulations of the same system. Their use of the total, metallic, and semiconducting percolation thresholds individually allowed a clear argument for the lack of shorted and gate insensitive conduction paths through the network.

It is important to consider the impact of varied metallic content on the network conduction, however, with the recent development of purification techniques to allow for tuned amounts of semiconducting CNTs up to 99.9% for device fabrication [55, 83, 119, 120] it makes more sense to investigate the case where metallic CNTs do not short the network. This work takes inspiration from Topinka et al. [31], which provides clear example of a careful investigation of varying metallic % on a CNT network's electrical properties. They also consider the extent to which a model of the physical process in a conducting network can be simplified in order to highlight properties of the system due to the interaction between network topology and the constituent elements.

Topinka et al. [31] considers a simplified model of the conduction of the elements within a CNT network in order to demonstrate "phase" changes in the nature of the conduction through the network as a whole. They have simplified the relative resistances in the network as follows: They simplify the system so that 1. m-s junctions block conduction and 2. all other CNTs and junctions conduct equally. The decision to treat m-s junctions as blocking conduction is based on their cAFM measurements showing many orders of magnitude higher resistance across them and extensive literature measurements showing, not just the high resistance of such m-s junctions, but their significance as gate-dependent elements due to the Schottky junctions formed [14, 15, 31, 68, 114, 116, 124, 150]. Topinka et al. [31] focus on the effect of these simple blocking junctions on the conduction through the whole network as a function of network density and the percentage of metallic CNTs. They observe sharp transitions between networks where conduction is through only semiconducting CNTs, only metallic CNTs, and blocked networks where there is a mix of both resulting in a large amount of m-s junctions. From these sharp transitions, shown in Figure 2.6, they then make recommendations that devices with network densities with densities one to three times the percolating threshold and metallic percentages between 66% and 90% semiconducting will produce networks that are dominated by m-s junctions.

5.3.1 Conduction mechanisms used in the literature on CNT network simulations

Fixed resistance models

Many papers use fixed resistances attributed to the junctions and tubes in the network to calculate how the conduction varies with the physical parameters of the network [29, 69, 93, 157]. Gong et al. [69] and Ishida and Nihey [157] treated semiconducting tubes as 10^3 to 10^5 times more resistive than metallic. Likewise the m-s and s-s junction resistance used was 2×10^2 to 10^3 times more resistive than mm junctions [69, 157]. Behnam and Ural [29] investigated a range of junction to tube resistance ratios from 10^{-2} to 10^4 and found a ratio of 10^2 best fit their results. These works cite Fuhrer et al. [13], Snow et al. [25], and Fuhrer et al. [68] as sources for estimating those resistance values.

Drift diffusion models

So-called drift-diffusion models were initially put forward in Kumar, Murthy, and Alam [28] as an alternative to fixed resistance simulations. However, the fixed values for the coefficients used do not add any additional capability to the models using fixed resistances, despite being motivated by the charge transfer between tubes. The junctions and their differing characteristics are captured by a charge transfer coefficient $c_{ij} = G_i/G_j$ where G_i and G_j are the mutual self conductances of the tubes involved. c_{ij} is taken directly from the difference in contact resistances from experimental papers [25, 68]. Several papers use this model, and select the charge transfer coefficient to be 50 [28, 30, 79, 90]. It is my view that the drift-diffusion models do not add anything more to the model of conduction through CNT networks than a fixed resistance system. This is a good example of the addition of more complex mathematics into a model obscuring the underlying methods used with jargon and convoluted equations without providing any significant benefit.

Fixed resistance models provide an example of the simplest possible model of conduction in a network system. Such a simple model is suited to comparison between experimental and simulated measurements of CNT network systems with varying physical parameters. In the case of this work, where the primary goal of the simulated system is to compare with experimental transfer curve and on-off ratios, a fixed resistance model is insufficient, especially due to the lack of a simple way to determine the off resistance of elements in the system. Experimental work in the literature that is used to select fixed resistances of CNT junctions and tubes do not present direct quantities of the off state resistance when gated [13, 15, 114]. The transfer curves that are presented can be used to estimate the magnitude of switching, even if a specific value cannot be obtained.

Density of states based models

Two papers since 2016 have incorporated a DOS-based calculation into their simulated conduction model [131, 149], however, neither consider gating in the system. These two papers and [148] all consider tunnelling mechanisms to simulate conduction through a CNT network.

Schiessl et al. [131] calculates "the bond conductance between two sites in a disordered system of sites, over which charges can hop, in the case of a small electric field F and in a mean field approximation" [131] using:

$$G_{ij}(E_F, E_i, E_j) = \frac{e^2 \cdot \omega_{ij}}{4k_B T \cdot \cosh(\frac{E_i - E_F}{2k_B T}) \cdot \cosh(\frac{E_j - E_F}{2k_B T})} \quad (5.1)$$

Where everything has the normal definitions including ω_{ij} simplified using a Miller-Abrams approach to be

$$\omega_{ij} = \omega_0 \cdot \exp\left(\frac{-|\Delta E_{ij}|}{2k_B T}\right) \quad (5.2)$$

ω_0 is unknown, so they only calculate relative mobilities from Equation 5.1. This is extended to the case where each site has an energy distribution given by its DOS. In this case Equation 5.1 is extended to become:

$$G_{ij}^{junct}(E_F) = \int \int G_{ij}(E_F, E_i, E_j) \cdot D_i(E_i) \cdot D_j(E_j) dE_i dE_j \quad (5.3)$$

The approach that they present provides a good example of a possible extension of the work I have done to incorporate a range of band gap CNTs. By doing so, the simplification of considering either s or m type tubes would expand to tubes with a band gap corresponding to their density of states. m-s junctions could then be considered to consist of a range of junctions with varying Schottky barriers due to the difference in band gaps of sCNTs with different chiral vectors.

5.4 Selection of a network conduction mechanism

In this work, the selection of a conduction mechanism to represent the field dependence of the CNT network was motivated by two primary considerations:

1. The conduction mechanism must describe how the network conduction varies with gate voltage.
2. The conduction mechanism must be as simple as possible.

The goal of this simulation is to compare with the experimental transfer characteristics and on-off ratios shown in Chapter 4. We observed a sharp increase in on-off ratios at network densities below 15 bundles/ μm^2 to 10 bundles/ μm^2 for both locally gated top gates and global back gate. The networks in those experimental devices were well below the metallic percolation threshold, so increased metallic shorts cannot be taken as the cause of the sharp observed change in on-off ratio at low network density.

Our previous work [11], as well as work by others [31, 124, 125] suggests that the junctions dominate the conduction and gating within a CNT network. Schottky junctions formed between the metallic and semiconducting CNTs have are strongly gate-dependent [15, 68], and dominate the conductance and gating through the network [14, 31, 124]. As described in Chapter 4, I have fabricated a mixed network of single CNTs and bundles. We describe there the assumption that bundles which contain at least one metallic tube will act as metallic to form Schottky junctions. Our assumption is supported by experimental work by Stadermann et al. [14] and others [31, 77, 80, 124, 128] which showed m-s junctions dominating the conduction of networks of mixed bundles and tubes. They use the work by Fuhrer et al. [68] to support their description of the Schottky barriers that form at m-s junctions.

We adapt the methodology of Topinka et al. [31], where they use a simplification of the conduction in the network to be 1 everywhere except at m-s junctions, which they set to block conduction. Making a clear assumption in order to investigate the impact of the m-s junctions satisfies our criteria for the simplicity of the conduction model. However, we also require that our model describes gate-dependence. We consider a simplification of the current through a Schottky barrier due to thermionic emission in order to include gate-dependence.

$$I = AA^*T^2 \exp(-\varphi_B/V_T) [\exp(V/V_T) - 1] \quad (5.4)$$

The equation for current through a Schottky junction due to thermionic emission is shown in Equation 5.4 again for clarity. Taking estimates of the constants involved we take the temperature $T = 300$ K, the contact area between bundles $A = 1 \text{ nm}^2$, the thermal voltage $V_T = 25$ mV at room temperature [158], and the effective Richardson constant $A^* = 1.2 \times 10^6 \text{ Am}^{-2}\text{K}^{-2}$ [38]. $[\exp(V/V_T) - 1] \propto V$ for small V . The driving

voltage across a device measured in this work is at most 100 mV, which means that the voltage drop across any junction must be ≤ 100 mV. The output characteristics shown in Figure 2.3 show the linearity of the devices used here for $V_{DS} = 100$ mV and Lee et al. [15] demonstrates linearity in V for single junctions under $V_{DS} = 100$ mV [13, 68]. Taking the current to be linear in V and adding estimate values into Equation 5.4 we get:

$$I = 1.08 \times 10^{-7} \exp(-4\varphi_B)V \quad (5.5)$$

The gate voltage will directly modulate the Fermi level at the Schottky barrier [38], thus $\varphi_B \propto V_G$. The conductance through the junctions will depend on the gate voltage as:

$$G = \alpha \exp(-\beta V_G) \quad (5.6)$$

with α and β constants. The primary consideration in choosing these constants was that they produce on-off ratios of $\sim 1 \times 10^{-5}$ over the range $V_G = -10$ V to 10 V, consistent with values for the resistance range of an m-s junction observed in literature [15, 68]. They must also normalize the on conductance to be 1 for the on-voltage $V_G = -10$ V to 10 V fitting with Topinka et al. [31]. $\beta = 0.5$ was used to enforce a 10^5 on-off ratio from gate voltage and $\alpha = \exp(-10 * \beta) = 6.7 \times 10^{-3}$ to normalise the on-conductance to be one. Figure 5.2 shows the shape of the conductance with gate voltage curve used to simulate the junction-conduction shown in Equation 5.6.

The exponential dependence based on Equation 5.6 and shown in Figure 5.2 provides an extension to the model used in Topinka et al. [31] to include gate-dependence. We did not use the full form of the conduction through a Schottky junction shown in Equation 5.5, as the constant of proportionality between the gate voltage and the Schottky barrier is unknown. A future extension of this work would be to model the electrostatics at the surface of the device to determine the exact relationship between the voltage applied to the gate and the voltage at the Schottky barrier, and modify the form of Equation 5.6 accordingly. This approach could result in improved absolute values of the conductance, but the on-off ratios should be minimally affected, as the values selected here were based on experimental results from our work and others [13, 68].

Heterogenous junctions between semiconducting CNTs with mismatched band

Figure 5.2: Form of the transfer characteristics of the junction-conductance used in simulation showing G with respect to the gate voltage V_G .

gaps exhibit gate sensitivity [15]. A possible modification of the mechanism in this work would be to incorporate the heterojunctions between semiconducting elements as additional gate-dependent elements. The existence of these s-s' gate-dependent junctions in the semiconducting regions of the network would make the circumventing parallel paths within the network less favorable. More current forced through paths that have gate-dependence would increase the on-off ratios at higher densities where these parallel paths are more prevalent. The effect of this on the work done here would be to soften the transition between high and low on-off ratios shown in Figure 5.8, and increase the on-off ratios at high network densities. Such heterojunctions have been shown to exhibit comparable gate-dependence to m-s junctions [15], with their magnitude depending on the band mismatch between the two tubes. To incorporate such analysis into the simulated work while still being able to compare with our experimental results, the chiralities of the CNTs used would be required. The purified tubes used do not have chirality distributions, or sufficient spectroscopic information included by the manufacturer (NanoIntegris) to deduce this.

There is sparse literature investigation of CNT s-s' junctions compared with studies which take a simplified examination of the different behaviour of m-s and s-s junctions [31, 50, 68, 131]. Further research on the electrical properties of crossed CNTs with mismatched bandgaps would pave the way for the inclusion of s-s' junctions into the model used here. Some existing works consider heterojunctions which occur within a single CNT due to a kink in the carbon lattice [33, 37], but this has not been extended to an explicit study of s-s' junctions between adjacent nanotubes in the primary works on crossed nanotube junctions [15, 68, 114].

5.5 Results of Monte Carlo simulations of CNT network systems

The gate-dependent m-s junction model discussed above was implemented for the conducting elements in the simulation algorithm described in Section 5.2.1. Figure 5.3 shows a representation of the final output of the algorithm described in Section 5.2.1 on a network with an area $5\text{ }\mu\text{m}^2$ and a stick density of $\rho = 12\text{ sticks}/\mu\text{m}^2$. A small network size is used for this figure for visual clarity in describing the output of the simulation algorithm described in Section 5.2.1. Following this reduced size example, this work exclusively considers larger systems with a size equal to the experimental systems measured in Chapter 4.

The sticks and junctions are shown in Figure 5.3 (a) and (d). In Figure 5.3 (a) the sticks have been colored according to the cluster of connected sticks that they belong to. If a cluster exists that spans the left and right of the device, it is called the spanning cluster and is colored black. Figure 5.4 will later detail the size of this spanning cluster with respect to the overall network size. It is this spanning cluster that is used to produce the electrical graph structures shown in Figure 5.3 (b) and (c) where the color corresponds to the voltage at the graph nodes and the current through the graph edges respectively. Figure 5.3 (e) and (f) display the voltage and current across the network area, but as contour plots without any indication of the graph structure underlying them. The $5\text{ }\mu\text{m}^2$ square system shown in Figure 5.3 is an important visual aid, but many of the plots shown are

Figure 5.3: Simulation output plots generated for a small $5\ \mu\text{m}$ square network area for visual clarity. (a) and (d) shows the generated sticks with a density of $\rho = 12\ \text{sticks}/\mu\text{m}^2$ across the network area. (a) sticks are colored corresponding to the connected cluster that they are in, with the spanning cluster shown in black. (d) stick color corresponds to the nature of each stick: blue is semiconducting, red is metallic, black represents the electrode. Green circles highlight the m-s junctions. (b) and (e) show the voltage across the network area for a driving voltage of 100 mV and a gate voltage of 0 V. (b) is the electrical conduction graph of the network, where nodes correspond to sticks and the color of the node denotes the voltage from high (red) to low (light yellow), and graph edges (black) represent conducting junctions. (e) shows the voltage equipotentials across the network. (c) and (f) show the current through the network from maximum (red) to zero (yellow). (c) shows current, with black dots representing nodes and the edges representing conducting junctions where their color is representative of current through them. (f) shows an abstraction of (c) showing current density.

impractical when considering a larger system. Instead, refer back to Figure 5.3 to provide a visual reference for the metrics used to characterise larger systems.

The full sized systems simulated in the remainder of this work were square networks with length $l = 60 \mu\text{m}$ to a side chosen to match the size of the experimental CNT networks in Chapter 4. The stick densities simulated ranged from $6 \text{ sticks}/\mu\text{m}^2$ to $12 \text{ sticks}/\mu\text{m}^2$. This range was selected after initially investigating $1 \text{ sticks}/\mu\text{m}^2$ to $20 \text{ sticks}/\mu\text{m}^2$ to determine a reasonable range over which to run Monte Carlo simulations. The parameters of the sticks used in each simulation were taken from the experimental work characterising solution deposited CNT films in Section 4.3. The length distribution used was a zero-truncated gaussian with mean and standard deviation set from the experimentally observed $L = (0.66 \pm 0.44) \mu\text{m}$. The percentage of metallic sticks was 13.5% as described in Section 4.3.1

5.5.1 Physical network characteristics

The number and size of clusters of connected sticks within the network were investigated in order to determine the percolation threshold of the simulated systems and compare with the percolation threshold as determined from theory in Section 2.3.3 as well as the experimentally observed minimum conduction threshold in Section 4.3.2. The method in Pike and Seager [121] was used to determine whether a given network is percolating: if there exists a connected cluster of sticks which contacts opposite edges of the network (spanning cluster), that network is said to be percolating in that direction. Thus to numerically determine the percolation threshold for a given set of input parameters, a Monte Carlo method was used whereby many such systems were generated with the same network densities. The lowest density at which a spanning cluster is observed is the percolation threshold. The network topology is investigated by considering the size of the largest connected cluster of sticks within each network system and whether it spans the network.

The size of the largest connected cluster from simulated networks with densities ranging from $8 \text{ sticks}/\mu\text{m}^2$ to $12 \text{ sticks}/\mu\text{m}^2$ is shown in Figure 5.4 (a). The maximum cluster size is normalized by the number of sticks in each system in Figure 5.4 (a).

Figure 5.4: Network stick density vs. the normalized maximum connected cluster size in the network. 800 $60 \mu\text{m} \times 60 \mu\text{m}$ networks were simulated with sticks with mean and standard distribution of $(0.66 \pm 0.44) \mu\text{m}$ and a network density from 8 sticks/μm² to 12 sticks/μm². (inset) the cluster size of 20 devices with densities between 1 sticks/μm² to 20 sticks/μm². (a) Spanning (blue) and non-connected networks (red) are shown. The calculated percolation threshold $\rho_{Th} = (8.670 \pm 0.005)$ sticks/μm² is shown. (b) $60 \mu\text{m}$ square simulation with a stick density of $\rho = 9.5$ sticks/μm² close to the percolation threshold. Generated sticks are color-coded by the connected cluster. The spanning cluster is labeled in black.

Red points are systems where there is no spanning cluster, and blue points are those where a spanning cluster exists. The lowest network density that shows a spanning cluster and thus defines the percolation threshold of the system is $\rho_{Th} = (8.670 \pm 0.005)$ sticks/μm². This is significantly lower than the percolation threshold of 13.3 sticks/μm² calculated for an infinite system with no variation in stick length [121] in Section 4.3.2.

Similar to Section 4.3.1, we consider the network of only metallic sticks, which by definition has a density of 13.5% of the total network density. The total network density at which metallic or semiconducting CNTs could first form a spanning cluster in the simulated systems here was $\frac{1}{0.135} \cdot \rho_{Th} = 66$ sticks/μm² and $\frac{1}{0.865} \cdot \rho_{Th} = 10$ sticks/μm² respectively.

The transition from the largest connected cluster in the system comprising <20% of the total sticks in the system to comprising >80%, seen in Figure 5.4 (a), occurs above the measured percolation threshold. As more sticks are added to the system, clusters of connected sticks form and are joined together to form larger clusters. The percolation threshold is defined as the lowest density at which a cluster which spans the network area exists [121]. Thus, across many different random networks, it makes sense for the percolation threshold to occur at the beginning of the transition from many smaller clusters within the network to one large spanning cluster.

Figure 5.4 (b) shows an example of a full 60 μm square simulation with a stick density of $\rho = 9.5 \text{ sticks}/\mu\text{m}^2$. Connected clusters are color labeled, with the spanning cluster being black. It shows the existence of many other clusters in addition to the spanning cluster. At that density of network shown in Figure 5.4 (a) there are both spanning and disconnected networks. These smaller clusters still comprise a significant portion of the total sticks for networks with densities between ρ_{Th} and $\sim 10 \text{ sticks}/\mu\text{m}^2$.

The percolation threshold $\rho_{Th}^{sim} = (8.670 \pm 0.005) \text{ sticks}/\mu\text{m}^2$ is below the classic percolation threshold $\rho_{Th}^{sim} = (13.3 \pm 0.1) \text{ sticks}/\mu\text{m}^2$ calculated in Section 4.3.2. This is consistent with a percolating system which has a finite network region [123], and significant variation in the length of the sticks simulated [27]. Li and Zhang [123] showed that for square networks with edge length $< 256L$ there was significant lowering of the spanning probability. Hicks, Behnam, and Ural [27] showed a shift to lower densities of the transition region for devices with a standard deviation in stick length σ_L comparable to the mean stick length μ_L . The sticks used in this work have $\sigma_L = 2/3\mu_L$, and a finite network area with a network length of $\sim 90\mu_L$. Thus the lower percolation threshold measured using Monte Carlo simulation here agrees with results in the literature and highlights the limits of the classical percolation equation for sticks [121] in predicting the percolation threshold of a Network of CNTs in conditions which match our experimental work.

5.6 Electrical characteristics of simulated CNT FETs

The simulation that has been developed enables calculation of the conduction through the entire network and has been constructed such that only the m-s junctions vary with gate voltage. The simulated network systems have also been constructed so that the components retain their positional information and can be addressed according to their position, even when the system has been abstracted to a graph structure to calculate the conduction. The physically addressable components can thus have gate voltages applied to them *en masse* or in any defined spatial region.

Having a gate-dependent CNT network simulation that allows local gating of the network has not been explored in the literature. It allows investigation of the effect of gating specific regions of the network on the conduction through the network as a whole, analogous to localised chemical sensing or application to conductivity tuned thin film electronics.

In this work, the gating of select regions of the network area has been used as a means to probe the localisation of gate sensitivity within the network.

5.6.1 Topology induced dominance of m-s junctions in low-density networks

The topology of the conduction paths that exist within the network are examined in order to understand the change in on-off ratio at low CNT network densities. We investigate how the network topology could cause increased dominance of the device conduction by m-s junctions at low CNT network densities.

The current density through the simulated network is used to determine the nature of the conduction paths present. However, the 60 μm square network systems simulated here that have densities in the range of 9 sticks/ μm^2 to 12 sticks/ μm^2 correspond to $\sim 30\,000$ s to $\sim 45\,000$ sticks across the network area. Because of the high density of sticks, visualising the full arrangement of sticks is difficult to interpret.

Instead, the current density through the network is visualised using a heat map, as shown in Figure 5.5. The current density is calculated from the known currents

Figure 5.5: Current across the full $60 \mu\text{m}$ square device region, with current density from maximum (red) to zero (blue) shown for (a) $\rho = 9.5 \text{ sticks}/\mu\text{m}^2$, and (b) $\rho = 12 \text{ sticks}/\mu\text{m}^2$.

through every element in the simulated network. A sparse network, with a density of $\rho = 9.5 \text{ sticks}/\mu\text{m}^2$ close to the percolation threshold $\rho_{Th} = 8.67 \text{ sticks}/\mu\text{m}^2$, causes the current to be concentrated in a few localized conduction paths as shown in Figure 5.5 (a). Conversely, a dense network with a high density $\rho = 12 \text{ sticks}/\mu\text{m}^2$ well above the percolation threshold can be seen in Figure 5.5 (b) where the current density is spread across the entire network area. The contour maps in Figure 5.5 (a) and (b) have been generated from the same network as the transfer curves shown in Figure 5.7 (b) and (d), and represent the current through the network at zero gate voltage on those plots.

Schematics of conduction pathways through a mixed network of metallic (grey) and semiconducting (black) sticks are shown in Figure 5.6 (a) and (b) for a sparse network near the percolation threshold and a dense network far away from the percolation threshold respectively. The system shown is not to scale but is used to highlight the effect of parallel conduction paths within the network that circumnavigate key components in the network.

Figure 5.6: Schematic representation of the conduction paths present in top gated CNT random networks for network densities (a) close to, and (b) well above the percolation threshold. Dimensions are not to scale. The total network area is shown in blue, and the area gated by partial and total top gates are shown in green and red respectively. Junctions between metallic (grey) and semiconducting (black) bundles are highlighted in pink.

Conduction paths through low-density networks

Figure 5.5 (a) demonstrates the restricted current paths that arise in a low-density network. Because of the low density, and the corresponding low size of the spanning cluster as shown in Figure 5.4, the current is forced through bottlenecks where there are no parallel conduction paths between regions of the network. A schematic depiction of such a sparse network is shown in Figure 5.6 (a) illustrating the lack of any parallel conduction paths. The restricted current paths shown here are fundamentally different from the metallic sections of the network that are shown by Stadermann et al. [14] using cAFM to image sections of the network that conduct when the network as a whole has been gated off. Those conducting sections are due to purely metallic conduction paths.

When the conduction is localised to conduction paths in a sparse spanning cluster, the conduction paths present must contain m-s junctions. The current is forced to flow through these junctions because the metallic and semiconducting sticks are both below their respective percolation thresholds. A schematic representation of this is shown in Figure 5.6 (a), where neither the metallic or semiconducting bundles could span the

network on their own, and so the only conduction path available contains m-s junctions highlighted in pink. If these key m-s junctions are gated, either via localised gating or through gating of the entire network area, then the current through the network as a whole will be dominated by the gate-dependence of those key junctions.

Conduction paths through high-density networks

The concept of topology enabled dominance of the network conduction by key m-s junctions can also be applied to explain the absence of any response to localised gating and the low on-off ratios when globally gated in systems with high network density.

Conduction through a network with distributed current paths as shown in Figure 5.5 (b) would not be significantly affected by partial local gating, as there would likely be conduction paths that do not fall within the gated region. One might expect a total spanning local gate, or a global gate would still show a large overall gate response, as all conduction paths would be in part or fully gated. However, a more dense network where there exist conduction paths that do not contain m-s junctions, will not show a significant gate response, as there exists circumventing conduction paths that bypass any significant gate-dependent junctions. The schematic representation of a dense network shown in Figure 5.6 (b) demonstrates how an increase in network density causes a lack of current paths that are forced through m-s junctions. By tracing a path from one side to the other in this diagram, a path can be found that circumvents the gate-sensitive m-s junctions highlighted in green.

5.6.2 Transfer characteristics of density varying CNT networks under localised gating

The transfer characteristics were calculated by summing the current through the simulated network as the gate voltage was varied from -10 V to 10 V . The gate voltage is varied independently for three different regions across the network area shown in Figure 5.7 (a). Each transfer curve in Figure 5.7 is comprised of 11 gate voltage points, from -10 V to 10 V in 2 V steps. At each gate voltage, the conductances of the gate-sensitive m-s junctions in the network are updated, and the current through the network is cal-

culated. All other elements in the simulation have conductances which are set to 1, as described in Section 5.4.

The entire network area was gated via a global gate shown in blue. A $12\text{ }\mu\text{m}$ wide section of the network area perpendicular to the direction of conduction is termed the total top gate as it spans the full width of the network area, and is shown in green. Another $12\text{ }\mu\text{m}$ wide section which only spans $20\text{ }\mu\text{m}$ or one-third of the network areas width is called the partial top gate and is shown in red. The total and partial top gates use the same lateral dimensions as those on the experimental devices in Chapter 4. The terms "back" and "top" to refer to the simulated gates is used for consistency of language with Chapter 4.

Figure 5.7 (b), (c), and (d) shows the transfer characteristics of devices with densities of $9.5\text{ sticks}/\mu\text{m}^2$, $10\text{ sticks}/\mu\text{m}^2$ and $11.5\text{ sticks}/\mu\text{m}^2$ respectively. The transfer curves for the gate voltage applied across the back, total top gate, and partial top gate areas as shown in Figure 5.7 (a) are shown in each of Figure 5.7 (b), (c), and (d) as blue, green, and red curves respectively.

For every gate voltage value in the transfer curves shown in Figure 5.7 the current and voltage must be recalculated after updating the conductance of the m-s junctions. This calculation involves an $n \times n$ matrix inversion for a system with n sticks as detailed in Section 5.2.1. In order to minimise the impact of performing this computationally expensive step when performing Monte Carlo sampling of many systems, the on-off ratio was calculated instead of a full transfer curve. The current was calculated at -10 V , 0 V and 10 V and the on-off ratio was calculated by taking $I_{-10\text{V}}/I_{10\text{V}}$. While the full transfer curve is an important qualitative measurement, the on-off ratio is the metric that this work used to asses the amount of switching. A higher on-off ratio indicates a higher sensitivity of the simulated device as a whole to the applied gate voltage in the region studied.

Simulated systems with densities from $8\text{ sticks}/\mu\text{m}^2$ to $12\text{ sticks}/\mu\text{m}^2$ in $0.25\text{ sticks}/\mu\text{m}^2$ increments were generated. 100 realisations of random networks at each density were simulated, for a total of 1700 random systems. The simulated yield for a given density is shown in Figure 5.7 (a) and is defined as the ratio of simulated systems that have a spanning cluster to the total number of systems generated at that density (100). The on-off ratios of each system gated using the back gate, total, and

Figure 5.7: Simulated transfer characteristics for a CNT FET schematically shown in (a) using localized gate regions corresponding to back gate (blue) total top gate (green) and partial top gate (red). Transfer curves for gate voltages swept from -10 V to 10 V and a driving voltage of 100 mV. (b) $\rho = 9.5$ sticks/ μm^2 , (c) $\rho = 10.5$ sticks/ μm^2 , and (d) $\rho = 11.5$ sticks/ μm^2 , showing back gate (blue) total top gate (green) and partial top gate (red)

partial top-gate are shown in Figure 5.8 (b), (c), and (d) respectively.

The back gate on-off ratios show a sharp transition between two distinct regions from on-off ratios $<10^{1.3}$ to on-off ratios between 10^2 and 10^4 . Systems with network densities between 10 sticks/ μm^2 and 11.5 sticks/ μm^2 are split between these high and low on-off ratio states. The transition between such states is echoed in the total and

Figure 5.8: Monte Carlo sampling of 1700 networks with density from 8 sticks/ μm^2 to 12 sticks/ μm^2 in intervals of 0.25 sticks/ μm^2 was performed. Conducting yield is shown in (a). The gate voltages used to calculate the on-off ratio are -10 V (on) and 10 V (off). On-off ratios for gating over the entire device region (b), the total top-gate region (c) and the partial top-gate (d) are shown with respect to density.

partial top gate on-off ratios in Figure 5.8 (b) and (c) respectively. The low on-off state for both top gates is $<10^{0.8}$, while the high on-off state is between 10^1 and $10^{2.5}$ and is a more indistinct transition than the back gate on-off ratios. The transition for both top gates is at lower densities than the back gate and occurs between 9.75 sticks/ μm^2 and

10.75 sticks/ μm^2 for the total top gate and 8.75 sticks/ μm^2 and 10 sticks/ μm^2 for the partial top gate. Additionally, the proportion of systems that exhibit high on-off ratios is successively lower for the total and partial top gates, with the partial top gate having high on-off ratios for <5 systems per density.

The specific examples of transfer curves shown in Figure 5.7 and then the Monte Carlo investigation of the on-off ratios of many realisations of the system shown in Figure 5.8 demonstrate that as the network density approaches the true percolation threshold, the system becomes more sensitive to both global and local gating.

We attribute the high on-off ratios for local top-gates in Figure 5.8 (d) to the local gating of key m-s junctions dominating conduction through the network as a whole due to their positioning in localised conduction paths brought about by the network topology. It should be noted that the lack of any response to partial top-gates in some realisations of low-density devices shown in Figure 5.8 (c) and (d) is due to the random position of these key conduction paths and the dominant m-s junctions within them. The positioning of these conduction paths does not affect back gating. A global gate will always gate key m-s junctions if they exist in any conduction path by definition, supported by the low variation in the back-gated on-off ratios for low network densities shown in Figure 5.8 (b). Conversely, gating an arbitrary localised region, as with the partial and total local top-gates, will only have a significant impact on the device as a whole if the key m-s junctions within the conduction path are located in that region. The reduced on-off ratios at lower network densities for all gate types shown in Figure 5.8 is attributed to the increased likelihood of parallel conduction paths which circumvent the gate-dependent m-s junctions within the network.

The simplifying assumption of only m-s junction gating contributes to the sharp transition observed, similar to the clear "phase" shift observed by Topinka et al. [31]. When the semiconducting bundles in the network are above their percolation threshold, there is a probability that a spanning cluster which contains only semiconducting bundles will exist. Any m-s junctions in such spanning clusters will, by definition, have at least one parallel conduction path without m-s junctions. These parallel paths will reduce the impact of m-s junctions on the overall gating. Incorporating the s-s' junction contribution to gating into our model would cause the split in on-off ratios to become blurred as dis-

cussed in Section 5.4.

The simulated work shown here exhibits a similarity with the on-off ratio trends with the experimental work in Chapter 4. Both show a trend towards increased on-off ratios for all gate geometries at low network densities. In both cases, all three gates show a sharp transition from low to high on-off ratios. In the simulated work this transition is much clearer, in part due to the quantity of data available from Monte Carlo sampling at each network density. Figure 5.8 shows that for a given density some networks will exhibit a high on-off ratio while others will be low, showing a distinct transition between the two. Clearly split on-off ratios are not apparent in the experimental data shown in Figure 4.8. The data that is shown does not conclusively rule out such a split population, as the low number of data points at low densities precludes examining this random variation. Even with significantly more experimental results at low densities, this transition may not be as sharp as the simulated results.

The assumption of m-s gate sensitivity and the treatment of CNT bundles described here is used to build a simple model of a CNT network system below the density where metallic shorts dominate the conduction and gating [5, 11]. The network topology must be such that it does not contain conduction paths that would allow circumvention of gate-sensitive m-s junctions. The network density must be above the percolation threshold, while the density of both semiconducting and metallic CNTs individually are below their respective percolation thresholds. Such a network density will ensure that any conduction pathways must contain m-s junctions, as neither metallic or semiconducting sticks can span the network individually.

5.7 Conclusion

This chapter presents a network CNT FET simulation, which was used to investigate local gating of CNT networks with varying density. Only the m-s junctions in the simulation were defined to be gate-dependent in order to compare the effect of dominant m-s junctions with the experimental results in Chapter 4. CNT network systems were investigated by Monte Carlo analysis of 60 μm square network areas containing up to 70000 sticks, each representing a single CNT or CNT bundle. The treatment of m-s junctions

here builds from work in Topinka et al. [31] where they consider m-s junctions as conduction blocking elements due to the Schottky barriers that are known to form [68].

The physical characteristics of the simulated networks were used to determine the nature of the transition from an unconnected network to a connected network. The percolation threshold was numerically calculated to be (8.670 ± 0.125) sticks/ μm^2 for $60 \mu\text{m}$ square systems with sticks of length $L = (0.66 \pm 0.44) \mu\text{m}$ and a metallic percentage of 13.5%. The corresponding metallic stick and semiconducting stick percolation thresholds were determined to be (65.6 ± 0.9) sticks/ μm^2 and (10.0 ± 0.1) sticks/ μm^2 respectively. Close to the overall percolation threshold, the maximum size of connected clusters of sticks was shown to undergo a sharp transition from <20% of the total sticks in the network to >80% consistent with percolation theory [121].

Simulated networks with densities from 8 sticks/ μm^2 to 12 sticks/ μm^2 were locally and globally gated. The current through the network was calculated while the gate voltage was varied to produce transfer curves for the simulated system. These were shown to be qualitatively similar to the local and global gate responses observed in the CNT FET devices measured in Chapter 4. Transfer characteristics for localised gating demonstrated high on-off ratios for the networks closest to the percolation threshold and dropped off sharply for network densities above 10 sticks/ μm^2 . We attribute the observed reduction in on-off ratios to the dominance of m-s junctions being obscured by network topology, not metallic shorts as is prevalently stated in the literature [5, 26, 32].

We argue that these m-s junctions only dominate the overall conduction when the network topology is such that the current through the network as a whole is forced to pass through them. The current was shown to be restricted to very localised conduction paths in low-density networks by comparing the current density calculated for networks with 9.5 sticks/ μm^2 and 11.5 sticks/ μm^2 . 9.5 sticks/ μm^2 is below the percolation threshold for purely semiconducting sticks. Thus any conduction path across the network must contain m-s junctions. This suggests that for networks with a density below the percolation threshold for purely semiconducting spanning paths, the highly localised conduction paths containing m-s junctions allow local gating of the network with high on-off ratios.

We show the trend towards high on-off ratios at low network densities to be qualita-

tively similar to that seen in the experimentally produced CNT FETs in Chapter 4 for all gate geometries. The simulation used here assumed that only the m-s junctions were gate-dependent, and set all other conducting junctions to have no gate-dependence. This assumption was based on literature work on the gate-dependence of m-s CNT junctions and their dominance of the conduction within CNT network systems [13–15]. The agreement between simulation and experiment supports the assertion of m-s junction dominated gating in network CNT FET devices.

Chapter 6

Fundamental concepts and current research on atomic switch networks

With the end of the reign of Moore's law [1], we must look beyond the improvement of computers by incremental size and speed increases to existing CMOS architecture. Alternative computing paradigms such as biologically-inspired architectures offer huge improvements in computational effectiveness, especially at tasks where conventional transistor-based computing architectures struggle. This work focuses on systems of nanomaterials with complex connectivity and nanoscale atomic switches that act as artificial synaptic elements. The research on atomic switches is presented, beginning with their discovery as the first physically realised memristive system. The properties of memristors are described, and the work on single atomic switches showing their memristive characteristics as well as establishing their neuronal traits is detailed.

Atomic switch networks (ASNs) implement the memristive characteristic of atomic switches in a complex network, which has been shown to be suitable for biologically-inspired computing. The work of the Gimzewski group at UCLA Sillin et al. [6], Sillin et al. [8], Demis et al. [16], Avizienis et al. [17], Demis et al. [22], Scharnhorst et al. [141], Scharnhorst et al. [159], Aguilera et al. [160], Sandouk, Gimzewski, and Stieg [161], Avizienis et al. [162], and Stieg et al. [163, 164] on Ag_2S ASN systems is presented as a starting point for the work done on similar systems in Chapters 7 and 8. The memristive properties of the atomic switch networks lead to internal dynamics that have been shown to be charac-

teristic of self-organised criticality, which has been leveraged in the application of ASN to computing applications.

Recent work in the literature on the application of ASN systems to reservoir computing (RC) is presented. RC operates by selecting a linear combination of complex outputs of a system to reproduce a desired output function. Self-organised criticality is a state of the system where switching events do not have a characteristic size or time scale, leading to a wide range of complex output. RC and the concept of self-organised criticality (SOC) are both described as general concepts and with respect to ASN systems. In ASN systems the complex output is attributed to the nature of the dynamics characteristic of SOC. SOC is characterised in our devices by power-law distributions of the network switching dynamics which are assessed by measuring how an input signal varies across the network area. Principal component analysis (PCA) is used as a novel analysis technique on ASN systems in Chapter 8 to characterise the multiple voltage signals measured. The details of the PCA process and potential applications are described.

6.1 Importance of biologically-inspired network devices

Neural networks as computing tools already see widespread use in modern software and hardware development to solve increasingly complex computational tasks. The IBM True North chip uses 5.4 billion transistors designed from the hardware level up to simulate 1 million neurons and 256 million programmable synapses on a 2 inch chip [165]. True North represents the state of the art in hardware-based neural simulation on transistor architectures and has a 5000:1 ratio of components to simulated neurons. In principle, artificial synaptic systems fabricated from nanomaterials that exhibit neuronal characteristics inherently could be used to realise size-competitive systems with a 1:1 ratio of components to neurons.

Synaptic electronics is the study of electronic systems with electrical characteristics similar to the synapses and neurons in the brain. Nanoscale synaptic systems benefit from the low size and novel characteristics of nanomaterials and biologically-inspired complex structure, leading to potential value in computation and furthering the understanding of neuronal systems [166]. In this work, networks composed of

nanoscale atomic switches were investigated that showed short- and long-term memory effects similar to biological synapses [7], as well as the complex dynamics necessary for biologically-inspired computation [164].

Biologically-inspired systems are of interest as they circumvent one of the inherent limitations of the Von Neuman architecture of computers that are in use today. The Von Neuman bottleneck arises from the separation of memory and processing elements in modern computer architectures, which necessitates the transfer of information between the two for any process [167]. The inherently sequential nature of information flow in such a system means that this transfer will always be a rate-limiting factor. In the brain, processing and memory are co-located in the same operating elements. Having all neurons capable of contributing to both memory and processing circumvents the need for an explicit transfer of information via limited channels between separate regions.

The potential for a system with integrated memory and processing can be realised in inorganic hardware by taking individual elements such as atomic switches that have inherent memory traits [7], and connecting them in an interconnected fashion inspired by the connectivity in biological neuronal systems [164]. Useful computation has been shown to be possible in literature where such an artificial synaptic system has been used as the reservoir in an RC system to achieve logic function and signal construction [22, 141].

The fabrication of ASN device platforms is detailed in Chapter 7 and their electrical properties investigated in Chapter 8 by applying switching event analysis and PCA data processing as a novel analysis method for an artificial synaptic system, drawing parallels with complex signal analysis and biological neuronal systems [19, 168, 169].

6.2 Atomic switches as memristive devices

The nature of memristors and memristive systems are described from first principles to provide a background for the class of electrical elements that atomic switches most closely resemble. Existing research on atomic switches is presented, detailing how their physical mechanism gives rise to memristive behaviour and demonstrating their similarity to biological neuronal systems.

6.2.1 Memristors and memristive systems

The memristor is a two-terminal electronic device with memory characteristics. It is the fourth passive circuit element in addition to the three more commonly known fundamental elements; the resistor, the capacitor and the inductor. First postulated by Chua [170] in 1971, he reasoned that there should be a fourth passive element from symmetry arguments based on the six relationships between the four fundamental circuit properties; current I , voltage V , charge q , and magnet flux ϕ . A depiction of the equations linking these four variables is shown in Figure 6.1. As with the other circuit components, the

Figure 6.1: Diagram showing the six equations which link the four fundamental circuit variables; current I , voltage V , charge q , and magnet flux ϕ . The four fundamental passive circuit components are shown alongside their governing equations. Reproduced from Strukov et al. [171]

memristance M can vary with the independent variable in its linking equation, shown in Figure 6.1, to give the defining equations for a memristor:

$$V = M(q)I \quad (6.1)$$

$$M(q) = \frac{d\phi}{dq} \quad (6.2)$$

The term memristor derives from the fact that $M(q)$ is inherently dependent on the history of the current through the device as $q = \int I dt$, introducing a concept of memory to the device [170].

More broadly the concept of a memristor has been extended by Chua and Kang [172] to a class of memristive systems by generalising Equations 6.1 and 6.2 to be governed by a state variable k to be:

$$V = M(I, k, t)I \quad (6.3)$$

$$\frac{dk}{dt} = f(I, k, t) \quad (6.4)$$

where M and f can be any explicit functions of time. From Equations 6.1 and 6.3 it can be seen that for zero voltage drop across the memristor, the current through the memristor is zero. The memristor is thus a passive dissipative circuit element similar to a resistor where the resistance depends on the current history through the device.

The first physical system to act as a memristor was a thin film of TiO_x reported in 2008 by Strukov et al. [171]. They treated their system as a semiconductor of thickness D between two electrodes where a region of highly doped semiconductor extends across the semiconductor by a distance w . The resistance of the system can thus be modelled as two resistors, R_{on} corresponding to the highly doped region, and R_{off} the low resistance region with low doping concentration:

$$V(t) = \left[R_{on} \frac{w(t)}{D} + R_{off} \left(1 - \frac{w(t)}{D} \right) \right] I(t) \quad (6.5)$$

where the extent of the highly doped region $w(t)$ changes with the charge flow through the system due to the ionic drift of the charged dopants. They take the case of an ohmic conductor and a simple ionic conductor with ionic mobility μ_v where:

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{on}}{D} I(t) \quad (6.6)$$

$$w(t) = \mu_v \frac{R_{on}}{D} q(t) \quad (6.7)$$

Given $I = \frac{dq}{dt}$ and combining Equations 6.5 and 6.7 and simplifying for the case where $R_{off} \gg R_{on}$:

$$M(q) = R_{off} \left[1 - \frac{\mu_v R_{on}}{D^2} q(t) \right] \quad (6.8)$$

Equations 6.5 and 6.6 satisfy the general memristive equation postulated by Chua [170] shown in Equations 6.3 and 6.4. Strukov et al. [171] highlights the importance of considering the limits for this system. Equation 6.7 is only defined for $w \in [0, D]$, which corresponds to the boundary between the low and highly doped regions being restricted to the total extent of the semiconductor D .

Because of the inherent size limitation on memristive behaviour due to the D^2 term in Equation 6.8, there has been significant interest in networks of memristors where the properties of a memristive device could be realised with higher conductances due to many memristive elements [17]. In Chapter 8, atomic switches which have been shown to act as charge controlled memristors [173–175], are investigated in ASN electronic device platforms.

6.2.2 Single atomic switch devices in the literature

Atomic switches are metal-insulator-metal devices that show memristive conduction and switching behaviour due to atomic-scale movement within the insulating layer. The general composition is of an active metal electrode such as silver or copper, with an insulating layer of an ionic conductor such as Ag_2S , CuS , or Ta_2O_5 and a final metal electrode. Switching and memristive characteristics are due to the migration of metal ions through the ionic conductor and reduction of the active metal to form a filament that grows to bridge the insulating gap [176, 177]. This work focuses on devices that use silver active metal electrodes and Ag_2S provides the active medium for ion movement due to the significant body of research that exists on the physical and electrical mechanisms of Ag_2S atomic switch operation [7, 173–182].

The most comprehensive work on the mechanism of Ag_2S atomic switches was performed by Xu et al. [179] in 2010, by observing the operation of a $\text{Ag}-\text{Ag}_2\text{S}$ atomic switch during voltage-driven switching using real-time HRTEM to investigate the physical processes involved. They observe four distinct physical stages under voltage bias. These are a phase transition in the Ag_2S , growth of a silver filament across the junction, connection of the silver filament, and finally subsequent dissolution of the filament after removal of bias [179]. Figure 6.2 shows the evolution of a $\text{Ag}-\text{Ag}_2\text{S}-\text{Ag}$ atomic switch junction un-

der bias to illustrate the key physical mechanisms that describe the electrical behaviour of a single atomic switch. The figure is not to scale but is instead meant to indicate the action of critical features of the switch on the atomic level [7, 175, 181, 183]. Figure 6.2 (a)

Figure 6.2: A single Ag-Ag₂S-Ag junction is shown not to scale. (a) phase change from α -Ag₂S to β -Ag₂S in the channel is induced by voltage across the junction. (b) migration of Ag^+ ions through the β -Ag₂S and reduction of Ag^+ at the cathode to silver metal causes a silver filament to begin to grow across the junction. (c) complete filament formation due to reduction of a bridging silver atom. (d) subsequent removal of bias causes thermodynamic drive towards the dissolution of the filament.

shows the phase change of the Ag₂S in the junction from the argentite (α) phase to the acanthite (β) phase along a channel within the junction. Acanthite has a higher conductivity and is a superior ionic conductor, increasing the conduction of the channel and facilitating the migration of Ag^+ ions towards the cathode [179]. Acanthite is stable only above 178 °C. It is the presence of bias that reduces the phase transition temperature and thus allows for stable channels of acanthite to exist within the junction [179]. Reduction of the Ag^+ ions migrating towards the cathode occurs along the acanthite channel where the Ag^+ ions are reduced to metallic silver at the β -Ag₂S - silver interface, resulting in the growth of a silver filament across the junction as shown in Figure 6.2 (b). The

conductance increases gradually during the growth of the filament across the junction as the tunnelling distance for an electron between the metallic filament and the anode decreases [179]. Figure 6.2 (c) shows the completion of the silver filament with the reduction of a single atom of silver, hence the term atomic switch, which is accompanied by a sharp increase in conduction across the junction [175, 179, 181]. With the applied bias subsequently removed the filament dissolves, and the channel reverts to argentite as shown in Figure 6.2 (d).

6.2.3 Junction symmetry and off switching mechanism

The only point in the above mechanism that is not conclusively agreed upon in the literature regards the off-switching mechanism shown in Figure 6.2 (d). The literature agrees that off switching is due to the dissolution of the metal filament. However, whether that filament is dissolved by an active process driven by a reversed voltage across the device, or whether it is due to an equilibrium process is inconclusive. The literature on single atomic switch devices is primarily focused on asymmetric junctions of the type $\text{Ag}-\text{Ag}_2\text{S}-\text{X}$ where X is some inert electrode such as platinum. Such single asymmetric junctions studied in the literature have attributed voltage-driven off-switching as the dominant off-switching mechanism [7, 174, 175, 177–179, 181], with some work stating that an equilibrium process contributes to the dissolution [7, 184]. Joule heating causing oxidation of the metal filament, voltage-driven ionisation of the filament leading to oxidation, and filament dissolution due to Ag^+ ion concentration gradients are described as the primary mechanisms of voltage-driven off-switching in such asymmetric junctions [179, 180, 182]. Ohno et al. [7] and Xu and Wang [184] both discuss equilibrium-driven off switching, where the filament dissolves back into the Ag_2S junction on the removal of the voltage that was driving the filament growth.

In the literature on Ag_2S atomic switch networks, the junctions that form have silver metal on both sides of the Ag_2S , forming a symmetric junction [164]. This is in contrast to the asymmetric single junctions studied elsewhere in the literature where one side of the junction is silver metal, and the other side is some inert metal such as tungsten or platinum [7, 174, 175, 177–179, 181]. Despite this difference in junction symmetry, off-switching

has been described as voltage-driven in earlier work by the Gimzewski group at UCLA on Ag–Ag₂S–Ag ASN devices [6, 8, 17, 164]. However, there is also clear evidence contradicting these conclusions in the same work. These include unstable switching under DC bias and resistive spikes in the IV characteristics of network CNT devices [17, 164]. These effects provide evidence for off-switching of the atomic switches within the network while the driving voltage remains positive, indicating that the off-switching mechanism is not reverse voltage-dependent. Recent work from the Gimzewski group by Demis et al. [22] has described the removal of the applied voltage and the subsequent relaxation of the junctions in the network as the dominant off-switching mechanism. They do not link this explanation to the symmetry of the component junctions within the network or reference the previously stated voltage-driven mechanism from their group. This suggests a

Although it is not explicitly addressed, it is my view that all of the work on silver ASN systems here and in the literature [6, 8, 16, 17, 22, 141, 159, 160, 163, 164] is on symmetric Ag–Ag₂S–Ag junctions. In such symmetric junctions, the notion of reverse voltage is not relevant on a junction level, as there is a possibility of filament growth from either silver electrode. The electrodes at each side of the Ag₂S junctions that comprise the ASNs that were fabricated here are formed between adjacent silver nanowires in the network, and should not be confused with the gold contact electrodes that have been used to provide contact to the network as a whole for electrical measurement. Gubicza et al. [173] studied the asymmetry in Ag–Ag₂S–Ag junctions by producing numerical simulations of morphologically asymmetric junctions. The resulting hysteresis that they observed in a single Ag–Ag₂S–Ag junction was explained by electric field asymmetry due to the filament growth. Their study did not incorporate the equilibrium effects into their discussion, and thus is useful as an examination of a particular aspect of the switching mechanism rather than a comprehensive picture of the symmetry within a junction.

We follow the later work of the Gimzewski group [22], and assume equilibrium driven off-switching, given the symmetric junctions present in the network. This is supported by the work of Ohno et al. [7] showing time dependant off-switching consistent with an equilibrium process. While the volatile nature of equilibrium driven off-switching in Ag₂S junction ASNs precludes its use in stable memory or robust switching systems [6, 159,

163], the variation in conductance state for a given input that it enables is essential for the kind of internal dynamics that are necessary for reservoir computing as described in Section 6.3.1 [22, 141]. To better understand to what extent the properties of the Ag₂S atomic switches that comprise the ASN are observed in the overall device function, and what properties are emergent due to the complex connectivity within the network of atomic switches, I examine the literature on the nature of the junctions that were investigated.

Artificial synaptic behaviour of an Ag₂S atomic switch

In Figure 6.3 Ohno et al. [7] show the short- and long-term memory of a single asymmetric Pt–Ag₂S–Ag atomic switch acting as an artificial synapse analogous to a biological synapse. They showed in Figure 6.3 (a) that after a certain number of infrequent input voltage pulses the system would begin to respond to the pulses with an increase in conductance followed by decay back to its original conductance. They have termed this a long-term memory effect due to its analog in biological synapses, and the observed rapid decay back to its original conductance. Figure 6.3 (b) shows more frequent pulses causing a gradual increase in conductance leading to a stable high conductance state which they have called a long-term memory effect due to its stability after the pulses have stopped. They attribute short- and long-term memory effects to the change in conductance of the atomic switch due to partial and complete filament formation respectively, and show that changing the voltage (and charge flow) history of the atomic switch leads to rapidly decaying or more stable filament formation [7]. They link the behaviour to short and long term memory processes in biological synapses [185]

6.3 Ag₂S atomic switch networks in the literature

In this section, the body of literature dealing with the characteristics and mechanisms of individual atomic switches is described with a focus on systems using Ag₂S switches. Ag₂S ASN devices in the literature are then described, highlighting their importance for application and further research.

Figure 6.3: Change in conductance of an inorganic synapse fabricated from a gap type Ag–Ag₂S atomic switch are reproduced from Ohno et al. [7]. 0.5 s 80 mV pulses were applied with intervals of 20 s (a) and 2 s (b). The conductance of the artificial synapse with a single atomic contact is the quantum conductance $G_0 = 77.5\text{ }\mu\text{S}$.

In addition to being a suitable candidate for a physically realized memristive device [173–175], atomic switches show features that make them attractive candidates for use in hardware-based biologically-inspired computing [7, 174, 175]. Short- and long-term memory effects which correlate well with similar effects in biological systems [3] make them particularly suitable for the active elements in artificial synaptic systems inspired by neuronal networks.

ASN systems that have been studied in the literature were primarily fabricated through a combination of bottom-up growth of silver networks via electroless deposition of silver from solution onto copper seed sites [162], and photolithography to fabricate arrays of contacting electrodes across the network area [16]. The networks were then sulfurised to produce a complexly connected network of memristive Ag₂S junctions, which have demonstrated criticality and memory analogous to biological systems [8]. I discuss fabrication methods the silver ASN devices described in detail in Chapter 7.

Ag–Ag₂S–Ag based ASN electrical devices have been primarily studied by the Gimzewski group at UCLA since 2012 due to their potential for application in biologically-inspired computation [6, 8, 16, 17, 22, 141, 159, 160, 162–164]. Figure 6.4 shows an example of the ASN systems that the Gimzewski group uses in their work [22]. The system was fab-

ricated by electroless deposition of silver onto copper seed sites to produce the network of silver nanowires shown in Figure 6.4 (a). These networks were then sulfurised to produce the atomic switches between adjacent wires. Their early work focused on the key

Figure 6.4: An example of dynamic response of an Ag_2S ASN system is reproduced from Demis et al. [16]. The active region of the ASN is shown in (a) with 16 contacts. The input signal (b) is used to drive the ASN system shown in (a), and the voltage response is recorded and displayed in (c). The voltage responses are normalized for visual clarity.

characteristics of ASN systems. These include demonstrating memory features in networks consistent with the single atomic switches that make up the network as described in Section 6.2.3 [7]. Additionally, the network shows features that do not exist in single atomic switches, but which arise due to the complex connections between switches in the network. The most significant of these is non-regular switching events in the network under regular periodic or DC bias [6, 8, 17, 162, 164], which we will call dynamic switching. An example of the current response due to dynamic switching in the network is shown in Figure 6.4 (b) and (c), showing variation in the output signal across the network area. They attribute the specific characteristics of the dynamic output to self-organized criticality[22, 164], the details of which are examined in detail in Section 6.4.1. Their recent work has focused on proof of concept application of such dynamic response in ASN devices to implement reservoir computing systems showing logic and signal generation [16, 22, 141, 159, 160, 163].

6.3.1 Reservoir computing using atomic switch networks

Reservoir computing (RC) is defined by some reservoir which produces a higher dimensional representation of an input signal (The process by which this is achieved is not important to the computational application, leading to it being referred to as "black box computation" [8]). A linear combination of the high dimension outputs is used to produce any desired function on the inputs, including nonlinear functions [186, 187]. Provided that you have such a black box reservoir, approximating a desired output function is achieved by training a linear combination of the outputs. Any nonlinearity in the desired function is made possible by the high dimensional outputs of the reservoir. The training of the linear combination is achieved by any numerical method on linear systems eg. gradient descent. A pictographic representation of an RC system is shown in Figure 6.5 (a), where a time-varying signal is fed into a fixed connectivity network, with arbitrary components. The readout layer is then shown as a linear combination of outputs to produce some arbitrary waveform. The use of ASN devices as the reservoir in a physical RC system relies on the combination of complex network structure and dynamic switching, which could be used to replicate arbitrary desired functions. Key to using the output signals from an ASN system is some non-linear transform of the input signal within the reservoir. Without this, the desired function will be restricted to only those which are linear combinations of the inputs.

In one of their first papers, the Gimzewski group points to the suitability of Ag_2S ASN devices as potential physical candidates for RC [164]. They have shown that the dynamic switching at the junctions, memory characteristics of the network, and its complex topology result in varying dynamic signal outputs across the network [17, 164]. They have claimed that the nature of those dynamic signals makes them suitable candidates for RC [22]. Most recently they have investigated using ASN devices as reservoirs to achieve logic functionality from binary inputs [141] and waveform construction from sinusoidal input [22].

Demis et al. [22] used a 64 channel ASN device platform driven with an 11 Hz sinusoidal input to achieve waveform generation. They achieved $\sim 90\%$ accuracy in producing a cosine, triangular, and sawtooth waveform and 73% accuracy producing a square waveform. The linear readout layer was trained using standard linear optimisation on

1 min of training data followed by 1 min of testing data to verify the results. The RC results from Demis et al. [22] are reproduced in Figure 6.5 (b) showing the target (red) and produced (blue) waveforms along with their calculated accuracy. The ability to produce different waveforms was dependent on the network's ability to produce sufficient higher harmonics, a property shown in previous work to be due to non-linear transformation on the inputs [17]. The use of ASN based RC systems to replicate the logic functions

Figure 6.5: (a) schematic of an RC system, where a time-varying input is fed into the closed reservoir system composed of complex but fixed interconnected elements. The linear readout layer is then trained to achieve a desired arbitrary output. The results of using an Ag_2S ASN as the reservoir in such a system are reproduced from Demis et al. [22] showing their systems ability to produce a (i) cosine, (ii) triangular, (iii) sawtooth, and (iv) square waveform with the target waveform (red) and achieved RC output (blue) shown.

AND, OR, NAND and XOR as target functions were investigated in Scharnhorst et al. [141] using two terminals for inputs and one channel for output from a 16 channel Ag_2S ASN device. The AND, OR and NAND functions are all linearly separable, ie they can all be reconstructed by a linear combination of their inputs. The XOR function is not, and so would require some nonlinear combination of the inputs to reconstruct it. The power of an ideal RC system is that the reservoir produces arbitrarily many high dimensional outputs that can be combined to any function, thus the XOR function is a key factor in establishing the success of using the ASN as a successful reservoir.

They found that after training on 1000 input combinations the linear readout layer was able to reproduce the linearly separable functions AND, OR, and NAND with 95%

confidence for driving voltages of 0.01 V, but were unable to produce the linearly inseparable XOR operator that performed better than random. For higher driving voltages of 3 V they were able to achieve XOR functionality above random, but with a maximum confidence of 40%, i.e. the RC device was able to perform better than random 40% of the time. Additionally, the reliability in the performance of the linearly separable functions suffered at the higher driving voltage.

A linearly separable function by definition can be perfectly reproduced by the linear readout layer if it has access to the original inputs directly. Thus the ability of the ASN to produce linearly separable functions at low voltages is unsurprising. The low driving voltages used were unlikely to cause switching within the network, and so would exhibit little non-linearity or dynamics that would transform the input signals significantly. The non-linearly separable XOR function was only shown to be producible with 3 V input signals where switching and non-linearity within the network would be observed.

In the case of both Demis et al. [22] and Scharnhorst et al. [141] they used the ASN to produce non-linear and dynamic output signals to approximate the high dimensional outputs of an RC reservoir. Accessing those transformed outputs via the voltages at different regions of the network proves a significant barrier to further advancement. Chapter 8 and literature research have shown conclusive evidence for the self-organised criticality of the ASN systems, and non-linear response to input signals [8, 16, 164]. Thus while the Gimzewski group has taken the tact of demonstrating proof of concept RC capability with Ag₂S ASN devices, this work focuses on expanding analysis of both the spatial and temporal dynamics of the system.

6.4 Key concepts in atomic switch network analysis

In order to tackle the analysis of ASN systems, a number of fundamental concepts must be well understood. One of the key traits of ASN systems that makes them suitable for RC application is the dynamics of the system due to the self-organised criticality that they have been shown to exhibit [164]. The concept of self-organised criticality is examined, with reference to the importance of systems that exhibit it, in order to motivate its importance as a model when considering synaptic network systems. The multiple output

signals from an ASN device that have been used for RC application in the literature [16, 141] require significant post-measurement analysis. A constructed example using principal component analysis to reduce the dimensionality of a dataset is described to cement the key characteristics of the process and highlight its potential for analysing multichannel data from ASN systems as shown in Chapter 8.

6.4.1 Self organized criticality

Self organized criticality, often shortened to criticality in the literature, is a key characteristic of the complexity of the internal dynamics of ASN systems [6, 8, 16, 17, 22, 141, 159, 160, 163, 164]. Self-organised criticality is defined as a system which has semistable states that it settles to, but which is unstable with respect to arbitrary perturbations. When such a semistable state is disturbed, the system settles after some time to some other semistable state. Such critical systems are characterised by the lack of characteristic length and time scales of perturbations, resulting in power-law distributions of the perturbation. The result of which is a power-law distribution of duration and size with a so-called 'critical exponent' $\alpha = 1.5$ [21].

In order to provide an intuitive model of a system with self-organised criticality, we examine the classic example given by Bak, Tang, and Wiesenfeld [21] of a "sandpile" which is disturbed by the addition of further "sand". The term "sand" is used loosely in this work, and the specifics of its behaviour is defined for a one- and two-dimensional "sandpile" respectively.

Consider a one-dimensional system with N bins where sand can only leave the system via the right-hand side. When the height difference (slope) between two adjacent bins is greater than a critical value δz_c , the higher bin 'topples' spilling one unit of sand to the lower level. When a bin has a slope equal to the critical value δz_c , we call that bin minimally stable. In this system, perturbations take the form of sand added to a single bin. The state of the sandpile is stable with respect to a perturbation if the addition of sand to a bin does not cause that bin to topple, and unstable if it does.

Sand is added at random to this system, corresponding to random perturbations. If it is added to a bin with slope $< \delta z_c$, it is added to the bin increasing the surrounding

slope. The system is considered stable with respect to this kind of perturbation. If the sand is added to a minimally stable bin with slope $= \delta z_c$ then that bin will topple thus increasing the slope of the adjacent bins, and toppling them in turn if they were also minimally stable. If we keep adding sand at random, all of the bins will eventually come to have a slope equal to the critical value δz_c . Since sand can only leave the system on the right, a critical slope will exist from the left to the right of the systems. Such a system state is now the least stable of all of the states of this system, in that sand added to *any* point will cause that point to be above the critical slope, thus causing it to topple to the adjacent bin. That unit will slide down the slope and exit on the right resulting in the same critical slope across the whole system. Importantly, if sand is added at random to this system, the duration and spatial extent of the resulting sand flow will only depend on where in the slope the sand is added as it always flows down the slope and out the right side of the system. For random perturbations, the number of toppling piles until the sand exits on the right will be random with a $1/\text{length}$ spectrum of the length of perturbation [21]. A system where all of the bins are minimally stable is thus stable with respect to the addition of sand (small perturbation) as it will return to that state after the perturbation. We call this state where all bins are minimally stable a minimally stable system state.

To extend this idea to a system that exhibits self-organised criticality, we now consider a similarly constructed system but in two dimensions. There are two key differences in construction, a bin will now topple when its height z_{ij} is greater than some critical value z_c , and when it topples, it will spill sand to each of its 4 directly adjacent bins. This extension of the 1D sandpile model to two dimensions could naively be expected to reach a minimally stable state with similar characteristics as the one-dimensional case. To demonstrate that this is not the case, consider the explicit model which is a slight modification of Bak, Tang, and Wiesenfeld [21], but shows the same dynamics while being more conceptually relatable [188, 189].

For a two-dimensional grid of $N \times N$ bins, where if the height of sand in any bin z_{ij} is greater than some critical value z_c then the bin 'topples' spilling sand into the directly adjacent bins leading to the following rules:

$$\begin{aligned} z_{i,j} &\rightarrow z_{i,j} - 4 \\ z_{i+0,j\pm 1}, z_{i\pm 1,j+0} &\rightarrow z_{i+0,j\pm 1} + 1, z_{i\pm 1,j+0} + 1 \end{aligned} \quad (6.9)$$

The intuitive expectation is that by adding sand to the system at random, the system will eventually evolve to a minimally stable state similar to the one-dimensional system. However, an examination of Equation 6.9 will show that this is not the case.

Consider the stable system state where $z_{ij} = z_c \forall i, j$, which is analogous to the single critical slope in the 1D example. When sand is added at random to any site, that site will topple, and sand will transfer to each of its neighbours causing them to topple on their neighbours in an amplifying fashion. Since each site is connected to multiple minimally stable sites this system will not settle to the same state after perturbation, and so is not a minimally stable system state. Instead, a perturbation to this stable state propagates through the entire system, settling into some minimally stable states and some less than minimally stable states where $z_{ij} < z_c$. A state where all bins are minimally stable in two dimensions is thus unstable when perturbed, as it will not settle back to the same state after perturbation. This contrasts with its one-dimensional analogue and does not have the same trivial dynamics.

After perturbation from the minimally stable state, the two-dimensional system will become stable precisely at the point when groups of minimally stable bins have been broken down to the level where a perturbation cannot extend over infinite distance [21]. Imagine adding a single grain to any site after the system has settled from the disruption described above. Such a site might not be a more-than-minimally stable site $z_{ij} < z_c$ and thus impede the motion of the perturbation, or it could be a part of a large group of minimally stable sites through which the perturbation will propagate. When the system reaches such a stable state, it is called self-organised critical (SOC) state and will have no length scale or time scale that characterises perturbations [21].

Self-organise criticality in ASN systems

Instead of a sand pile which collapses at a certain height, consider the filament length which grows until it forms across the junction. When the filament connects across the

junction, the voltage across it decreases, causing it to dissolve as described in Section 6.2.2. When the voltage across a junction decreases those junctions connected to it will experience an increased voltage, making them more likely to switch on. The nature of the connections between that junction and the surrounding network will determine how the change in that junction affects the voltage across those junctions connected to it. In a similar manner to the collapsing sandpile which affects those sites around it that are also in a critical state, a switching junction will thus affect switching in those connected to it if they are minimally stable, or near to switching.

ASN devices in the literature have been shown to exhibit dynamic activity characteristic of self-organised criticality by showing power-law scaling of the frequency response of the system [6, 8, 16, 17, 22, 141, 159, 160], with the exponent of the power-law equal to 1.5 [21]. The so-called critical exponent $\alpha = -1.5$ of the power-law scaling is due to the lack of both characteristic time and length scales within the system [21]. In the example of the sandpile described in Section 6.4.1, the power-law scaling is due to a perturbation causing toppling across a region of connected minimally stable sand piles, where the size of the minimally stable region determines the size and duration of the perturbation. Since these regions can be of any size (limited by the smallest unit in the system and the size of the system), there is no characteristic scale dictating how a perturbation propagates through them. For a network of memristive junctions, the number of junctions that will subsequently switch in response to an initial switching event in a single junction will dictate the size of the change in conductance ΔG observed across the whole device. The size of switching events measured across an ASN can thus be directly related to the number of switches involved in the event.

In the literature on Ag_2S ASN devices, metastable state duration during pulses [163, 164] and power spectral density of the noise response to DC bias [8, 22, 159] are used to demonstrate SOC in the system. Although this is shown to do so [21, 190], the treatment of ASN in a more biological fashion leverages the extensive research on the link between criticality and functionality in similar biological systems, as well as providing a simple metric for criticality. The size and time between events have been used to characterise SOC in systems that exhibit SOC such as neuronal networks [18], single neurons, and earthquakes [168]. SOC has been linked to memory effects within such systems [168],

and their dynamics have been shown to affect the information transmission and capacity [2]. In Section 8.2.1 I take the approach of analysing the size and time between switching events above a threshold in order to demonstrate SOC in our ASN devices.

6.4.2 Principal component analysis

PCA is a mathematical technique to recast a dataset in terms of a basis set of vectors that better encompass the variation in the dataset and remove redundancy. PCA involves taking the eigenvectors of the covariance matrix of some dataset and ordering them with respect to the magnitude of their eigenvalues. These eigenvectors represent an orthogonal basis set that encompass the maximum variance in the data in descending order. The mathematical proofs for its operation are not detailed here. However, a concise introduction can be found in Shlens [191].

Following Smith [192] an example of the application of PCA to an arbitrarily constructed two-dimensional dataset is shown in Figure 6.6, to illustrate the process and utility in dimensions which are intuitively simple. Figure 6.6 (a) shows a dataset D composed of $m = 300$ data points in two dimensions, which have been constructed from 3 Gaussian distributions. The projections of the dataset onto its basis axis $x = [1, 0]$ and $y = [0, 1]$ are obtained by taking the dot product $D \cdot x$ and $D \cdot y$ and are shown as histograms in the top and right of Figure 6.6 (a) respectively. There are two obvious peaks in each projection histogram. Thus by looking at the projection onto its basis vectors, it is difficult to identify the three distinct distributions present in the data.

Applying PCA to the dataset produces unit vectors $p_0 = [0.70, 0.71]$ and $p_1 = [0.71, -0.7]$, the direction of which are shown in Figure 6.6 (a) in red. The relative fraction of the variation in the dataset that is encompassed by p_0 and p_1 is 90% and 10% respectively. The dataset can be shown in full when it is transformed to be in terms of the new basis vectors p_0 and p_1 in Figure 6.6 (b). The transformation takes the form of a rotation, illustrated by the direction of p_0 and p_1 again shown in red. The projection onto the new basis p_0 and p_1 can again be seen as histograms in the top and left of Figure 6.6 (b) respectively. The projections onto p_0 show three distinct peaks, which encompasses the most significant feature of the original data, namely that it is comprised of points from 3

Figure 6.6: Constructed dataset of 300 points before (a) and after (b) transformation via PCA. (a) points are presented in conventional (x, y) coordinates with the projection onto the x and y axis shown as histograms on the top and right respectively. After application of PCA the principal components p_0 and p_1 are shown in red. (b) the dataset is transformed into p_0, p_1 coordinates, where p_0 and p_1 are the first two principal component vectors. Projection onto p_0 and p_1 are shown as histograms on the top and right respectively. p_0 and p_1 are again shown in red.

Gaussian distributions. Importantly, this is visually apparent from the projection onto a single dimension and is indicated by the fact that it encompasses 90% of the variation in the data.

In this example, the significant variation in a two-dimensional dataset can be extracted from its projection onto a basis vector by selecting that basis to be representative of a maximum variation in the data using PCA. Reduced dimensionality of a dataset from two to one dimension is trivial, and the 3 Gaussians that comprise the original data can be easily identified without any transformation or analysis. However, if the problem of identifying features is extended to 4 or higher dimensions the features that might be present in such data quickly become opaque. PCA can thus be applied to higher dimensional data to reduce it to one or two principal dimensions where more intuitive analysis

is possible.

The state of analysis of multichannel data from the literature on ASN devices is to interact with multichannel voltage data as current traces plotted across multiple channels [16, 22, 159], which as shown in Figure 8.15 is at best limited to arbitrarily selected and size restricted data sets. PCA has been used as a technique in neuroscience to elucidate the change in large collections of neuronal measurements when correlated to some activity or stimulus [169, 193–195]. In this work, the application of PCA to 14-dimensional voltage datasets collected from across ASN devices was explored to analyse the spatiotemporal variation in their electrical activity in Chapter 8. We will show that representations of the full 14 channels of the data prove challenging for intuitive analysis. PCA provides a mathematically sound and physically reasonable method for the analysis of the spatiotemporal dynamics, which is scalable to long time periods of feature-rich data and arbitrarily high dimension.

Chapter 7

Fabrication and measurement of atomic switch networks

In this chapter, the atomic switch network (ASN) device fabrication and electrical measurement process that was developed to measure the connectivity and dynamics of Ag_2S ASN devices are detailed. The final devices used in Chapter 8 consisted of silver nanowires fabricated as a network on top of a chip that was then sulfurised to produce Ag_2S junctions between the nanowires. Electrical measurement of the ASN device was used to characterise the dynamics of the complex system described in Chapter 6. The adaptation and optimisation of fabricating a connected network of sulfurised silver nanostructures from the literature is explained here [6, 162]. This work represents the first foray for our research group into ASN device fabrication and measurement. As such I investigated multiple fabrication options in parallel for producing silver nanowire atomic switch networks. Growth of silver nanowires directly on the device surface was explored using random and patterned seed sites in parallel with fabrication using pre-grown silver nanowires spray-coated on to the device surface. Spray coating was selected for use in this work due to the ease of rapid fabrication for prototype iteration, and lack of significant fabrication issues. The chips designed to allow electrical contact with the network are detailed, and the electrical measurement setup and protocols used for measurement are described.

7.1 Two channel test device platforms

Figure 7.1: A schematic diagram of the test device used for two channel ASN characterisation is shown. 4 electrodes were fabricated to provide redundancy of electrical connection. The electrical connection of the driving voltage V and measured current I is shown.

The fabrication and measurement procedure for producing silver nanowire-based ASN devices had to be adapted from the literature and built from scratch for this research. Two-channel test devices were designed that would allow rapid prototyping of the network fabrication using the literature available on ASN systems as a starting point [6, 162]. Two-channel devices offer a simple platform to electrically test the fabrication of the silver network and generate a proof of concept ASN device without the complication of multi-channel devices discussed later in Section 7.5. To do this, four gold contacts with a separation of 1 mm were fabricated on $\sim 1 \text{ cm}^2$ Si chips with 300 nm of SiO₂ as shown in Figure 7.1. Only two opposite electrodes were used for electrical measurements, with the remaining two being included in fabrication for redundancy in initial tests. We then adapted methods for silver network fabrication and sulfurization from literature [6, 8, 16, 17, 162–164] to achieve ASN network devices on these prototype platforms.

7.2 Spray deposition of silver nanowire networks

Demis et al. [16] investigated drop-cast silver nanowires from solution, and commented on the lack of uniformity and control over the deposition. Spray deposition of silver networks was used for the fabrication of ASN devices shown in Chapter 8, inspired by spray deposited quantum dot devices via masked spray coating [196]. This was the most rapid and consistently functional fabrication method investigated. A schematic of the spray

Figure 7.2: Spray coating of premade silver nanowires is shown diagrammatically in (a), showing the device substrate, spray gun, and the mask used to restrict the area covered. SEM images of the spray deposited nanowires are shown in (b) with a 20000x magnification shown inset.

coating setup is shown in Figure 7.2 (a), and SEM images of the resulting silver nanowire network are shown in Figure 7.2 (b). Spray coating allows the deposition of nanowires in a liquid suspension while avoiding aggregation due to the evaporation of large quantities of the suspension on the surface. The distance between the spray gun and the substrate is chosen such that much of the solvent evaporates before the suspension reaches the chip. The suspension is sprayed in short bursts to allow any remaining solvent to evaporate before more is sprayed.

A suspension of 2 mg/ml was prepared by the dilution of pregrown silver nanowires (BlueNano, SLV-NW-90) in ethanol. As specified by the manufacturer the nanowire diameters were (90 ± 20) nm with a length range from 20 μm to 60 μm . The suspension was stirred at 1000 rpm for 5 minutes followed by a 1 min sonication to ensure no aggregates were present. ~ 2 ml of the nanowire suspension was then loaded into the hopper of an

aerosol spray gun where it was sprayed onto the substrate using N₂ gas as a propellant. The substrate was affixed to a mask with a recessed alignment notch, which allowed alignment of the centre of the device with a 2 mm by 2 mm hole to restrict the region of the chip covered by the spray-coated silver nanowires. The masked substrate was held ~10 cm from the nozzle of the spray gun, and the nanowire suspension was sprayed on in short bursts of <1 s allowing any solvent remaining on the chip to visibly evaporate under the flow of nitrogen before the next burst. 20 - 30 such bursts were used until the resistance across the device was 50 Ω for two-channel devices, or 200 Ω to 1000 Ω for MEA-based devices measured via multimeter every 10 spray bursts.

7.3 Electroless deposition of silver

Spray deposition of premade silver nanowires was determined to be the most repeatable and high throughput method of fabricating silver networks, and was used in all devices that are analysed in Chapter 8. Solution-based growth of silver nanowires was tested in parallel to spray coating but was not selected for continued use in this work due to rapid successes using spray coating. Solution grown nanowires were investigated as they have been reported in the literature as a simple bottom-up fabrication process for silver network formation [6, 8, 16, 17, 22, 141, 159, 160, 162–164]. Two different copper seed sites were investigated based on their use in the literature for growing silver nanostructure networks. Copper microspheres [6, 16, 163] for their ease of solution-based fabrication and lithographically defined copper posts [8, 16, 17, 141, 159, 162, 164] for the control afforded in terms of size, shape, and spacing of the seeds.

7.3.1 Copper microsphere seed sites

Copper microsphere growth deposition followed the methods described in Sillin et al. [6]. A 2 mg/ml suspension of copper microspheres was prepared in isopropyl alcohol (IPA). A liquid well was placed over the top of each chip, consisting of a 3 mm thick section of PDMS which had a 3 mm diameter hole cut through it. This was placed on top of the chip with the hole in the center of the device producing a liquid well. 30 μ l of the

copper microsphere suspension was pipetted into the PDMS well. The bulk of the IPA from the microsphere suspension was allowed to dry at room temperature, followed by a 5 min bake on a hotplate at 70 °C. Wire growth was achieved by pipetting of 30 μl of 50 mM AgNO_3 solution into a 3 mm diameter PDMS well that was placed on the surface of the chip to contain the liquid in the device region which contained the copper seed sites. The growth was left at room temperature for 15 min.

Figure 7.3 (a) shows the dendritic growth of silver nanostructures from randomly placed copper seed sites via diffusion-limited growth (inset). The silver nanostructures grown are fractal, where the primary growth stem diameter ranges from 10 μm to 200 μm , and the minimum feature size at terminal branching is 200 nm in diameter. Dendritic sil-

Figure 7.3: (a) dendritic silver nanowires grown from copper microsphere seed sites (inset). (b) schematic of the branching growth of silver structures due to local variation in the Ag^+ concentration, reproduced from Avizienis et al. [162]

ver nanostructures are due to the localised variation in the Ag^+ ion concentrations during dendritic silver nanostructure growth as shown in Figure 7.3 (b). When the depletion of the local ions due to the nanowire growth at the tip of a nanowire outstrips the diffusion of ions to correct that depletion, so-called Mullins-Sekerka (MS) instabilities form [197]. MS instabilities take the form of periodic variation in the local ion concentration [197]. At the antinodes of these concentration waves, where there is sufficient local concentration of Ag^+ ions to cause nucleation, new growth fronts begin, which in turn begin generating local instabilities as shown in Figure 7.3 (b) [198]. Avizienis et al. [162] demonstrate this growth process for AgNO_3 solution concentration of 50 mM, which was used here.

Although the growth of dense networks of dendritic silver nanostructures as shown in Figure 7.3 (a) was achieved, there were issues with the uniformity of the resulting structures. The fabricated devices were either non-conductive or no resistance change was observed during sulfurisation when they did conduct. This was due to the observed nonuniformity on a 100 μm length scale which prevented good electrical contact and resulted in disconnected regions of very dense network structures. The disconnection prevented good electrical contact throughout the network and the very dense clumping prevented sufficient sulfurisation occurring within the clumps.

Sillin et al. [6] states only that a 20 μl drop was placed on the substrate "... allowing the Cu spheres to disperse uniformly across the region" [6]. However, the propensity of the microspheres to settle out of suspension rapidly combined with the lack of adhesion to the substrate caused significant coffee ring patterns in the microspheres as the IPA evaporated. The most successful method for achieving a uniform distribution of microspheres found was a combination of wicking of excess IPA followed by final rapid evaporation of any remaining IPA by placing the substrate on a hotplate at 70 $^{\circ}\text{C}$ for 5 min.

Microsphere concentrations from 0.2 mg/ml to 20 mg/ml were investigated to achieve the most consistent and even spread of spheres over the 3 mm diameter region of the chip defined by the PDMS well. The microsphere suspension was shaken immediately prior to each pipetting due to rapid sedimentation of the microspheres when left to sit for more than ~ 30 s. In order to minimally disturb the grown nanostructures, a majority of the remaining AgNO_3 solution was wicked away with an absorbent wipe. The device area was then successively rinsed with 30 μl of DI water four times. After final wicking of any excess DI, the chip was then placed on a hotplate at 70 $^{\circ}\text{C}$ for 5 min to ensure any excess water was evaporated.

Despite the above work towards achieving a uniform distribution of copper microspheres across the device area, non-uniform coverage and the resulting non-uniform growth of silver nanostructures hampered the use of copper microspheres in functional ASN devices. No devices that were successfully fabricated were dense enough to be electrically connected, while also showing a lack of clumping. All devices were either nonconducting or they could not be sulfurised sufficiently to cause resistance change corresponding to Ag_2S junction formation in the network.

7.3.2 Lithographically defined copper pillar seed sites

Lithographically defined copper seed sites have also been used in the literature to provide control over the size and distribution of seed sites for electroless deposition (ELD). They show greater control of the grown silver network than using solution deposited seed sites [8, 16, 17, 22, 141, 159, 162–164]. Electroless deposition is the spontaneous reduction of silver ions in solution to silver metal at copper seed sites, accompanied by the simultaneous oxidation of copper metal from the seed sites [162]. A grid of circular seed sites was fabricated using the standard lithographic process for AZ1518 detailed in Section 3.1.1 and Appendix A. Copper was then deposited using thermal evaporation to produce a 300 nm thick layer. ELD was achieved by dropping 30 μl of 50 mM AgNO_3 solution onto the seed sites as detailed in Section 7.3.1.

Variation in spacing and seed diameter was tested, the results of which are shown in Figure 7.4.

- Figure 7.4 (a) shows 10 μm diameter circular seeds with 20 μm pitch. Some dendritic nanostructures can be seen.
- Figure 7.4 (b) shows 10 μm diameter circular seeds with 30 μm pitch. Only small nanocrystals can be seen.
- Figure 7.4 (c) shows 5 μm diameter circular seeds with 10 μm pitch. Some dendritic nanostructures can be seen.
- Figure 7.4 (d) shows 5 μm diameter circular seeds with 15 μm pitch. Only small nanocrystals can be seen.

The spacing and size of copper seed sites were investigated in an attempt to reproduce the variation in silver nanostructure morphologies shown by Avizienis et al. [162]. They demonstrate that seed sites smaller than $\sim 7 \mu\text{m}$ in diameter produce unbranched silver nanowires, while those larger than $\sim 7 \mu\text{m}$ produce branched dendritic structures. Dendritic structures were shown here from those seed sites that had a pitch that was twice their diameter shown in Figure 7.4 (a) and (c), but not in those with a pitch 3 times their diameter as shown in Figure 7.4 (b) and (d), irrespective of the seed site diameter.

Figure 7.4: SEM of circular copper seed sites in a regular array are shown after ELD of silver nanostructures. (a) 10 μm diameter circular seeds with 20 μm pitch, (b) 10 μm diameter circular seeds with 30 μm pitch, (c) 5 μm diameter circular seeds with 10 μm pitch, (d) 5 μm diameter circular seeds with 15 μm pitch.

The variation of silver morphology with seed site spacing suggests that it is the fractional coverage of the area with copper seed sites that dictates the structures grown, not the seed diameter as suggested by Avizienis et al. [162].

Figure 7.4 (a) and (c) both show some growth of dendritic nanostructures. The smaller post sizes used in Figure 7.4 (c) were more sensitive to the individual variation in fabrication during their photolithographic patterning. Thus, the larger post sizes were selected for continued testing of nanowire growth for ease of repeated fabrication. A regular array of circular 10 μm diameter copper seed sites with a 20 μm pitch over the full 2 mm $\times$ 2 mm device area was selected for further ELD tests on lithographically defined seed sites. The variation in growth of silver structures across the entire 2 mm $\times$ 2 mm

device area is shown in Figure 7.5 (a). Details are shown in inset (b), (c), and (d) for a single seed site at the center of the device area, at the edge of the device area, and on top of one of the pre-deposited gold electrodes respectively. The lack of any growth on the

Figure 7.5: Silver nanostructures grown from lithographically defined 10 μm copper seed sites with a 20 μm pitch. (a) the full device shows distinct variation in growth across the 2 mm by 2 mm device area. (b) dendritic silver nanowires have grown from seeds at the center of the device area, (c) while seeds near the edge of the device area show clumped crystalline growth. (d) those seeds on the electrodes show no silver growth.

seed sites shown in Figure 7.5 (d) is due to delamination of the copper posts from the gold and was corrected in subsequent work by capping the electrodes in a solid copper layer.

It is clear that there is a gradient from the center of the device area outwards in the ap-

parent growth of nanostructures at seed sites, with the most visible growth at the center and becoming less towards the edges. Variation in the morphology of the silver nanostructures is attributed to a millimetre-scale gradient in the concentration of silver ions in solution that causes the inhomogeneity of silver structure morphology across the device area.

To further investigate the equilibrium between the growth rate and the flow of ions to the growth front, silver nanowires were grown via ELD at temperatures from 20 °C to 70 °C on 10 µm diameter circular seeds with 20 µm pitch as shown in Figure 7.6. We see dendritic growth on select sites for growth at 60 °C and widespread dendritic growth at 70 °C as shown in Figure 7.6 (e) and (f). Increasing the growth temperature increased the growth rate, resulting in faster local Ag^+ ion depletion. In growth solutions of the same concentration, and with the same concentration of Cu seed sites, a higher rate of local ion depletion would increase the likelihood of Mullins-Sekerka instabilities forming [162, 197–199] and thus dendritic growth.

Each parameter investigated in the ELD of silver using lithographically defined copper seed sites had a significant impact on the quality of the nanostructures grown. The seed size and pitch of seed sites shown in Figure 7.4, the position of the seed site across the desired network area shown in Figure 7.5, and growth temperature shown in Figure 7.6 all had a significant effect on the morphology of the silver structures grown. It is my opinion that the local ion concentration dynamics must be investigated in order to fully optimise the silver nanostructure morphology for ELD of silver on patterned copper seed sites. By changing the seed size on a grid of equal pitch, and thus the density of copper seed posts, Avizienis et al. [162] were in effect changing the local Ag^+ ion concentration available. This in turn affected the interplay between local ion depletion due to growth and replenishment due to concentration gradients.

Work by Maddah, Unsworth, and Plank [200] in our group on the growth of Zn_0 nanowires suggests that the fractional area of the seed sites is of great importance when considering crystal growth from an aqueous solution. An increased portion of the substrate that is covered in seed sites will result in an increased rate of ion removal from solution near to the surface compared with a surface with sparse seed sites. The MS instabilities that Avizienis et al. [162] identify as causing dendritic growth occur where the

Figure 7.6: 10 μm copper seed sites with 20 μm pitch after ELD growth of silver nanostructures for 10 minutes under varying growth temperature. 20 $^{\circ}\text{C}$, 30 $^{\circ}\text{C}$, 40 $^{\circ}\text{C}$, 50 $^{\circ}\text{C}$, 60 $^{\circ}\text{C}$ and 70 $^{\circ}\text{C}$ growth temperature shown in (a) - (f). Inset shows full device area, including silver growth from copper capped electrodes.

local ion depletion outstrips the ability for ions in solution to replace them. They associate the change in morphology with seed site with the size of the site. Figure 7.4 suggests that the seed site size is less important than the fractional coverage of the substrate. This is consistent with the observation in Avizienis et al. [162] where the spacing between seed sites was kept constant, and so the fractional coverage was directly proportional to seed site size.

This work is focused on developing and demonstrating the capability to fabricate and electrically measure ASN devices as proof of capability within our lab group. As such, the ability to rapidly iterate on device construction and measurement was the primary consideration. The investigation of lithographically patterned and solution deposited Cu seed sites was performed in parallel with the investigation of spray coating pre-grown silver nanowires. The spray deposition of silver nanowires was selected over lithographically defined ELD growth of silver, due to the functional networks produced with minimal fabrication optimization. Additionally, the spray deposition process has fewer fabrication steps that could disrupt a pre-deposited CNT layer in a combined CNT-ASN device.

Although on-substrate growth of nanowires was not further investigated here, literature results [16, 22, 162] and my work suggest that ELD grown silver nanowires are a viable alternate fabrication for future work. Further investigation of the seed sizes that would yield good wire growth, similar to the systematic investigation in Maddah, Unsworth, and Plank [200] using varying arrays of seed sites, could be used to optimise the growth parameters. Parameters of seed sites for growth that could be investigated include surface adhesion of Cu sites, crystallinity, and shape. An investigation of the disruption of CNT films by fabricating seed sites on top of them would also be necessary to determine whether ELD silver wire growth would be suitable for the fabrication of combined CNT-ASN devices in future work.

7.4 Sulfurisation of silver networks

After fabricating the silver network using spray deposition of premade silver nanowires as described in Section 7.2 the network was sulfurised to introduce Ag_2S junctions into the network. Sulfurisation was achieved by exposure of the chip with the silver network

on it to sulfur gas via evaporation of sulfur. The length of sulfurisation was determined by measuring the resistance across the device throughout the process, and removing the device when the resistance reached $\sim 1\text{ M}\Omega$. The sulfurisation setup is shown in Fig-

Figure 7.7: Sulfurisation of a network of deposited silver nanowires. The sulfurisation was achieved by evaporating sulfur at 140 °C in a closed chamber with the ASN chip suspended above (a). Resistance was measured throughout (b), with the chip shown here being removed from the chamber at 850 s.

ure 7.7 (a) as a schematic showing a crucible of solid sulfur, which was melted on a hotplate held at 140 °C to produce sulfur vapour. The vapour is contained in an upturned beaker in which the chip is suspended on a wire stand. The steps of the process are detailed here:

1. ASN chips were affixed to a wire stand for minimal heat conduction during sulfurisation. Two electrodes were connected to a multimeter using silver paint to enable resistance measurement during Sulfurisation
2. 10g of sulfur powder was placed in a watch glass on a hotplate held at 140 °C and allowed to pre-melt
3. The wire stand with the attached chip was then placed over the melted sulfur, and covered with an upturned beaker

4. The resistance was measured continuously to determine the length of time to sulphurise the device for, which varied between devices from 5 min to 30 min. An example of the resistance measured for a two-terminal device is shown in Figure 7.7 (b).
5. At a measured resistance of 100 k Ω the beaker was removed, and the wire stand was taken off of the hotplate without ceasing to measure the device resistance
6. An increase in resistance from 100 k Ω to $\sim$ 1.5 M Ω was normal after removal of the chip from the sulfurisation chamber

In Figure 7.7 the chip was removed at 850 s corresponding to a resistance of 1 M Ω . Over the course of the next 50 s the resistance rose to 80 M Ω where it remained stable. The rapid increase in resistance following a gradual change over time is characteristic of connected silver networks in the literature [6, 162]. After the resistance of the device across the two channels measured during sulfurisation had stabilised, all of the remaining electrical pads were checked. The resistance across pads was pairwise checked via multimeter to ensure that they were electrically connected to the network. The two-terminal and MEA measurements shown in this work were performed on devices with no floating connections.

7.5 Sixteen channel multi-electrode array device platforms

A device platform that allowed measurement of the ASN across the network area using multiple electrodes was designed in order to fully characterise the ASN systems that were initially fabricated and characterised using two-terminal devices. Although this necessitated more complex fabrication, the primary means of using the dynamic signals from an ASN system in the literature require multiple signals from a single device, which has been reported using multi-electrode arrays [8, 16, 17, 22, 141, 159, 160, 163, 164]. A multi-electrode array device as shown in Figure 7.8 (a) is an array of electrodes that allows contact to the system at a grid of points across the network area. The electrodes were encapsulated with a 300 nm layer of insulating SU8 to prevent contact between the

Figure 7.8: (a) multi-electrode ASN chip with 2 mm × 2 mm sulfurised silver network at center. (b) diagram of a single electrode showing encapsulation leaving large square outer electrodes uncovered for electrical connection and a 100 μm region of the electrode uncovered to provide electrical contact at a precise location within the silver network area. (c) electrical connections in a 4 × 4 grid in the network area showing the source and ground on pins 1 and 16 and voltage probes v2-v15. (d) precise electrical contact achieved with vertically aligned spring-loaded pogo pin contacts to the outer electrodes on the chip.

electrodes and silver nanowires except at a 100 μm circle at the end of each electrode end within the network area. Encapsulating of the electrodes is schematically drawn in Figure 7.8 (b). The electrical contact made to 16 points in a grid across a 2 μm x 2 μm ASN network area is shown in Figure 7.8 (c).

The diameter of the holes in the SU8 was set to be 100 μm to ensure that the spray-coated silver wires would be able to contact the electrodes. The wires used had a length of 20 μm to 60 μm , which ensures that no wires would be able to bridge the hole in the SU8 without contacting the electrode on the surface below. The electrical contact was tested prior to sulfurization via multimeter measurement of the pad-to-pad resistance. Resistances measured were from 50 Ω to 1000 Ω , and resistances higher than 1000 Ω were rejected. The resistance across an unsulfurised device Figure 8.12 agreed to within uncertainty with the multimeter measured $(875 \pm 50) \Omega$ and $(853.000 \pm 0.703) \Omega$. Control measurements are discussed in further detail in Section 8.2.2.

The two-channel test devices could be readily measured using manually positioned probes to contact the electrodes. With 16 electrical contacts, manual positioning of probes for electrical contact becomes time and equipment prohibitive. A mechanical chip carrier was designed that used spring-loaded pogo pins to contact all 16 electrodes simultaneously as shown schematically in Figure 7.8 (d). Alignment of the chip and the contact pins was achieved using a 3D printed alignment block registered mechanically with the 1.5 cm $\times$ 1.5 cm chip. A pre-aligned mechanical rig allowed easy loading and unloading of chips for measurement.

7.6 Electrical measurement setup

The multi-electrode device shown in Figure 7.8 (a) were measured using a National Instruments (NI) PXI based measurement system with a number of modules offering an extensive suite of electrical measurement capabilities. An NI-4138 source measure unit (SMU) was used to drive the device at a constant voltage across pins 1 and 16 as shown in Figure 7.8 (c), while the voltage across the network area was measured on channels 2 - 15 using an NI-4303 Multichannel Data Acquisition (mDAQ) card. The NI-4303 provides up to 32 differential voltage probes, 14 of which were attached between pin 16 (ground) and each of the 14 channels to measure the voltage across the device area.

A custom LabView script was written to control the measurement. The 14 channels of voltage data from the NI-4303 and the driving voltage and device current from the NI-4138 were synchronised using the PXI chassis' internal clock signal. The data from the NI-

4138 was typically collected at 100 Hz unless otherwise noted, while the voltage data was collected simultaneously at 1 kHz. The maximum sample rates for the NI-4138 and the NI-4303 are 1.8 MHz and 50 kHz respectively. The NI-4303 has a voltage resolution limit of 24 bits. Using the maximum range of 60 V this yields a resolution of $\sim 3 \mu\text{V}$. Each differential voltage probe in the NI-e4303 (National Instruments) multichannel differential voltage measurement system has an input impedance of $>1 \text{ G}\Omega$. The maximum resistance of the systems measured when switching was $1.2 \text{ M}\Omega$. Thus the effect of the input resistance of the voltage probes would be to cause at most a 0.12% systematic error in the voltages measured due to current flow through the voltage probe instead of through the network. Noise is observed in measurements that far exceeds the instrument limit, indicating that further optimisation could be done on the circuitry connecting the chip to the DAQ to improve the signal-to-noise ratio. The considerable noise in the voltage measurements is to be expected, as the electrical system used to connect the DAQ and chip was designed with flexibility in mind, in order to test multiple configurations and connections without having to rework components. In future, dedicated hardware could be developed to remove all of the modular coaxial connectors between the NI-4303 and chip, and instead have a direct shielded ribbon cable connector between the instrument and chip carrier.

7.7 Summary and future work

This chapter details the work done to develop the capability to fabricate and measure Ag_2S ASN devices from work in the literature [6, 8, 16, 17, 22, 141, 159, 160, 162–164].

Simple two-channel device platforms were designed to allow rapid prototyping of fabrication methods for producing sulfurised silver networks. Spray deposition of solution suspended silver nanowires was selected for the fabrication of complex interconnected quasi-2D networks of silver. Gas-phase sulfurisation was then used to form Ag_2S junctions between adjacent wires in the network. An electrical measurement system was developed to allow the time-resolved conductance and spatial voltage data from across the network region to be collected.

Spray coating of premade silver nanowires was shown to be a robust and rapid

method for silver network fabrication but posed some difficulty regarding controlling the density of the networks that were fabricated. Lack of density control has been compensated for by using the sulfurisation step to ensure that the networks fabricated have a post sulfurisation resistance of $\sim 1\text{ M}\Omega$. However, it is not difficult to realise that a high-density network that has been extensively sulfurised to and a low-density network that has been moderately sulfurised may have the same resistance, but will inherently differ due to the difference in the size of the Ag_2S junctions as well as their number and connectivity. Electroless deposition of silver networks from drop-cast and lithographically defined copper seed sites were investigated to provide more explicit control of the network density but determined that the extensive parameter space that determines the silver nanostructures would require significant future optimisation to achieve a robust fabrication process.

After ASN devices on the test device platform, which were fabricated using spray deposited silver networks, a sophisticated device platform was designed to allow measurement of the spatiotemporal variation of the signal from ASN devices. 16 channel multi-electrode array based devices were fabricated, and an electrical measurement system was designed to allow time-resolved measurement from all channels simultaneously. The results of electrical measurements of both two-channel and multi-electrode devices, using swept and constant driving voltages, are detailed in Chapter 8.

Chapter 8

Ag–Ag₂S–Ag atomic switch network devices

The ASN devices were first electrically measured under triangular voltage bias to determine the extent to which characteristics of the Ag₂S atomic switches were exhibited by the ASN device, and what traits were emergent due to the network structure. A slow increase in conduction was observed under positive voltage sweeps due to phase change and initial filament growth in the Ag₂S junctions followed by a sharp increase in conduction due to the formation of the metallic filaments within the Ag₂S. The observed switching behaviour and characteristic pinched hysteresis under repeated voltage sweeps were consistent with filament formation and dissolution in the Ag₂S junctions [7, 181]. We showed semistable conductance states consistent with the memristor-like behaviour of ASN systems in literature [6, 163]. We attribute the semistable device response to positive and alternating voltage sweeps to be due to the network connectivity of symmetric Ag₂S junctions where off-switching was driven by equilibrium relaxation as described in Section 6.2.3.

Multi-electrode array (MEA) devices were fabricated as described in Chapter 7 that allowed the measurement of the voltage across the atomic switch network area during switching measurement. By using DC driving voltages, these MEA devices were used to analyse the power law size and time distributions of the switching event. These showed power law distributions consistent with self-assembled critical network sys-

tems. The spatiotemporal evolution of the voltage across the network area was investigated. Changes in relative voltages across the network were found during switching events, demonstrating distributed switching throughout the network. Finally, principal component analysis was used as a novel analysis technique on ASN systems to reduce the dimensionality of the multichannel voltage data to allow examination of stable and transitional states within the network. We developed these tools and methods to visualise and analyse the spatial variation in conductance in order to better inform future work on integrated ASN and CNT devices.

8.1 Testing atomic switch network connectivity

The first step in characterising the ASN devices fabricated was to verify their connectivity and the presence of silver filament formation across the Ag_2S junctions within the network. In order to do so, ASN devices were fabricated by spray-coating silver nanowires onto prefabricated gold contacts, and sulfurising by exposure to sulfur gas until the resistance across the device was measured to be $0.1\text{ M}\Omega$ to $1.5\text{ M}\Omega$ as described in Chapter 7. These initial devices were measured using the two opposite electrical contacts to obtain I-V data across the network. Similar behaviour was observed using adjacent electrode pairs, so opposite pairs were used for consistency.

Filament formation

Each device was subjected to positive unipolar voltage sweeps to induce filament formation in the $\text{Ag}-\text{Ag}_2\text{S}-\text{Ag}$ junctions throughout the network. The current and voltage were recorded and used to calculate the conductance using $G(t) = I(t)/V(t)$. Following the convention in the literature, conductances are given in units of the conductance quantum $G_0 = 2e^2/h$ where e is the electronic charge and h is Planck's constant. The magnitude of the voltage sweeps was gradually increased until a sharp conductance increase consistent with the formation of metal filaments across junctions within the network was observed.

The mechanism for filament formation has been characterised in the literature and

is detailed in Section 6.2.2. Briefly here:

1. Voltage-driven phase change in the Ag₂S junction from argentite phase to more conductive and higher ionic mobility acanthite phase
2. Ag⁺ ion migration through the acanthite channel and reduction at the cathode to form a metallic silver filament.
3. Filament formation bridging the Ag₂S junction causes a sharp increase in conduction
4. Chemical equilibrium in the Ag₂S drives filament dissolution and phase reversal without a voltage driving the junction away from equilibrium.

The ASN devices that were measured showed evidence of filament formation after a certain number of sweeps corresponding to the necessary current flow through the junctions in the network to completely form filaments, providing the driving voltage was above a certain threshold voltage. Bipolar voltage sweeps with a magnitude below the voltage required for formation were then used to probe the switching of the device after the initial filament formation.

Figure 8.1 (a) shows five successive IV sweeps from 0 V to 0.7 V across a two-terminal ASN device directly after sulfurization where the initial conductance was measured to be 0.008 G₀ (1.7 MΩ). For each successive sweep, the conductance increased incrementally from 0.008 G₀ to 0.013 G₀ as shown inset. The small relative conductance change of only 18% is consistent with the gradual conduction change due to acanthite channel formation and filament growth across Ag–Ag₂S–Ag junctions within the network.

Figure 8.1 (b) shows five successive IV sweeps from 0 V to 1.1 V across the ASN device where prior measurements at lower voltage sweep magnitude were shown in Figure 8.1 (a) and had shown no evidence of filament formation or switching. On the third sweep in Figure 8.1 (b) the current responses increased sharply corresponding to a conductance increase from 0.01 G₀ to 0.2 G₀ shown in the inset. The formation voltage of this device was thus 1.1 V as this was the voltage sweep magnitude where a sharp conductivity increase was first observed. The first rapid increase in conductivity under repeat bias sweeps has been termed 'formation' in ASN [6, 17], and is due to filament formation

Figure 8.1: Voltage sweeps across an Ag–Ag₂S–Ag ASN device immediately following sulfurization. (a) I–V sweeps from 0 V to 0.7 V show smooth and only slightly nonlinear current response and gradual conductance increase (inset) prior to metallic filament formation across the device. (b) IV sweeps from 0 V to 1.1 V show a sharp change to nonlinear current response and an increase in conduction (inset) between sweep number 2–3 due to formation of metallic filaments across the junctions within the network. Conductance vs sweep number shown inset in (a) and (b)

throughout the Ag₂S junctions in the network. The filament formation observed in literature studies on single Ag–Ag₂S atomic switches was shown to occur after repeat voltage sweeps above a certain voltage ~ 100 mV [7], called the formation voltage, as high as 5 V in network devices [17]. The higher formation voltage in network devices is attributed to the highly parallel conduction paths through the network and the large number of junctions in any given conduction path. The voltage across the network as a whole is divided across these junctions, and filament formation occurs on any junctions that have a voltage drop over their individual formation voltage. We observed threshold voltages from 0.5 V to 5 V between devices due to variations in network fabrication. Filament formation is necessary for further switching and dynamics, which depend on the breaking and reformation of small regions of the already formed metallic filaments spanning the

Ag₂S as described in Section 6.2.2 and in the literature [7, 17].

Formation is a necessary step to preparing an ASN device for dynamic switching [17, 22]. Because of the interconnected nature of the networks used, understanding how the formation step occurs at a junction level throughout the network is non-trivial. To better understand how this occurs, a combination of characterisation of the junction properties in the network, and a model as to how these interactions could be used. SEM/TEM could be used as in Xu et al. [183], to examine the physical sizes of the junctions formed when sulfurising adjacent wires. This could be used to provide values with which to model the junctions using the memristor equations in Section 6.2. Plugging this information into a network simulation would then allow simulation of the voltages behave in the network. The simulation presented in Chapter 5 could be used for this, as it was designed to be adaptable to any conducting element that had a linear relationship between current and voltage. The time/charge dependance of the junctions could be incorporated by updating the junction state using Equation 6.2. Such a conducting network simulation would hinge on obtaining reasonable estimates for the junction parameters within the network.

8.1.1 Post filament formation switching

Following the formation step, the device was measured with bipolar voltage sweeps with a magnitude less than the voltage used to achieve filament formation. Figure 8.2 shows an ASN device with a formation voltage of 0.4 V driven at ± 0.3 V where a clear and sharp nonlinear hysteresis is observed consistent with the ASN operating as a memristive system [8, 17, 164]. The direction of the IV curve annotated in Figure 8.2 shows the on-switching from an initially low conduction state at a high positive voltage, and then the subsequent off-switching at a negative voltage back to the original state. The abrupt switching between high and low conductance, and the zero-crossing of both conductance states is called pinched hysteresis, is characteristic of memristive systems described in Section 6.2 [6]. It should be noted that Figure 8.2 is a selected current response to demonstrate hysteresis, but in general, the ASN devices measured did not show repeat pinched hysteresis response. We instead observe irregular switching while driven with

Figure 8.2: IV sweep from -0.3 V to 0.3 V across an ASN device after formation of silver filaments across the network showing clear hysteresis characteristic of memristive systems. The start and switching points are indicated along with the regions indicative of on and off states. The hysteresis following the direction of the arrows (red).

regular voltage sweeps.

Figure 8.3 shows the IV characteristics of an ASN device post-filament-formation driven at $\pm 0.3\text{ V}$ for 10 bipolar triangular voltage sweeps. Switching is observed as a change in the slope of the IV curve. The changes between high and low slope (conductance) occurs at varying voltages for each sweep. The conductance calculated at each point as V/I is plotted inset. The conductance switches in the range $0.01 G_0$ to $2.2 G_0$ for the first 5 sweeps before settling in a low conductance state of $0.01 G_0$. The switching between high and low conductance states Figure 8.3 in the first five voltage sweeps does not occur at a certain set voltage. This lack of a set voltage where on- and off-switching occurs suggest that the interconnected nature of the network makes the behaviour of the ASN not directly mappable to the behaviour of a single atomic switch. A single junction begins to switch on when the voltage across it is above V_{Th} as described in Sec-

Figure 8.3: 10 bidirectional IV sweeps from 0.3 V to -0.3 V and back again across an ASN device post filament formation step. Silver filaments across $\text{Ag}-\text{Ag}_2\text{S}-\text{Ag}$ junctions throughout the network form and dissolve, resulting in a rapidly changing conductance between semistable conductance levels followed by a decay to a stable low conductance state (inset).

tion 6.2.2. Switching proceeds according to the amount of charge flowing across the channel as the metal filament forms. A network is composed of many of these junctions interconnected, and so the voltage and charge flow across any given junction is dependant on the other junctions in the network. The lack of periodicity in Figure 8.3 is due to this connected nature of the junctions causing certain regions of the network to switch

independently, rather than the whole network switching at once. The eventual relaxation to a low conductance state shown in Figure 8.3 (inset) was common for devices that were driven by triangular sweep with an amplitude near to the formation voltage. Devices would either settle to a constantly high, or constantly low voltage corresponding to filament formation or dissolution across the network as a whole. Settling of the device to a low(high) conductance state can be reversed by increasing(decreasing) the driving voltage amplitude. Later work measuring MEA devices at a constant voltage in Section 8.2.2 avoided the device settling to a constant conductance state by fine-tuning the driving voltage used.

8.1.2 Symmetric switches with equilibrium driven off-switching

Switching that does not occur at a set voltage in each sweep such as those shown in Figure 8.3 can be explained by equilibrium driven filament off-switching in symmetric Ag–Ag₂S–Ag junctions in the ASN devices measured as described in Section 6.2.3.

We demonstrate semistable conductance states for a device that is driven with a voltage above the formation voltage consistent with the literature. In the two-terminal silver network devices, further semistable switching between conductance states in the range $0\ G_0$ to $22\ G_0$ is shown in Figure 8.4 (a) where an ASN device that showed evidence of filament formation at 0.4 V is driven with $\pm 0.5\ V$ triangular sweeps. The device switches between a $22\ G_0$ state and a $\sim 16\ G_0$ state repeatedly for the first seven sweeps, after which the switching becomes erratic for five sweeps. The system then settles at a $22\ G_0$ conductance state for the remainder of the measurement. A stable high conductance state is consistent with literature work on single junctions [7]. Such a state is reached after repeated triangular voltage sweeps with an amplitude above the voltage where the formation is originally observed [7]. This high conductance state corresponds to the formation of connected silver filaments across the Ag–Ag₂S–Ag junctions throughout the network. In Figure 8.4 (b) the same device as in (a) is driven with unipolar triangular voltage sweeps from 0 V to 1 V. The conductance of the device switches between a number of stable states between $21.5\ G_0$ and $25.5\ G_0$ where transitions are not repeated, periodic, or correlated with a particular voltage value.

Figure 8.4: Non-periodic switching between semi-stable conductance states shown under periodic driving voltage for ASN devices after filament formation has occurred. (a) Repeated triangular voltage sweeps from -0.5 V to 0.5 V (blue) across a formed ASN device at greater than filament formation voltage. The conductance (purple) shows large magnitude $22\text{ }G_0$ and $5\text{ }G_0$ switches between stable conductance states. (b) Repeated triangular voltage sweeps from 0 V to 0.5 V (blue) across the same device. The conductance (purple) shows small magnitude $1\text{ }G_0$ and $0.5\text{ }G_0$ switches between stable conductance states.

In contrast with this work, Stieg et al. [163] showed switching between conductance states $0.065 G_0$ and $1.61 G_0$ in Ag–Ag₂S–Ag ASN devices that were stable for 100 switching cycles. This seems to initially contradict the idea of equilibrium driven off switching within the network, as it suggests that the off switching is somehow driven by the voltage sweep. However, it should be noted that such stable switching was only achieved at low switching rates. This suggests that their devices are actually being allowed to completely relax between each driving cycle, rather than the reverse sweep having any effect on off-switching. By switching slow enough that the network relaxes into the off-state, and using voltage sweeps well above the formation voltage, stable switching could be achieved but is inherently limited by the relaxation of the network, which is not well characterised.

The observed on and off-switching events when the device in Figure 8.4 is only ever driven at positive voltages supports the model of equilibrium driven off-switching in the system. The irregular switching voltages here support equilibrium driven off switching in symmetric junctions as described in Section 6.2.3. We examine the dynamics of switching when driven at DC voltage in Section 8.2 to better quantify the dynamics of this switching.

8.2 Atomic switch network measurement using multi-electrode arrays

To understand the nature of the dynamic switching within the network, the change in conductance across the network as a whole was measured while the device was driven by a DC voltage as described in Section 7.6. We aim to examine whether our results are consistent with neuronal systems exhibiting self-organized criticality (SOC) by showing the distribution of the size and length of the switching events follows a power law distribution with a critical exponent of $\alpha = 1.5$ [2, 18, 19]. The link between SOC, the critical exponent $\alpha = 1.5$, and the switching dynamics of ASN systems is described in Section 6.4.1. Although the conductance is measured across the entire network area, the switching events that cause it may occur in some or all of the network. Both the conduc-

tance across the whole device, and the voltage measured across the network area were measured for MEA-based ASN devices. We first examine how the conductance switching measured across the whole network is characteristic of SOC.

To analyse the spatiotemporal dynamics of switching within the ASN devices used, MEA devices were fabricated as described in Section 7.5. Briefly, devices were fabricated that had 16 point contacts in a grid across a 2 mm × 2 mm ASN device region. The devices were driven at a constant voltage across two contacts, and the current was measured through them. The other 14 contacts in the network area were used to measure the voltage across the network area with respect to ground.

8.2.1 Conductance switching events in atomic switch networks

In Figure 8.5 (a) the overall conductance of the device between the source and ground varies from $0.03 G_0$ to $32 G_0$ when driven at 2 V. The changes in the voltages measured across the surface of the device with respect to ground are shown in Figure 8.5 (b), vary from 0 V to 0.77 V with an uncertainty of ± 0.06 V. The voltages across the device area are colored according to their physical location according to the device area map shown inset. They are overlayed, and so prove difficult to directly analyse due to the overlap in the voltage signal. The analysis of the voltage data will be covered in Section 8.2.2. The focus of the initial analysis was on the variation in the conductance across the entire network as described below.

A switching event was defined as any conductance change above a certain threshold value determined by examining the noise in a given conductance measurement to ensure only significant transitions are recorded. For the events shown in Figure 8.5 the conductance threshold for events was chosen to be 3% of the maximum conductance range measured across the ASN device which in this case is $1 G_0$. Switching events were detected by calculating the difference between the conductance of successive data points ΔG . The time of occurrence and the size of each event above the conductance threshold was recorded as a switching event within the network.

Both the time between switching events [18, 19, 168, 201], and the size distribution of such events [2, 201], are important metrics for understanding the dynamics of neuro-

Figure 8.5: Electrical data collected from an MEA device driven at 2 V between contacts diagonally across the network area as shown inset over 115 s. (a) conductance variation over time was calculated from the current measured between the source and ground and the driving voltage. (b) voltage measurements between each channel and ground were measured across the area. Voltage traces were color-coded according to their position in the network area (inset)

morphic and critical systems and are examined here. In Figure 8.6 (a), (b) and (c) respectively the switching events determined by threshold from the raw conductance measurement shown in Figure 8.5 (a) are plotted against their time of occurrence, at 3 time scales of 100 s, 10 s, and 1 s. The appearance of groupings of switching events at all three

Figure 8.6: Events above the change in conductance threshold $\Delta G > 1 G_0$ are plotted against their time of occurrence at 3 different time scales, (a) 100 s, (b) 10 s, and (c) 1 s showing periods of activity and inactivity at a range of timescales. (d) the magnitude of conductance transitions $\Delta G > G_0$ is plotted against their probability of occurrence in the full dataset on a log-log scale. The fit to a power law is shown in black with an exponent $\alpha = -1.45$. In (e) the size of inter-event intervals (IEIs) between transitions $\Delta G > 1 G_0$ are plotted against the probability of occurrence. The IEI power law fit is shown in black with an exponent $\alpha = -1.40$

time scales shown in Figure 8.6 (a)-(c) illustrates a similarity between the nature of the patterns of events and those seen in biological systems [168], where so-called "bursty events" characterise the time behaviour of the system.

A characteristic of critical systems is the power law distribution of the time occurrence of events [168] and the size of such events [2, 21]. A power law is of the form $y = cx^\alpha$

where the critical exponent α defines the slope of the distribution when plotted on a log-log graph due to the transformed equation $\log y = \log c + \alpha \log x$. A power law exponent of $\alpha = -1.5$ is characteristic of 2 dimensional self-assembled critical systems [2, 21].

We calculate critical exponent α to examine the power law dependence of the events in Figure 8.6 (a)-(c). The switching events that were identified ranged in size from $1 G_0$ to $29.5 G_0$. The data was binned into 20 even partitions of size $1.4 G_0$, and the number of events in each bin was normalized by the total number of events to obtain the probability of an event occurring at that magnitude. The size vs probability data was then plotted on a log-log scale, and fit with a least squares linear model. The slope of that linear fit is the measured power law exponent α . The power law distribution of the size of the switching events measured is shown in Figure 8.6 (d). The power law exponent calculated was $\alpha = -1.45 \pm 0.12$, with the uncertainty as one standard deviation σ_α from the linear fit. A similar analysis was performed on the inter event intervals (IEIs) which ranged from 0.01 s to 3 s. The IEIs were binned, and the counts converted into a probability of occurrence as with the event sizes. The IEI size vs probability of occurrence was then plotted on a log-log scale in Figure 8.6 (d) and a linear fit was performed. The size of the IES follow a power law distribution with $\alpha = -1.40 \pm 0.08$. The critical exponent calculated agreed to within σ with the characteristic power law exponent for SOC of $\alpha = -1.5$ for the switching event sizes and within 2σ for the IEIs.

Power law analysis of the switching events observed on a different sample (shown later in Figure 8.7) also show good agreement with $\alpha = -1.5$. Using a threshold of 3% of the maximum conductance range to determine switching events, and performing linear fits to the log-log probability of occurrence of event of a given size and IEI, critical exponents of the event size $\alpha = -1.52 \pm 0.17$ and IEI $\alpha = -1.44 \pm 0.25$ both agree with $\alpha = -1.5$ to within σ . Literature reports of $\alpha = -1.34$ [17] and $\alpha = -1.38$ [22], which only agree to within 10% with $\alpha = -1.5$ have been used as evidence of SOC in ASN devices. We have shown closer agreement, but have uncertainty in our values of up to $\pm 16\%$.

Extending the linear fit over an increased range of orders of magnitude would more conclusively confirm the SOC of our ASN devices. A fit over a larger range would help to reduce uncertainty, and yield insight on where the power law fit breaks down. The potential for a significantly larger range of event sizes is limited on the low end by the

threshold used to detect switching events, and on the upper end by the maximum conductance of the ASN device. Future investigation of more dense devices, devices with larger contact electrodes, or devices with an increased network area could provide greater maximum conduction. However, these changes would require reworking the device architecture and fabrication process used in this work.

A more feasible next step would be to investigate increasing the range of event intervals measured. The measurement time interval of ~ 100 s and the sampling rate of 100 Hz impose hard constraints on the minimum and maximum IEI of 0.01 s and 100 s. These parameters were chosen for this work due to file size constraints while sampling 14 voltage channels and current across the device simultaneously. In future work the measurements made could be altered to only collect current across the device. Running the measurements for extended periods of time on the order of hours, and sampling up to the maximum 1.8 MHz available on the current instruments, would open up a possible four orders of magnitude on the low end of IEI and an upper limit only limited by patience and device stability.

An additional benefit to increasing the time of measurement would be that statistical variations in those event sizes/IEIs that are very infrequent would be less likely to impact the probability of occurrence calculated from the data. For example, the two points visible in Figure 8.6 (d) that sit far below the power law fit may be due to statistical fluctuation. The true probability of such an event occurring may be higher than calculated, as those two points correspond to switching events that occur only once and twice respectively in the measurement window. By increasing the time of measurement those events with a low true probability of occurrence will be sampled more times, thus yielding a better approximation to the true probability. Conversely, those events could genuinely reflect a lack of power law dependance for the largest switching events. If that is the case, it would suggest an upper limit on the size of a switching event for that network.

Measuring an increased range of IEI would also improve our understanding of the limits of the devices manufactured. It is unlikely that sampling at 1.8 MHz for a month would yield IEIs showing a power law exponent consistent with SOC from 5.5×10^{-7} s to 2.6×10^6 s. Instead, the lower and upper limits of the switching intervals could be

exposed providing insight into the maximum switching rate (minimum IEI) and the maximum stable switching period (maximum IEI). In this work, there is no non-linear tail on the of the IEI power law in Figure 8.6 (e) that would be conclusive evidence of either limit being reached in the data presented here.

8.2.2 Spatio-temporal variation of voltage across atomic switch networks

In order to measure the switching across the ASN device area, MEA-based ASN devices were developed as described in Section 7.5 to measure the signal variation across the network directly. Self-organised criticality (SOC) is characterised by the power law dynamics of the switching of a system which are directly tied to the spatial extent of propagation of a perturbation to the system as described in Section 6.4.1. Literature application of these ASN systems to reservoir computation have used the variation in voltage at points across the network area to provide complex variation on an input signal [8, 16]. The focus in the literature has been on direct application [22, 159], while qualitative and quantitative analysis of those voltage channels has not been well established.

We start by examining an alternative visualisation of multiple voltage traces overlaid over one another, to better interpret the voltage channels across an ASN area while the network is switching. A different MEA-based ASN device from that shown in Figures 8.5 and 8.6 is driven at 5 V DC over 45 s. The conductance between the source and ground is shown in Figure 8.7 (a), which shows formation of the device visible as the initial smooth increase in conductance prior to $t = 5$ s. After this, the device shows conductance changes consistent with switching. The voltages measured across the device area are shown in Figure 8.7 (b) where 14 voltage channels are shown measured between the grid of points across the network area and ground respectively. Figure 8.7 (b) shows the spatial variation of voltage across the network area to be feature rich in the time direction but this data is challenging to interpret despite colour coding of the channels due to overlapping of the voltage signals. To add visual clarity to the voltage traces present in Figure 8.7 (b) they have been colour coded according to the spatial mapping shown inset. Those voltage traces close to the voltage source are red, and those close to the

Figure 8.7: 46 s of voltage data from an MEA device driven under 5 V. Current through the system was measured at 10 Hz and used to calculate the conductance shown in (a). In (b) 14 voltage probe traces were measured between a grid of points across the network area and ground sampled at 1 kHz. Voltages are color-coded as shown inset and overlayed, with close to source, close to drain, and equidistant from both are red, black, and blue respectively.

ground point are black, with those equidistant between the two being blue.

8.2.3 MEA measurement validity and voltage trace clumping

Before continuing to analyse the complex multichannel voltage signals shown in Figure 8.7 (b), we first examine the validity of those measurements. The MEA devices and the PXI measurement system detailed in Chapter 7 were the first attempts by our research group to measure ASN network devices. One of the primary results of this work is thus to verify the functionality of the devices as expected from other works in the literature [17, 22, 163], as well as our ability to measure them.

Control measurements

An open circuit control was performed on the measurement apparatus with the chip carrier connected and a chip loaded which had no nanowires on its surface. The open circuit conductance is shown in Figure 8.8 (a) for comparison with the other measurements shown in this work and has a value of $(-1.140 \pm 0.185) \times 10^{-3} G_0$, and corresponds to a current of $(-443.0 \pm 71.8) \times 10^{-9} A$. The current and corresponding conductance was typical of the lowest values that were able to be measured on this system. In future work the slight offset observed could be corrected for in software or through hardware calibration, however all of the work done was well above this limit, and so it was not deemed critical for initial measurements. The 14 voltage traces shown in Figure 8.8 (b) show readings above and below the physically reasonable range for a driving voltage of 5 V. We observed similar voltage readings when no chip was loaded, consistent the amplification of spurious voltages in our system by the differential voltage probes of the NI-4303 DAQ used.

The measurement system described in Chapter 7 was used to measure a known passive circuit which was constructed of an array of resistors connected as shown in Figure 8.9. The values of the resistors used in each control were 2.2 k Ω and 220 k Ω for the measurements shown in Figures 8.10 and 8.11 respectively. The low and high resistance grids were selected to encompass the range of conductances that were observed when measuring active switching devices. The lower of the two resistance grids showed a conductance of $(3.170\,00 \pm 0.002\,14) G_0$, while the higher showed a conductance of $(32.400 \pm 0.243) \times 10^{-3} G_0$ over the full time period when driven at 5 V. The symmetri-

Figure 8.8: Electrical control measurement of the chip carrier detailed in Chapter 7 with a chip loaded where no nanowires are present. (a) shows the conductance of the system over 100 s and (b) shows 14 voltage traces measured with respect to ground over the same interval. The coloring of the voltage traces by their position across the network area if there were to be a chip loaded in the chip carrier. The DC driving voltage V_+ is 5 V.

Figure 8.9: Resistor grid arranged in an array of 4x4 contact points to mimic variation of resistance between the probes.

cally spaced voltage levels shown in both Figures 8.10 and 8.11 (b) directly relate to the position of the measurement point within the resistance grid, analogous to the position of the electrical contact within a network MEA device, and are distributed across the 0 V to 5 V driving voltage range.

Following the measurement of known resistor grids, measurements were performed on a MEA chip with a silver nanowire network that was unsulfurised using the full system and chip carrier. The resistance measured across pads 1 and 16 was measured to be $(875 \pm 50) \Omega$ with a multimeter prior to measurement on the PXI based measurement system. Figure 8.12 (a) shows a conductance of $(15.1000 \pm 0.0125) G_0$ over the measurement period of 140 s, corresponding to a measured resistance of $(853.000 \pm 0.703) \Omega$ which agrees to within uncertainty with the multimeter measurement prior.

The 14 voltage channels measured in Figure 8.12 (b) were tightly clustered about $(2.55330 \pm 0.00125) V$ over a range of 2.5 mV. Tight clustering of the voltages within the network indicates that the voltage drop from the source and drain electrodes to the network is large compared with the voltage differences within the network, indicating a large contact resistance between the leads and the nanowire network. The voltage clustering observed when measuring a MEA chip with silver nanowires deposited contrasts with the

Figure 8.10: Multichannel electrical control measurement of a 4×4 $2.2 \text{ k}\Omega$ which was measured using the same electrical equipment used to measure the MEA chip except that resistor grid was directly connected to the measurement leads, rather than using the chip carrier described in Chapter 7. (a) shows the conductance of the system over 120 s and (b) shows 14 voltage traces measured across the network with respect to ground over the same interval. The coloring of the voltage traces by their position across the network area is shown inset with a DC driving voltage $V+$ of 5 V.

Figure 8.11: Multichannel electrical control measurement of a 4x4 220 k Ω which was measured using the same electrical equipment used to measure the MEA chip except that resistor grid was directly connected to the measurement leads, rather than using the chip carrier described in Chapter 7. (a) shows the conductance of the system over 160 s and (b) shows 14 voltage traces measured across the network with respect to ground over the same interval. The coloring of the voltage traces by their position across the network area is shown inset with a DC driving voltage V_+ of 5 V.

spread of voltages seen when measuring a comparable resistance as in Figure 8.10. The difference between the two indicates that the change in the system arises from contact with the silver network on the MEA chip, as the passive resistive network was connected directly to the measurement leads, while the silver network is deposited on top of electrodes on the MEA chip. It is this contact between electrodes on the MEA chip and silver network that is most likely to be the cause of such significant contact resistance.

The presence of the chip carrier in the circuit is also a difference between the passive resistor grid and the silver wires on MEA chip, but it is comprised solely of soldered electrical connections, and spring loaded pins contacting directly with electrodes on the MEA chip both of which have been measured via a multimeter to contribute $<5\ \Omega$ of electrical resistance to the measurement system as a whole.

The voltage traces shown in these control measurements are consistent with the voltages expected from these known systems and establish the accuracy limit for our voltage measurements at $\pm 1\text{ mV}$. Any difference between voltages measured, or changes in voltage measured, that are over this magnitude are considered a significant difference or change. The differences in voltages measured from ASN devices shown in Figures 8.5 and 8.7 are significant where they are above that limit. The $>1\text{ G}\Omega$ input impedance of the differential voltage probes on the NI-4303 (National Instruments) is approximately 3 orders of magnitude greater than the highest overall network resistance of $1.8\text{ M}\Omega$ measured via multimeter or PXI system in this work. The high input impedance prevents any unwanted current flow through the voltage probes that would affect the voltage measured and supports the voltage accuracy of $\pm 1\text{ mV}$. Thus we assume that the voltage measurements are real, and features above $\pm 1\text{ mV}$ are a feature of the ASN or the electrical setup.

Voltage clumping

Given this assumption that the features of the voltage traces measured are real, and not artefacts of the voltage probe arrangement or measurement system, we must address the close clustering of voltage traces evident in switching measurements in Figures 8.5 and 8.7 and control measurements in Figure 8.12. If we consider the network in the simplest case to be a grid of resistors, we would expect the voltages measured to be spread

Figure 8.12: Electrical measurement of a MEA chip where silver nanowires have been deposited in a 2 mm square network area and then measured without sulfurization of the wires. (a) shows the conductance of the system over 140 s and (c) shows 14 voltage traces measured across the network with respect to ground over the same interval. The coloring of the voltage traces by their position across the network area is shown inset with a DC driving voltage V_+ of 5 V. (b) and (d) show the conductance and voltage traces zoomed in to the first 1 s of the signals shown in (a) and (c) respectively.

across the range from 0 V up to the driving voltage.

The control measurement of a network of unsulfurised network of nanowires in Figure 8.12 shows voltages which are very tightly clustered over a range of $(2.552\,00 \pm 0.001\,25)$ V while the system is driven at 5 V. We can determine the resistance at the source and drain are $5/0.0025 = 2000$ times larger than the resistance within the network, and that the resistances at the source and drain are approximately equal. Figure 8.12 shows a conductance of (15.1000 ± 0.0125) G₀ over the measurement period of 140 s, corresponding to a measured resistance of (853.000 ± 0.703) Ω which agrees to within uncertainty with the multimeter measurement of (875 ± 50) Ω across the same electrodes. This rules out significant chip-carrier probe resistance, as the multimeter probes were contacted manually directly on to the electrodes. Thus, despite ruling out some resistance due to the probe contact with the electrodes or some resistance in the probe apparatus, there appears to still be a significant resistance between the electrodes on the chip and the silver network. This would account for the tightly clustered voltages shown in Figure 8.12 in the network for this unsulfurised control system.

The voltages measured during device switching in Figures 8.5 and 8.7 are more tightly clumped than the passive resistor grid control measurements shown in Figures 8.10 and 8.11, but less so than the control measurement on an unsulfurised silver network in Figure 8.12. Figure 8.7 (b) shows level shifts of all voltages traces at once, as well as periods where the voltage clumping becomes more and less pronounced. Given that error due to probe impedance mismatch or high impedance in the chip carrier or probes has been, I propose a resistance that occurs at the electrode network, or near to it within the network. Figure 8.7 (b) shows level shifts of all voltages traces at once, as well as periods where the voltage clumping becomes more and less pronounced. Given that error due to probe impedance mismatch or high impedance in the chip carrier or probes has been discounted, I propose a resistance that occurs at the electrode network, or near to it within the network. Au–Ag₂S–Ag junctions could be the cause of the large and variable contact resistance between the electrodes causing voltage clustering. They are inherently variable, as they are themselves atomic switches, and so provide the variable quality that is necessary to explain the level shifts in voltages across the network when

switching is observed as in Figure 8.7. Alternatively, those Ag–Ag₂S–Ag junctions near to the source/drain contact could behave atypically in such a way as to account for the strong variable resistance. The high voltages and currents that they would experience by being near to the approximately point contact with the source or drain could alter their behaviour from that discussed in Section 6.2.2. Joule heating of junctions due to high current flow through them has been shown to destroy the metal filaments across junctions, increasing their resistance and potentially damaging the junction itself [180, 182].

The most notable spread in voltages measured in a device showing active conductance switching is from 2 s to 6 s in Figure 8.7, where the voltages spread to cover a range from 1.9 V to 3.2 V. This change in voltage spread occurs when the conductance through the network as a whole is increasing, but the start and endpoints of the region of high voltage spread do not coincide with any feature in the increasing conductance. Because of the finite increase of conductance for each atomic switch a continuous increase in conductance across the device can be attributed to an increasing amount of atomic switches turning on across the device, without significant accompanying off switching of other atomic switches.

The level shifts in all of the voltage channels that are correlated with the change in conductance suggest that the switching events that are having the most impact on the conductance are very near to the source or drain electrodes in the network. A shift of the voltages below 2.5 V would suggest that the switches near to, or directly at, the ground electrode have switched on. The increased conductance at the ground electrode compared with the resistance at the source electrode would cause the voltages throughout the network to shift to lower voltages.

Future work on the cause of voltage clustering

Being able to differentiate individual events in time would allow examination of whether the expected small number of switches near source and drain are responsible for the bulk of the switching. If individual switching events were visible in the conductance data over the period of increasing conductance, then an analysis could be made of whether an increase in conductance was due to many switches in parallel paths switched on,

or few switches in more dominant paths (for example close to the source or drain electrodes). This would require some re-engineering of the measurement system to remove high frequency responses in the cabling and probes. The PXI instruments are capable of up to 1 MHz sampling rate, but examining such high frequency data would require a second version of the measurement apparatus where its frequency response is optimised.

The work by Xu et al. [183] using a TEM to observe phase transitions and filament growth in a single Ag₂S atomic switch shows that realtime measurement of their operation is possible. Examining the physical dimensions and structure of the junctions that form at the electrode junction would shed light on whether they could be the cause of a high and variable resistance between the network and the electrodes. Conductive AFM of the device as a whole while under a driving voltage could provide information on where the real voltage drops exist in the network. To be clear, the imaging rate of an AFM is slow (~ 10 min) compared to the switching intervals (≤ 100 ms) measured in our devices in Section 8.2. These measurements would need to be taken voltages below the switching threshold voltage or on silver networks pre-sulfurisation, but would still provide insight as to the existence of significant voltage drops at or near the electrodes that would provide evidence for significant contact resistance.

If there is some electrode effect which is dominating the resistance across the network, and thus causing voltage measurements within the network to be clumped together, then a series of devices with modified electrode arrangements could be used to extract that effect. This work uses a regular array of circular (50 μm diameter) electrodes for all source/drain and voltage probe points as described in Chapter 7. A series of devices could be constructed with the same array of voltage point electrodes, but source and drain electrodes of varying area from the 50 μm to 500 μm in diameter, limited only by the spacing between source and voltage probe electrodes. Any effects that are due to some contact between the electrode and network should then scale with the contact area with the network. Future devices developed using wire networks which have been grown from copper seed sites may also be used to explore network-electrode contact effects. Our work and literature [162] on ELD of silver nanowires suggests that they remain physically anchored to the seed sites after growth. Thus, if the seed sites are fabricated directly on top of the electrodes, then those wires which grow on top of the electrodes

will have a better contact to that electrode.

A switching simulation would build on this work and the work in Chapter 5. A precedent for a memristor network simulation exists in the literature [187, 202], and could be used to inform the adaptation of my CNT simulation to an ASN system. The existing simulation structure could be used as is by taking the equations for a memristor described in Section 6.2 as an update rule for the resistances of the elements instead of a gate dependence as described in Section 5.2.1. Such a simulation would enable examination of the effect of switching certain areas of the network arbitrarily and calculating the effect on the voltage throughout the network. For example, switching the regions of the network close to the source and drain electrodes would help to elucidate the effect that would have on the voltages throughout the network. A simulation would allow the testing of ideas about the cause of large resistance(s) in the system in a more nuanced fashion than simple resistor models and could be used in concert with any of the other methods discussed as a comparison point.

Conclusively determining the origin of the high but variable resistances that cause a changing voltage spreading in this case with the data collected in this work is a challenge, due to limitations on the ability for us to measure individual switching events in the network. We present a number of methods that would enable future works to determine the nature of the mechanism that could be the cause of the observed voltage clustering. These include; increased time resolution to resolve individual switching events, conductive AFM to examine voltages within the network near electrodes, a series of modified device structures to examine the effect of contact size on our measurements, and ASN network simulations to test models for localized switching near electrodes.

The work by the Gimzewski group at UCLA on Ag_2S ASN device does not explicitly address the issue of contact resistance, or the presence of voltage clustering when they have performed these kinds of multichannel voltage measurements in recent work [16, 22, 141, 159]. Examining some of the voltage plots that they present in their work, Demis et al. [22] shows voltages within ± 0.1 V of each other when the network is driven at 2 V. This is consistent with the tight voltage clustering is observed in this work and suggests that meaningful analysis can be performed as evidenced by their use of the voltages across the network on similar systems for RC application [16, 141, 159]. Given the voltage

clustering evident in our work and in the literature, one of the significant challenges in ASN systems is the analysis of multiple tightly clustered dynamic voltage signals. We focus on developing techniques for intuitive visualisation and analysis techniques that can be used to analysis the dynamics across these ASN devices.

8.2.4 Alternative visualisation of multichannel voltage data

Figure 8.13 shows a restricted time interval of the full dataset from $t = 43$ s to 44.4 s. Within this time series, there are a number of qualitatively different voltage states. Spiked voltage states (i), low voltage stable states (ii), high voltage stable states (iii), and mid voltage troughs (iv). The voltage states in Figure 8.13 (i) to (iv) are examined by showing time slices at each point within the time-series as a 4x4 element heatmaps where the colour represents the voltage on that channel shown in Figure 8.13 (b) to (e). The voltage levels on each channel are shown as a spatial map using a colour scale showing the voltage level at the time point specified for Figure 8.13 (b), (c), (d), and (e). The spatial maps of the voltage at each time point can then be compared to visualise changes in the relative voltages between different points in time. The spatial voltage maps were used in an effort to visualise multiple varying voltage channels to better compare the voltage between channels over time.

The voltage scale is deliberately different between the 4 spatial maps of the voltage in Figure 8.13. The voltage scales have been normalised for each slice independently in order to emphasise the relative voltage difference between the channels. Maintaining a constant voltage scale for all 4 voltage maps would instead highlight the absolute voltage difference between time steps. We are interested in the relative voltage difference between channels because of what that shows us about the conductance variation within the network area. A change in relative voltage magnitude between channels over time indicates a localised change in conductance within the network. A local change in conductance is evidence of distributed switching.

In Figure 8.13 (b) channel 2 is greater than channel 6 which is adjacent to it, while in Figure 8.13 (c) channel 6 is now greater than channel 2 in addition to other more subtle relative changes in the upper right-hand corner of the network and an overall lower volt-

Figure 8.13: A section of the data between $t = 43.4$ s to 43.6 s showing a number of stable states and switching events. Voltages in (a) are colour-coded as shown inset, with close to source, close to drain, and equidistant from both are red, black, and blue respectively. The voltages across the network are shown at (i) $t = 43.08$ s, (ii) $t = 43.48$ s, (iii) $t = 43.55$ s, and (iv) $t = 43.96$ s in (b), (c), (d) and (e) respectively as grids. The color corresponds to the voltage measured at that channel and is normalised for each time slice to highlight the relative voltage between channels at a given time.

age range. The localised changing of the relative voltages measured is consistent with a conductance change due to switching occurring at localised areas of the network near to those channels showing the most significant voltage change. Similar relative voltage changes can be seen in all four slices in Figure 8.13 (b) to (e). These relative voltage changes show that the highest conductance regions in the network change as localized

regions of the network switch between formed and broken filaments across Ag_2S junctions between silver nanowires.

For all of the slices shown in Figure 8.13 it should be noted that in the lower half of the network the relative voltages show a similar pattern at these time slices, indicating that these regions show little or no switching behaviour between the points shown. Of the 1400 data points collected in $t = 43$ s to 44.4 s only 4 were selected in Figure 8.13. This shows that there is some difference in relative voltage, and thus internal conductance, between those points.

The spatial mapping of voltage used in Figure 8.13 (b) - (e) is applied to each point over a further restricted interval of time to give a more fine grained picture of the evolution of the relative voltages across the network area over a continuous period. Every time slice in the range $t = 43.4$ s to 43.6 s was examined to visualise the evolution of the voltage mappings over the switching event which occurs at $t = 43.55$ s without including any other apparent switching events. The time period examined for the switching event is shown as a zoomed in voltage trace in Figure 8.14. Figure 8.15 shows the same time

Figure 8.14: A section of the data shown from $t = 43.4$ s to 43.6 s from the full 46 s data set shown in Figure 8.7. The time interval shown captures a low voltage stable state (I) followed by a switching event at 43.5 s to 43.54 s (II) to a second stable high voltage state (III). Voltages are color coded as shown inset, where close to source, close to drain, and equidistant from both are red, black, and blue respectively.

range as Figure 8.14, but where a voltage map has been made for each time point. The colour scale for each voltage map is relative to the voltage range for that time slice, as was shown in Figure 8.13. However, for clarity the scale bars for each slice have not been displayed, as the important feature of each map is the relative voltage values. Changes in color between each slice indicate a change in local conductance due to local switching. Focusing on the evolution of the voltage maps over this restricted time period allows us to visualise a complete picture of the spatiotemporal evolution of the local conductance across the network over this period. Figure 8.15 shows that the relative voltage shifts that were observed at the preselected time points in Figure 8.13 vary in a continuous fashion over a single switching event. Being able to visualise the change in local conductance during network switching is an important tool for comparing the quality of ASN devices. The lack of relative voltage change in the bottom half of the voltage channels in Figure 8.15 indicates that the switching in this device is limited to half of the device area.

In future work, this kind of spatial analysis can be combined with analysis of the physical network using SEM. SEM would provide an avenue to estimate the density of the network using either a fractional coverage or a wire counting method. The network density could then be correlated with the variation in switching areas. Deliberate control of the fabrication processes explored in this work and in literature [162] relies on comparison with the electrical properties to determine what networks perform well. Visualising the switching within the network as shown in Figure 8.15 provides a manual way to judge the quality of the networks produced. In the case of an integrated CNT-ASN device which has motivated this work, being able to quickly and intuitively grasp the changes to the switching caused by a locally gated CNT layer is important for rapid initial prototyping where a quick judgment is key.

Figure 8.15 portrays an intuitive picture of the spatial evolution of the voltage across a switching event for rapid analysis of the quality of the switching that occurs. We investigate tools that can be applied to the multichannel voltage data to provide quantitative analysis alongside the intuitive judgement possible with sliced visualisations.

Figure 8.15: Representation of the restricted data from $t = 43.4$ s to 43.6 s where each square is a 1 ms time step in the data and the color corresponds to the relative voltage at each channel. The color is normalised to the average voltage at each time step to display relative voltage change with time. $t = 43.4$ s is represented at the top left corner, with time evolving from left to right. The time interval shown is the same as Figure 8.14 and shows an initial stable state (I) followed by a switching event at 43.5 s to 43.54 s (II) to a second stable voltage state (III).

8.3 Principal component analysis (PCA) of multi-channel voltage data

I was inspired to investigate PCA by Etchegoin et al. [203] where it is used as a tool for dimensional reduction of Raman spectra. PCA has also been recently applied to the analysis of high-dimensional, time-varying electrical data from biological neuronal systems [169, 193–195]. This work takes the novel approach of applying PCA to ASN or other artificial synaptic systems.

The goal of using PCA is to transform the 14 channel data to a lower dimensional data set, in order to make the analysis of the full 100,000 data points more feasible than when considering the full 14 dimensions. PCA is used to reduce the dimensionality of a dataset by transforming the basis vectors to be those which encode the largest variance over time as described in Section 6.4.2.

An essential characteristic of atomic switch networks is their ability to generate variations in the output signal at a range of time and magnitude scales [6, 22]. In the case of SOC systems, the temporal and spatial variation in the propagation of signals through the system is linked, and so a combined understanding of the switching dynamics and their spatial extent provides an important starting point for device applications. The spatiotemporal variation in voltage has been shown to be distributed throughout the network area and can be visually represented as in Figures 8.13 and 8.15. We aim to show that PCA can be used to reduce the dimensionality of the voltage data, while still encapsulating the change in voltages that are of importance when investigating the switching within the network.

8.3.1 PCA on 14 time varying voltage channels

To quantify the variation in 14 channels of voltage data over time the complexity of the data must be reduced to encompass only those aspects of the data across time and the network area that encode the variation. As shown in Figure 8.13 (b) - (e) the variation between spatial voltage mappings over time is restricted to some regions of the device. Thus a discussion of the variation during that time should encompass the variation in

those regions in some way.

By considering the 14 channels of voltage data collected at each time point as a 14-dimensional data set that varies over time, mathematical techniques can be applied to reduce the dimensionality of the system in order to focus on the qualitatively apparent variation.

We use PCA to transform the data from the reference basis:

$$b_{ref} = \{[1, 0, 0, \dots, 0], [0, 1, 0, \dots, 0], \dots, [0, 0, \dots, 1]\} \quad (8.1)$$

which are 14-dimensional vectors with zero in all elements except in the element corresponding to each of the 14 voltage channels measured, in to a new basis of principal component vectors:

$$p_c = \{\vec{p}_0, \vec{p}_1, \vec{p}_2, \dots, \vec{p}_{13}\} \quad (8.2)$$

where the basis vectors p_c are ordered in terms of the magnitude of the variance in the dataset that they encode. An example of PCA applied to an example dataset in two dimensions can be seen in Section 6.4.2. The principal components $p_0 \dots p_i$ are an orthogonal basis set which are ordered according to the size of their corresponding eigenvalues. p_0 encodes the maximum variance in the data set, and each successive p_i encodes the most variance in the dataset possible, provided that it remains orthogonal to the previous principal components. By considering the projection of the data onto the first two principal components that encode the majority of the significant variance in the data, a picture can be constructed in two dimensions that represents the majority of the variation in the full 14-dimensional dataset.

8.3.2 PCA on a single switching event

To explore the feasibility of using PCA, it is applied to a restricted portion of the data set and compare the results with known behaviour from visual analysis. The restricted time window from $t = 43.4$ s to 43.6 s as shown in Figures 8.14 and 8.15 was again used as a test case. The interval $t = 43.4$ s to 43.6 s comprises a dataset of shape (200,14) with 200 time points composed of voltage data across 14 channels before and after a large and distinct switching event.

Figure 8.16: a) plot of the fraction of the total variance in the data along each of the principal components of the restricted dataset shown in Figure 8.14 taken from $t = 43.4$ s to 43.6 s. Representations of the two most significant principal components p_0 and p_1 are shown in (b) and (c) where the relative contribution to each from the 14 voltage channels that comprise the reference is shown as red (positive) and blue (negative). The projection of the restricted dataset shown in Figure 8.14 onto the first two principal component vectors is shown in (d). The start and end points of the time sequence are shown in red and black respectively as a guide for the representation of the time evolution of each step in the system with respect to these two principal components.

The PCA algorithm extracted a new basis set of principal component vectors as well as the variance of the dataset along each vector when the data is represented in that new basis. For simplicity, the variance of the data along each data is shown as a fraction of the total variance in the data. A plot of the principal component number against its fraction of the total variance is shown in Figure 8.16 (a). As described in Section 6.4.2, the dimension of the data is reduced by selecting one or more of the principal components that have the largest variance, and projecting the data on to them. The two principal component vectors p_0 and p_1 are responsible for 64%, 23% of the variance in the data respectively as shown in Figure 8.16 (a).

The principal components p_c are unit vectors which are represented in terms of the reference basis b_{ref} of single voltage channels that make them up. For example, the first principal component p_0 is

$$p_0 = [0.29b_1, 0.18b_2, -0.51b_3, ..0.02b_{14}] \quad (8.3)$$

where the reference basis vectors b_n correspond to each of the 14 measured voltage channels respectively. A positive change in the direction of p_0 would correspond to a positive change b_1 and b_2 , and a negative change in b_3 etc. The principal component vector p_0 is shown in terms of the spatial position of its component reference basis vectors (corresponding to voltage channels) in Figure 8.16 (b). The positive (red) and negative (blue) contribution of each channel to these new basis vectors is shown. The two principal component vectors p_0 and p_1 are shown in this way in Figure 8.16 (b) and (c).

The dot product of the dataset $t = 43.4$ s to 43.6 s with p_0 and p_1 is used to project the data set onto those basis vectors as the data evolves. Because those two principal components collectively account for 94% of the variation in the dataset, the projection onto them should illustrate the majority of significant changes in the relative voltage space including the switching event that is known to occur. Figure 8.16 (d) shows the evolution of the data over the time period $t = 43.4$ s to 43.6 s projected onto the two basis vectors p_0 and p_1 shown in Figure 8.16 (b) and (c).

The time evolution in the projected p_0 and p_1 dimensions is shown in Figure 8.16 (d) as the data remains in a loose cluster centered on $(p_0, p_1) = (-0.05, 0.24)$ about the start point shown in red, followed by a rapid transition period corresponding to the switching event at $t = 43.55$ s, and finishing in a loose cluster located at $(p_0, p_1) = (-0.05, 0.24)$

around the end point shown in black. In this way, PCA has been used to represent the variation in the data in two dimensions in a way that is both visually clear, and mathematically robust.

To examine a time interval where switching occurs, 3 possible representations are shown. The restricted time region over which switching occurs can be visualised as shown in Figures 8.14 and 8.15, using overlaid voltage traces, and time slices of the relative voltages across channels respectively. We then used PCA to reduce the variation between voltage channels from a 14-dimensional to a two-dimensional dataset. When the data is projected onto these two principal components p_0 and p_1 we observe the evolution between two loosely clustered points in the p_0, p_1 projection. The evolution between semistable points is consistent with the switching observed in the voltage traces and time slices evident in Figures 8.14 and 8.15. We demonstrate that the change in relative voltage states shown in Figure 8.15 can be captured by projecting the 14-dimensional data onto the two most significant principal components and observing the evolution in that reduced dimensional space.

The cost of reducing the dimensionality of the data using PCA is the loss of the variance in the data captured by the other 12 unused principal components. In the above example, 6% of the variance in the data is lost by projecting it onto p_0 and p_1 . When applying PCA to a new dataset the relative variance of the resulting principal components must be assessed for suitability. If the variance ratios are all relatively similar (and thus large), selecting only 2 of them to project the data onto would result in a loss of a large proportion of the variance in the data. Such a case would thus not be suitable for dimension reduction using PCA. PCA is not a magic bullet, but a tool which should be used carefully, acknowledging the tradeoff between loss of some of the variance in the full data, and simplicity of representation.

8.3.3 PCA on a full switching dataset

The above example of PCA on a restricted dataset demonstrates its use as a tool to examine the dynamics of the relative voltages across the network area by reducing the problem dimensionality. Visual analysis of the full dataset of 14 voltage channels in Fig-

Figure 8.7 with 120,000 data points is impractical. By applying the same PCA process to the full dataset, further understanding of the dataset can be achieved by reducing the dimensionality of the voltage data. In Figure 8.17 the PCA algorithm has been applied to the full dataset shown in Figure 8.5. Figure 8.17 (a) shows the resulting principal components against the relative amount of variation that they describe. Figure 8.17 (b) and (c) show representations of the first two principal components which account for 73% and 20% of the variation in the full 14 channel voltage data respectively. As previously, if the full 14 channel voltage dataset is projected onto the first two principal components shown in Figure 8.17 (b) and (c) a plot of the variation in the network in those two dimensions can be obtained and is shown Figure 8.17 (d). Taking the projections onto p_0 and p_1 will encompass 93% of the variation in the 14 data set. Thus the patterns in the data in these two dimensions and should show significant information despite being reduced from 14 to two-dimensional data.

The ability of PCA has been shown to represent variation in the relative voltage levels within the network in two dimensions in Section 8.3.2. By extension, the two-dimensional representation of the full dataset now encodes that information at a much larger scale. One of the significant challenges in PCA analysis lies with extending it beyond a dimensional reduction tool and examining the physical significance of the patterns in the projection shown in Figure 8.17 (d). A simple example of this could be noting that the projection onto p_0 is always positive. This correlates with a positive difference in relative voltage between the top and bottom of the network area, consistent with the position of the source and drain at the top left and bottom right respectively. Although a simple example, this highlights the potential for physical insight using knowledge of the transformations involved in PCA as well as the physical network system. Such insights could include cluster analysis of points in the p_0, p_1 projection to determine semistable states within the system. We show the evolution of the system between two point in the p_0, p_1 space during a previously identified switching event. In future work the large datasets could be analysed using analysis tools such as kernel density analysis or K-means clustering [Bailey1995] to identify clusters that correspond to common voltage states in the much larger projected data set. Once clusters or features have been established, a reconstruction of the physical voltages that correspond to those clusters can

Figure 8.17: a) plot of the fraction of the variance in the full data along each of the principal components of the full dataset shown in Figure 8.7. Representations of the two most significant principal components p_0 and p_1 are shown in (b) and (c) where the relative contribution to each from the 14 voltage channels that comprise the reference is shown as red (positive) and blue (negative). The projection of the restricted dataset shown in Figure 8.14 onto the first two principal component vectors is shown in (d).

be generated by taking their position in p_0, p_1 and multiplying them by the vectors $\vec{p}_0$ and $\vec{p}_1$. In this way, physical insight can be gained by examining the structure of the data projected in the more manageable two-dimensional projection and then reconstructing

the corresponding 14-dimensional data if necessary.

I hope that the demonstration of the effectiveness of PCA and the simplified data produced by its application to high dimension-switching data can enable a better understanding of future work on spatiotemporal switching. As advances in measurement systems allow more and more spatial granularity in electrical measurement across the network area and thus higher dimension datasets, the results will become less and less tractable for more intuitive analysis. PCA is scalable within the limits of computation, and so can be an important technique for analysis and visualisation moving forward with multidimensional artificial synaptic data analysis.

8.4 Conclusion and future work

ASN based devices were successfully fabricated which showed electrical characteristics consistent with network-wide filament growth across Ag–Ag₂S–Ag followed by switching behaviour consistent with the repeated breaking and reformation of those filaments throughout the network. The semi-stable conduction states measured across the ASN under periodic driving voltages have been shown to be consistent with a network of symmetric Ag₂S junctions in a self-assembled critical state.

To better characterise the switching events within the critical network system, MEA-based devices were developed allowing high sample rate conductance data as well as multichannel voltage measurements across the device area to be made. Using a thresholding method, the time and magnitude of switching events in MEA devices driven under constant voltage were analysed. The magnitude of conductance switching events and the time intervals between them show power law dependence consistent with self-organised criticality ($\alpha = 1.5$), with exponents of $\alpha = -1.45 \pm 0.12$ and $\alpha = -1.40 \pm 0.08$ respectively over 1.2 orders of magnitude. Power law behaviour is consistent with bursty behaviour across a number of systems such as neuronal firing patterns [168], and systems showing self-organised criticality [2, 21]. In future, higher sampling rates and longer measurement times could improve the accuracy and range of these fits, strengthening the analysis of the self-organised criticality in these ASN systems. Increase in the number of channels of voltage data will add better granularity to the analysis in

the next generation of MEA devices.

Simultaneous measurement of the voltage across the ASN device area during switching was performed. The voltages showed relative change, despite a high degree of clustering of the voltage values. The validity of these voltage measurements on a new measurement system was established by considering control measurements, and the cause of the voltage value clustering was discussed. Switching events were shown to be due to resistance changes throughout the network area by observing shifts in the relative voltage between channels. PCA was applied as a novel analysis technique on ASN devices to facilitate the analysis of the large multichannel datasets comprised of 100,000 time points of 14 channel voltage data. When PCA was used to reduce the dimension of the voltage data over a known switching event, the evolution of the data in two dimensions showed movement between two regions of the 2D space. This demonstrates that the information loss inherent in any dimension reduction still preserves the relative changes consistent with switching within the network. When applied to a full switching dataset, the data shows qualitative evidence of clustering behaviour, consistent with switching between multiple network states. Extended analysis of the clustering behaviour of the data after PCA based reduced dimensionality could in future allow quantitative identification of the movements between stable states over entire large datasets.

A successful fabrication and measurement process was developed which allowed the demonstration of key physical characteristics of the Ag–Ag₂S–Ag ASN system. Spatiotemporal switching in those systems was then analysed to attribute their behaviour to a critical system where switching was distributed across the network area, an important criterion for potential application in neural computing.

Chapter 9

Conclusions and future work

The initial inspiration for this work was to produce an integrated CNT and ASN device. Fabrication of a specific end-product device was pivoted to be an investigation of the impact of the spatially distributed conduction through both systems on their overall conduction properties. The fabrication processes developed, and analysis techniques applied to the systems measured, have paved the way for future device applications based on spatially extended complex networks of conducting nanomaterials.

A device platform was designed and fabricated to allow localised gating of a CNT film, building off of existing experience in fabricating network carbon nanotube (CNT) field effect transistor (FET) devices [101]. The intent was to provide insight into fabricating a tunable conductivity layer as a control for an integrated neuromorphic device platform. These top gated devices were used to determine the effect of local gating on CNT networks. Local gate sensitivity increased sharply at low network densities and a corresponding gradual increase in global gate sensitivity. These trends were attributed to Schottky barriers at dominant metallic-semiconducting (m-s) junctions within the CNT networks. I developed a numerical CNT network model to allow Monte Carlo simulation of network connectivity and conduction. When compared with experimental results, the variation in local and global gate sensitivity was qualitatively similar. The simulation results and their comparison with experiment support the dominance of m-s junctions in key conducting paths within the network that become prominent at low network densities.

The neuromorphic systems studied in Chapter 8 were Ag–Ag₂S–Ag atomic switch networks (ASNs) first developed by the Gimzewski group [8, 17]. I developed a fabrication process for ASN systems on multi-electrode devices based on their work. A measurement system was also designed and implemented to allow time-resolved multichannel measurement of these ASN devices. The systems fabricated were demonstrated to act as atomic switch networks comparable to those in literature [8, 16, 17]. The power-law scaling of the switching dynamics of the ASN systems was demonstrated to be consistent with self-organised criticality [21]. The spatiotemporal variation of switching events was analysed by the novel application of principal component analysis to ASn systems. The capability of PCA to encapsulate the significant dynamics in the system at reduced dimensionality was demonstrated.

The key results of this work are expanded below, and the future application of the research performed herein is discussed.

9.1 Locally gated CNT films

The primary challenge in exploring a locally gated CNT FET device with both global back gates and patterned localized top gates was the fabrication of a device stack that incorporated a dielectric layer that was easily patterned, of comparable dielectric strength to the SiO₂ used as the back gate dielectric, and robust to fabrication of electrodes on top of it. The dielectric chosen was the photopolymer SU8, which is directly patternable, has a dielectric constant matched to within 2.5% to SiO₂, and when hard-baked is robust to chemical damage [135, 136, 204]. Uniform insulating SU8 dielectric layers were fabricated that were robust down to thicknesses of 180 nm, after re-engineering the bottom electrode fabrication process to remove edge spikes that were breaching the dielectric layer.

The photolithographically defined local top gate CNT FET devices were used to examine the impact of gating localised regions of the CNT network on the overall device performance for devices with varying densities of CNT networks. An in-depth analysis of the network topology and morphology was performed using AFM images of the CNT network in the conducting channel of each device. AFM cross-sections were used to de-

termine the diameters of the mixed single CNTs and bundles in the networks fabricated. A 13% metallic bundle content was calculated from 1% metallic CNTs using circle packing to determine the probability that a bundle contained a metallic tube.

A stick fitting method for determining the density of bundles in the networks allowed a more granular analysis of density than is typical in the literature. The variation in density across the film was shown to change significantly with density. High-density films showed variation in the measured density higher than what would be expected for a Poisson random process, while low-density films measured were far more regular than random. The attraction between CNTs in solution and those already deposited on the surface was discussed as a possible physical mechanism that would cause this variation in the network density. The variation in density was consistent with devices which were observed to conduct with average densities as low as 4 bundles/ μm^2 , far below the classical percolation threshold [121] of 13.3 bundles/ μm^2 calculated from the average bundle length measured.

The on-off ratios of devices were measured with CNT network densities from 4 bundles/ μm^2 to 20 bundles/ μm^2 for the global back gate and two different local top gate regions. The on-off ratios from the global back gate increased gradually from 10 to 10^4 as the network densities decreased. The on-off ratios of local top gates were <10 for network densities above 10 bundles/ μm^2 . For lower network densities there was a sharp increase in local on-off ratios up to 10^3 . The trends in the on-off ratio for both the local and global gates were attributed to the increased dominance of Schottky barriers formed at m-s junctions within the network due to the network topology. This view is a departure from the standard view of the on-off ratios being dominated by metallic shorts across the network [25, 32], but is supported by research on the well known Schottky barriers at m-s junctions that have been shown to dominate the conduction and gating in crossed nanotubes [15, 68]. Scanning probe measurements in the literature show dominance of m-s junctions in CNT network conduction [14, 31, 80, 97, 124, 126]. The CNT networks fabricated showed maximum metallic bundle densities of 2.7 bundles/ μm^2 which is well below both the classical percolation threshold of 13.3 bundles/ μm^2 , and significantly below the minimum density for conduction observed in Chapter 4. Thus, there were no metallic conduction paths across the network. I proposed instead that

as the network density was lowered there were fewer conduction paths that locally circumvent the highly gate-dependent m-s junctions, and thus, the m-s junctions come to dominate the overall conduction. The sharp increase in the on-off ratio for local gates was attributed to the lack of parallel conduction paths such that by gating only the m-s junctions in restricted regions the overall conduction is significantly affected.

9.2 Simulation of junction dominated CNT networks

I developed A numerical simulation of a network CNT FET device to compare with the experimental results observed. The simulation was assumed to have only the m-s junctions as gate-dependent elements to examine the response to local and global gating at varying network densities. The system was modelled by generating sticks of length L from the experimentally measured bundle lengths with random orientation and position in a $60\text{ }\mu\text{m} \times 60\text{ }\mu\text{m}$ area. A metallic probability of 13.5% bundle probability was used, obtained by assuming any bundle which contains a metallic tube acts as metallic as described in Chapter 4. The m-s junctions were set as the sole gate-dependant elements. A graph structure of the sticks and the junctions between them was generated to allow calculation of the current through junctions and the voltage at sticks throughout the network for arbitrary junction conduction. Designing the simulation so that the gate voltage could be varied locally allowed direct comparison with the locally and globally gated experimental systems measured in Chapter 4.

The percolation threshold for this system was numerically calculated to be $8.67\text{ sticks}/\mu\text{m}^2$ using Monte Carlo methods to sample multiple realisations of the system at the same network density. This is 35% less than the classical percolation threshold of $13.3\text{ bundles}/\mu\text{m}^2$, which was attributed to the variation in stick length and finite system size which are not accounted for in the classical percolation threshold [121]. The numerically calculated threshold was twice the minimum conducting density of $4\text{ bundles}/\mu\text{m}^2$ observed in the experimental devices, which was attributed to the non-Poisson random network in the experimental system, while the model simulates a Poisson random process. These discrepancies with classical percolation threshold, which is often used in literature [27–30], and the experimentally observed conduction threshold

highlights a need for a more nuanced treatment of this threshold in the literature and future work.

Gating in the simulated network CNT FET used the same gate geometry as the experimental systems. The back-gated on-off ratios increased by three orders of magnitude over a range of network densities from 11.5 , to 9 , and the on-off ratios for the top gates increased from <10 to $\geq 10^2$ for network densities below 10 bundles/ μm^2 . This is qualitatively similar to the transition in on-off ratios from high to low network density as seen in experimental work. Moreover, as the simulation calculates the current through the spatially located elements in the network, the current densities in the system were observed to examine what aspects of the network topology. The current was observed to be distributed throughout the high-density network area with many branching conduction paths, while low-density networks showed few, localised conduction paths. This is consistent with a decreased number of locally circumventing conduction paths that were proposed to be forcing current flow through gate-sensitive m-s junctions consistent with the blocking model put forward by Topinka et al. [31]. The sharp change for local top gates occurs when these conduction paths are so few that there are no paths that do not have m-s junctions in the region gated. These will only occur with some probability at the lowest of network densities. The network topology at low densities forces the current to flow through key conduction paths which contain m-s junctions causing their gate-dependence to dominate the overall network performance. This supports the model of m-s junctions dominating the gating of the entire device at low network densities where the current is forced through conduction paths containing these junctions.

This work supports m-s junctions in key conduction paths that dominate the gate dependence of CNT networks below the metallic percolation threshold. We use this to explain the increased sensitivity of CNT FET devices to local and global gating at low CNT network density. Past research on optimizing the switching characteristics on CNT networks has focused on removing the impact of metallic CNT conduction paths through the network [5, 25]. With the commercial availability of purified CNTs, networks without metallic shorts can be readily fabricated [205]. However, the models for the variation in on-off ratios in FET devices using purified CNT network with varying network densities have been poorly reported. Application of the junction dominated model shown

here will allow future optimization of CNT network systems to produce higher on-off ratios, and the development of new fabrication procedures that enhance the production of network topologies that better enhance the dominance of m-s junctions on gating.

9.3 ASN systems design and analysis

Expertise in fabricating and characterising atomic switch network devices was developed based on the work in the literature by the Gimzewski group [16, 162, 164]. The bottom-up solution-based fabrication processes they used were exchanged for spray coating of silver nanowires to form the silver network. The spray coating method proved to be rapidly iterable and successful at producing initial prototype devices. The sulfurization process and characterisation of the optimal voltage sequence for the initial formation of the metallic filaments across the Ag_2S junctions in the literature were optimised for the devices made here. The systems that were fabricated and measured here showed network-wide formation and subsequent dynamic output to sequential input consistent with a self-organised critical (SOC) internal electrical state.

A device platform that allowed electrical contact to spatially distinct regions of the ASN was designed and fabricated using a multi-electrode array design. The electrical measurement system necessary to take simultaneous measurements from these devices was designed and implemented along with a chip-carrier system that allowed electrical probing of the system without the use of repeated wire bonding. The multi-electrode devices when coupled with the electrical measurement system and chip-carrier allowed rapid fabrication and measurement and short development cycles. The systems were used to measure the response of the ASN systems under DC bias to demonstrate that the systems show SOC. This is an important part of the potential application of such systems to reservoir computing [8, 22].

Simultaneous measurement of the overall current through the ASN systems and the voltage across the multi-electrode array was used to analyse the temporal and spatial characteristics of the switching within the ASN. By using a thresholding technique to identify the size and timing of switching events, a power-law relationship was shown for both the distribution of event sized and the intervals between switching events with an

exponent of $\alpha = -1.45 \pm 0.12$ and $\alpha = -1.40 \pm 0.08$ respectively. The characteristic exponent for two dimensional systems with self-organised criticality is 1.5 [21], which gives good evidence for SOC in the systems measured here. This is in agreement with similar analysis using the power spectral density of the current response in the literature [8, 163, 164].

The voltage traces across the multi-electrode array were examined in detail at manually selected switching in order to examine the spatial extent of the dynamics which had been shown to be due to self-organised criticality in the ASN. The spatial mapping of the voltage was shown to exhibit relative voltage level shifts across those events, despite a tight clustering of the voltage values measured. The validity of the voltage measurements despite this voltage clustering was established, and the clustering attributed to possible high resistance junctions forming between the electrodes and the network compared with resistances in the network area. The relative voltage changes observed indicate that the switching events were localised to within the network area. This manual analysis of switching across the network area was extended by the application of principal component analysis (PCA) to the multichannel voltage data. PCA was used to reduce the dimensionality of the data by transformation into a basis set where the basis vectors encode maximum variation in the data. The relative voltage state over a manually identified switching event was captured by movement between two stable points in the two-dimensional principal component space. The variation observed in two dimensions showed that PCA could be used to reduce the dimensionality of high dimensionality switching data without losing key information on the relative voltage changes consistent with internal switching in the network. PCA was then applied to an entire dataset to highlight its application for dynamic analysis of switching systems with multidimensional output data.

9.4 Future work

Further investigation into local top-gating of CNT networks via altered patterns of top gates can now be implemented using the optimised device stack fabrication in Chapter 3. Top gate configurations such as interdigitated electrodes to allow electrical mod-

ulation of the length of conduction paths through the network, or low size top gates fabricated using electron beam lithography combined with whole-network AFM imaging could be used for deterministic patterned gating of single junctions or specified conduction paths.

Applying the stick fitting method used in Chapter 4 to whole-network AFM images would enable a more robust analysis of the distribution of density that was done here for networks of deposited CNTs. The physical cause of the observed change in the density uniformity with average density bears further investigation because film density is an essential parameter for electrical performance optimisation in this work and in the literature. Such density uniformity variation will have a significant impact on device uniformity and reproducibility due to the impact of density on-conduction.

Extending the CNT network simulation presented in Chapter 5 to incorporate the density variation observed in physically fabricated CNT networks would enable numerical calculation of ρ_{Th} that approach the true threshold for a connected system. When the distribution of lengths and finite area are considered as well, the numerical simulation would produce a threshold for the system more accurately than the widely used but simplistic classical stick percolation model [27, 121, 123].

The simulation codebase developed in Chapter 5 was intentionally designed to be easily extensible to other methods of generating the physical system and varied conduction mechanisms. Conducting element models that have arbitrary current or charge dependence or explicit time dependence could be implemented without significant refactoring of the base code structure, provided that the conduction elements are linear with the voltage across them. As such, other models of conduction between CNTs such as DOS states based tunnelling [131], or full Schottky barriers [125], or even memristive models with charge dependence [171] could be incorporated into the core simulation functionality.

The simulation could be readily applied to the ASN systems studied here given that the spray deposited silver nanowires with sulfurised memristive junctions have the same basic characteristic as junction dominated CNT networks in that they are conducting sticks in a quasi-two-dimensional film with the electrical components of interest at the junctions between adjacent sticks. The conducting mechanism for atomic switch mem-

ristors could be used, with a change in the simulation to allow for time step updates. However, for accurate network properties, the density of the silver network would have to be measured or calculated. EDS, XRD, SEM image analysis, or optical transmission spectroscopy could all be used as mass sensitive techniques to produce at least a relative scale for the density of silver nanowires, if not an absolute measurement of density. Direct control of the network structure would be a significant improvement over using sulfurization to tune the resistance value of the network. Either better characterisation of the sprayed silver network density or further work towards implementing ELD deposition methods as used by the Gimzewski group are important for moving beyond proof of concept ASN devices. More control over network topology, not just the resistance after sulfurization, is necessary for inter-device characterisation.

Extending the analysis and measurement of the MEA systems shown in Chapter 8 will provide continued valuable insight into the complex network conduction and their application towards computational use. In particular, longer length, higher time resolution measurements would provide sufficient data to extend the power-law event analysis shown here and apply burst and average analysis to explore the correlation between events. The first generation of the electrical contact system developed can be optimised to reduce free wiring and rough un-shielded PCB design which are sources of capacitive and inductive interference. The existing electrical measurement system could thus be improved to take advantage of the high time resolution that the instruments are capable of.

I have shown that PCA can be used as a novel analysis method for ASNs, and has significant potential for future post-analysis after dimension reduction. Chapter 8 shows the ability of PCA to reduce feature-rich multidimensional data of switching events to a two-dimensional representation without significant information loss. The reduced dimensionality information is in a form suitable for 2D statistical analysis of the dynamics and state stability of the ASN device when operating as a dynamic system. For more quantitative analysis in future work, clustering or dynamic analysis in the two-dimensional principal component space would provide direct insight into the spatiotemporal signal variation on arbitrarily large ASN systems, while leveraging mature analysis techniques in two dimensions.

Using the models proposed here to provide a more in-depth analysis of the nature of the CNT network conduction a device with on- and off-conductance matched to the switching range of an ASN system is possible. The change in the dynamics of such a system when measured without a CNT layer, and when the CNT layer is gated locally can be characterised by the ASN analysis techniques developed here. Insight into how the dynamics of such an integrated ASN system will evolve when the connectivity is modulated via a CNT layer can be applied to future biologically-inspired computational platforms.

Appendix A

Detailed photolithographic recipes

All photolithographic exposure was performed on a Karl Suss MJB3 mask aligner, equipped with an USHIO SHP 350 W lamp. The measured dose of our machine was 20 mW/cm². All exposure times stated are at this power.

A.1 AZ1518 positive photoresist

1. AZ1518 was dropped onto the surface of the substrate such that the surface was covered, with care being taken to make sure that there were no gaps in the coverage or bubbles in the resist.
2. Spincoating was used to spread the photoresist across the substrate evenly and to flick off any excess resist. For a 1.5 µm resist layer the substrate was spun at 4000 rpm for 1 min with an acceleration of 10 425 rpm/s.
3. The chips was then pre-exposure baked for 1 min to 2 min on a hotplate at 95 °C to stabilize the resist.
4. After aligning the chip with the pattern in the mask aligner the chip was then exposed for 8 s.
5. The chip can then be developed by agitating for 10 s in a 1:4 dilution of AZ351B developer to deionized water. A subsequent rinse in deionised water removes any

remaining developer or debris.

The AZ5214E photoresist was designed as a positive photoresist that can be used in what is called an image reversal process [138] to produce a negative pattern instead. Crosslinking was achieved by performing a precise bake step after exposing the regions to be crosslinked to UV.

A.2 AZ5214E T-profile recipe

1. Spin AZ5214E at 4000 rpm for 1 min with acceleration of 10 425 rpm/s.
2. 95 °C prebake on a hotplate for 1 min.
3. Flash expose for 0.15 s *note that this is the minimum exposure available to our machine.*
4. Crosslinking Bake at 110 °C on a hotplate for exactly 2 min. This is a crucial step and should be handled with care.
5. Mask expose 12 s.
6. Develop for 40 s in 3:1 AZ326:DI as per normal, or 20 s in 1:3 AZ351B:DI rinse 10 s in water and N2 blow dry.

A.3 AZ 5214E image reversal

1. Spincoat AZ5214E at 4000 rpm for 1 min with acceleration of 10 425 rpm/s (acl=75).
2. Bake for 1 min at 95 °C on a hotplate .
3. Expose with a mask for 6 s. This was approximately half the standard time for conventional positive photoresist which is suggested in the AZ5214E datasheet and was corroborated by testing of exposure time.

4. Crosslinking bake at 110 °C on a hotplate for exactly 2 min. This is a crucial step and should be handled with care. Chips were placed on a clean area of the hotplate near to center to ensure good temperature control and conduction.
5. Flood expose all the chips for 30 s without a mask.
6. Develop for 60 s in 3:1 AZ326 or 30 s in 1:4 AZ351B, rinse 10 s in water and N₂ blow dry.

A.4 Sub 500 nm SU8 Recipe

The solid GMPI 1060 SU8 was remarkably difficult to dissolve, and so in order to produce a solution that was free of any lumps, the SU8 was stirred at 300 rpm with a small magnetic stirrer bar for 24 h on a hotplate at 70 °C. Because of the photosensitivity, the vials were wrapped in tinfoil for the duration.

Note: this recipe was for small 8 mm × 4 mm chips. Spin speed and acceleration may need to be changed for other chips or other SU8 mixtures

1. Drop 2 drops of 10 % or 15 % SU8 (GMPI 1060 used) in cyclopentanone on substrate.
2. Spin 40 s at 6000 rpm with acceleration of 10 425 rpm/s.
3. Pre exposure soft bake for 1 min on a hotplate at 95 °C
4. Mask expose 10 s.
5. Post exposure soft bake for 1 min at 95 °C on a hotplate. This step is critical to crosslink exposed areas, without it all the SU8 just washes away in developer.
6. 20 s develop in concentrated SU8 developer followed by an IPA rinse and N₂ blow dry.
7. Hard bake for 15 min on a hotplate at 200 °C to fully crosslink and ensure solvent resistance if mechanical and chemical stability is required. Barring aggressive O₂ plasma, SU8 is impossible to remove after this step.

This recipe was developed after determining the spin curves for 10 % and 15 % SU8 solutions made with GMPI 1060 SU8 shown in Figure 3.3. These curves were used to determine the optimum speed and solution to achieve sub 500 nm films.

Wafer protection.

1. Cover surface of the wafer with 15 ml of AZ1518.
2. Spin at 2000 rpm for 40 s.
3. Bake for 10 min at 95 °C on a hotplate.
4. Pour 10 ml of PDMS, trying to cover wafer as uniformly as possible.
5. Spin at 600 rpm to 900 rpm for 40 s.
6. Cure PDMS by baking 1 h on a hotplate at 90 °C, 3 h at 60 °C, or 2 days unbaked.

Appendix B

Detailed simulation algorithm information and code repository

B.1 Code repository and Open Source Licensing

The simulation code for this work was written in Python 3.5, with some bash scripts included to facilitate Monte Carlo measurements on large computing clusters.

The code is located on Github and is covered under the MIT license, which is a short and human-readable license that allows free and open use provided the copyright and license are preserved.

B.2 Simulation details

The simulation generates the tubes using density, metallic percentage, and length distribution as parameters. It then calculates the network intersections and converts that into a conducting network where the intersections are the conducting elements. The only requirement of those conducting elements is that they have a conductance(resistance).

The simulation yields a complete map of the physical network, as well as a current and voltage map within the network. The total current can be compared with experimental current values.

Parameter	Value Used	Description
ρ	$1/\mu\text{m}^2$ to $20/\mu\text{m}^2$	density of sticks generated in the device region
l	$60\ \mu\text{m}$	The edge length of the network such that the network area $A = l^2$
L	$(0.66 \pm 0.44)/\mu\text{m}^2$	distribution of stick lengths. Truncated gaussian with $n = 0.66$ and $\sigma = 0.44$ chosen to match experimental measurements. See Section 4.3
p_m	13.5 %	percentage of tubes that are denoted as metallic as opposed to semiconducting. Determined from experiment. See Section 4.3

Table B.1: Input parameters for the CNT FET simulations used in this work. The parameter is given along with a description of its use as well as the values used.

Column	Ex. Value	Description
sticks	36000	total number of sticks generated in the simulation
scaling	60	size in microns of the device area
density	10.0	density in sticks per μm^2
current	0.006	total current across the device in Amps.
gatevoltage	-10.0	voltage applied across the gate for the given gate configuration
gate	back	gate configuration: back gate, partial/total top gate
nclust	6153	number of connected clusters of sticks
maxclust	26593	size of the largest connected cluster of sticks
fname	...	filename for data
onoffmap	0	which mapping of on-off ratios to m-s, s-s, m-m junctions, 0 indicates that only m-s junctions have gate-dependence as discussed in Section 5.2.1
seed	794759425	random seed used to generate the network
runtime	11618	computation time on a single processor
element	LinExp	what conduction equation was used for the junctions. In this work the LinExp equation refers to Equation 5.6.

Table B.2: Simulation outputs with example values given for a simulated network with a density of $\rho = 10$ sticks/ μm^2 as well as description of the significance of each output.

The simulation code is fully functional and able to be run at high throughput on the computational cluster used. Statistically significant data runs can be produced overnight with multiple realizations of a random network with the same parameters. The systems that have been simulated were $60\text{ }\mu\text{m} \times 60\text{ }\mu\text{m}$ device areas with densities from 5 bundles/ μm^2 to 20 bundles/ μm^2 (18k to 72k sticks). For example: The highest density networks were simulated take 2.5 hours on a single modern CPU. By farming out measurements onto a computational cluster (256 cores), Monte Carlo measurements are possible with 100 realizations of each network density across 5 network densities in ~ 6 hours (500 total systems measured).

B.3 Optimisation for large systems

After a proof of concept to show functionality, a good deal of optimization was required to be able to simulate networks over an experimentally comparable network size. Initially when developing the code the networks simulated were over a $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$ square region, and a single simulation run would take approximately 15s on a single CPU. The experimental devices shown in Chapter 4 have $60\text{ }\mu\text{m} \times 60\text{ }\mu\text{m}$ device areas which would necessitate simulating 144 times more sticks than a $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$. Many of the operations and data structures used in the simulation scale nonlinearly with the number of objects simulated.

It was clear that optimization of the code was necessary. Areas of significant resource use were identified to be:

- Matrices used in MNA to solve for conduction were large and memory intensive
- Intersect search was a brute force two body interaction search causing a huge computational bottleneck as 4.9 billion intersect checks were performed
- Cluster determination was performed during the intersect check and necessitated a search of the full stick data structure every time an intersect was found
- Data structures used were initially all Pandas DataFrame objects, to facilitate easy human readability during development and debugging. They were not optimized

for speed.

To solve for conduction in the electrical network, the adjacency matrix of the network is calculated. This has a size of $N^2 \times N^2$ for N sticks in the network but is primarily a sparse structure matrix due to the low connectedness of the graphs involved. CSR (compressed sparse row) sparse matrices were used to form the components of the matrix equation $\underline{A}\vec{x} = \vec{z}$ required to solve for the conduction of the network using multi nodal analysis (MNA) [154] for their ease of slicing and concatenation. The final matrix $\underline{A}$ was converted to a CSR type sparse matrix for the efficiency increase when solving the sparse linear algebra.

Intersect detection using KDtree datastructures

Intersect detection is performed by using a standard algorithm for determining the intersection between two line segments. In the brute force case shown in Listing B.1 the algorithm will pairwise check whether each stick intersects with each other stick.

Listing B.1: Brute force intersect detection pseudocode

```
for i in sticks:
    for j in sticks:
        check_intersect(sticks[i], sticks[j])
```

For a device area with dimensions close to the average stick size, this algorithm is reasonably efficient, as the possible region around each stick in which other sticks could reside with a chance of intersection is comparable to the total area. However, for physically reasonable device areas such as ours where the dimension of $d = 60 \mu\text{m} \gg \langle L \rangle 0.66 \mu\text{m}$, the region around each stick in which another stick could exist which has a possibility of intersect is $< 1/1600$ of the total device area. To effectively search for intersects a range search approach was taken, where only those sticks within some search radius R of stick i would be checked for intersections. Brute force calculation of which sticks are within radius R of stick i takes time $t_{worst} = O(N)$ as each other stick must be checked.

A KDTree data structure was implemented to effectively perform a nearest neighbor search. A KDTree is a k-dimensional space partitioning tree where each k- dimen-

sional point in the data set is a node. Each non-leaf node splits the space into two parts along a dimension. Points less than this split in that dimension will be in the left subtree and all others in the right subtree. Each non-leaf node is usually selected based on a median value in the dimension to be split to produce a balanced tree [206]. Nearest neighbor search algorithms on a KDTree use the structure to eliminate large portions of the search space quickly. This is achieved by traversing the tree recursively from the root downwards and comparing whether the point is greater or less than the split defined by each node. When the algorithm reaches a leaf node, it sets that as the best neighbor and then unwinds the recursion to determine if any of the other nodes are closer than this best point. All radius checks to determine if nodes are closer are reduced to comparisons in a single dimension because of the underlying data structure [206]. A range search for points within some radius R of some search point i takes time $t_{worst} = O(kN^{1-1/k}) = O(\sqrt{N}/2)$ in 2D space ($k = 2$) [147]. For a simulation of $N = 70000$ points this means a factor of 132 increase in the search time compared to the brute force range search.

To further optimize this range search prior to checking intersection, the radius R of the search was set to be equal to L_i the length of the stick i . As long as the sticks are checked in order of descending length, no intersections will be missed. For a stick of length L_i , there are no sticks with center points within L_i of the center point of i with $L > L_i$ that could have intersects with i that would be missed, as those sticks will have already been searched previously.

The optimized intersection code incorporating a length sorted range search where the radius of search to determine intersects with stick i is L_i is shown in Listing B.2:

Listing B.2: Radius sorted KDTree based intersect search pseudocode

```
sticks['cluster']=sticks.index
sticks.sort_values('length',descending)
L=sticks.length
tree=spatial.KDTree(sticks)
for i in sticks:
    neighbors = tree.radius_search(center=sticks[i],
                                   R=L[i])
```

```
for j in neighbors:
    if i < j: # removes double/self counting
        check_intersect(stick[i], stick[j])
```

Cluster detection using graph connected components

Cluster detection was initially performed during intersect detection as follows: All sticks were initialized with a different cluster number. When an intersect was detected between two sticks with cluster numbers c_a and c_b all of the sticks with a cluster number c_b had their cluster numbers changed to c_a . Thus, for each intersect detected there was a search and replace across the entire set of sticks.

So many searches of data structures for each step added computational complexity to the already resource intensive process of intersect detection. Instead, the cluster detection was determined after converting the intersects as an edge list to convert the sticks and intersects into a graph. Using the intersects as an edge list will underestimate the number of clusters in the case where there are isolated sticks with no intersects, as they will not be included. This is not especially important, as the maximum cluster size is the metric used, but is noted for completeness. Using a breadth-first search on the graph structure yields rapid cluster determination, independent of the intersection search algorithm [152].

Data structure optimization

Pandas DataFrames are used to store the stick and intersect data. However, the search, slice and replace functions on the DataFrame structure are inefficient compared to the low level numpy array functions with the same functionality. Thus prior to performing the intersect calculation, the stick DataFrame object is split into arrays for the center points, endpoints, and lengths that are then used by addressing indices in the intersect search algorithm.

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